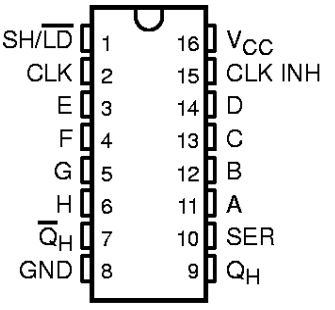
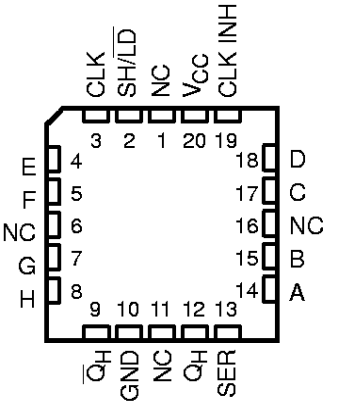
SCLS372 – MAY 1997

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT165 . . . J OR W PACKAGE
SN74AHCT165 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT165 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT165 are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The 'AHCT165 also feature a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

The SN54AHCT165 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT165 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

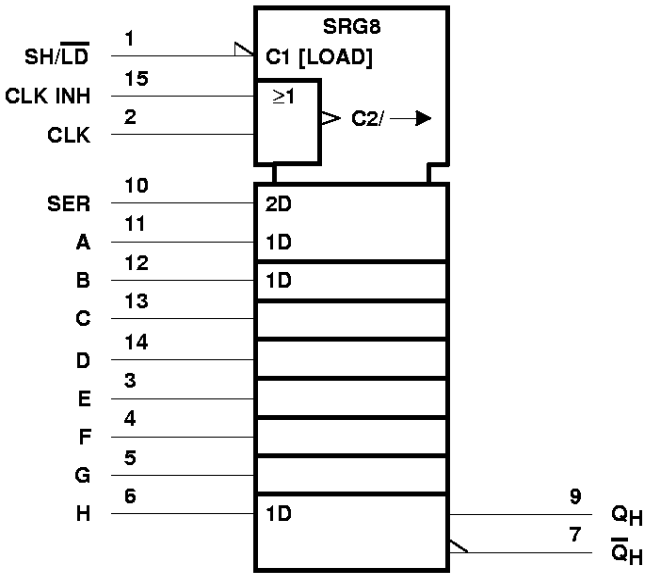
EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift†
H	↑	L	Shift†

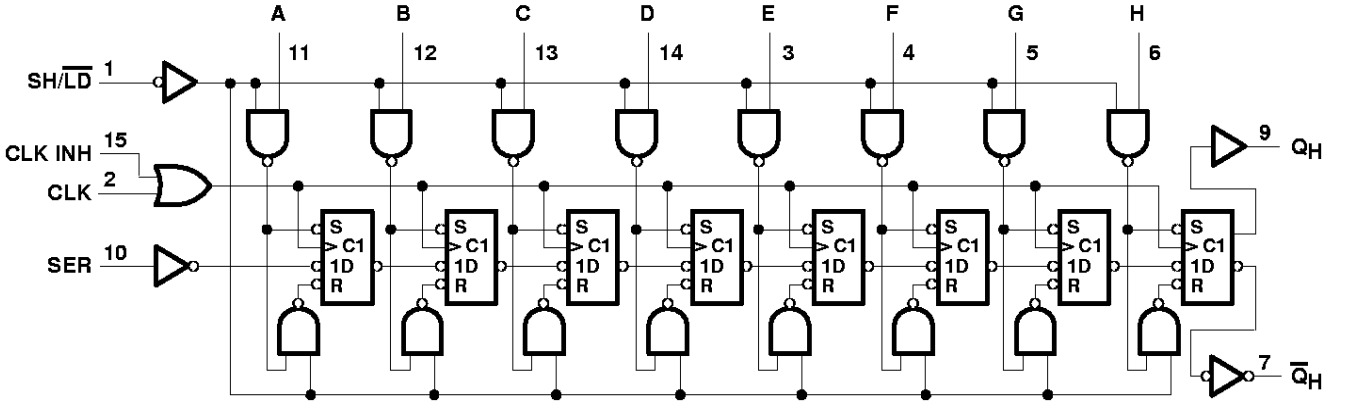
† Shift = content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

typical shift, load, and inhibit sequence