DALLAS SEMICONDUCTOR

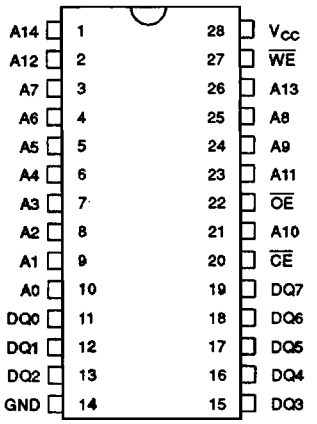
DS2257, DS2257S
32K x 8 3V Operation Static RAM

FEATURES

- Low power CMOS design
- Standby current

  400 nA max at $t_A = 25°C$ $V_{CC} = 3.5V$
  500 nA max at $t_A = 25°C$ $V_{CC} = 5.5V$
  4 µA max at $t_A = 60°C$ $V_{CC} = 5.5V$
  10 µA max at $t_A = 85°C$ $V_{CC} = 5.5V$
- Full operation for V_{CC} = 5.5V to 2.7V
- Data Retention Voltage = 5.5V to 2.0V
- Access time equals 70 ns at 5.0V and 150 ns at 2.7V
- Operating temperature range of -40°C to +85°C
- Full static operation
- TTL compatible inputs and outputs over voltage range of 5.5V to 2.7 volts.
- Available in 28 pin DIP and 28 pin SOIC packages
- Suitable for both battery operate and battery backup applications

PIN ASSIGNMENT



28 PIN DIP OR 28 PIN SOIC

PIN DESCRIPTION

A0-A14	-	Address Inputs
$\overline{WE}$	-	Write Enable Input
$\overline{OE}$	-	Output Enable Input
$\overline{CE}$	-	Chip Enable Input
DQ0-DQ7	-	Data Input/Output
V_{CC}	-	Power Supply Input 2.7V - 5.5V
GND	-	Ground
NC	-	No Connection

DESCRIPTION

The DS2257 is a 262,144 bit low power, fully static random access memory organized as 32768 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 volts and 5.5 volts. The chip enable input ($\overline{CE}$) is used for device selection and can be used in order to achieve the minimum standby current mode which facilitates both battery operate and battery backup applications. The device provides fast access time of 70 ns when operated from a 5 volt power supply input, and also provides relatively good performance of 150 ns access while operating from a 3.0 volt input. The device maintains TTL level inputs and outputs over the input voltage range of 2.7 to 5.5 volts. The DS2257 is most suitable for low power applications where battery operation or battery backup for nonvolatility are required.

OPERATION MODE						
MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 - A14	DQ - DQ7	POWER
READ	L	L	H	STABLE	DATA OUT	I_{CCO}
WRITE	L	X	L	STABLE	DATA IN	I_{CCO}
DESELECT	L	H	H	X	HIGH-Z	I_{CCO}
STANDBY	H	X	X	X	HIGH-Z	I_{CCS}

ABSOLUTE MAXIMUM RATINGS		
SYMBOL	PARAMETER	RATING
V_{CC}	Power Supply Voltage	-0.3V to +7.0V
V_{IN}, $V_{I/O}$	Input, Input/Output Voltage	-0.3 to +7.0V
T_{STG}	Storage Temperature	-55°C to +125°C
T_{OPR}	Operating Temperature	-40°C to +85°C
T_{SOLDER}	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

+5 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Data Retention Voltage	V_{DR}	2.0		5.5	V	

+5 VOLT OPERATION - CONTINUED

DC CHARACTERISTICS (t_A = -40°C TO +85°C, V_{CC} = 5V ± 10%)						
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		±0.1	µA	
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$		±0.5	µA	
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.2V		1.0	mA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=85°C		10	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=60°C		4	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=25°C		500	nA	
Operating Current	I_{CCO}	$\overline{CE}$=0.8V min cycle		60	mA	

AC CHARACTERISTICS (–40°C TO +85°C, V_{CC}=5V ± 10%)					
PARAMETER	SYMBOL	DS2257-70 DS2257S-70		UNITS	NOTES
		MIN	MAX		
Read Cycle Time	t_{RC}	70		ns	
Access Time	t_{ACC}		70	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		ns	5
Output High Z from Deselection	t_{OD}		25	ns	5
Output Hold from Address Change	t_{OH}	5		ns	
Write Cycle Time	t_{WC}	70		ns	
Write Pulse Width	t_{WP}	55		ns	3
Address Setup Time	t_{AW}	0		ns	
Write Recovery Time	t_{WR}	10		ns	
Output High Z from $\overline{WE}$	t_{ODW}		25	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		ns	5
Data Setup Time	t_{DS}	30		ns	4
Data Hold Time	t_{DH}	10		ns	4

+3 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.6	V	
Data Retention Voltage	V_{DR}	2.0		3.5	V	

DC CHARACTERISTICS (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)						
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		±0.1	µA	
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$		±0.5	µA	
Output High Current	I_{OH}	V_{OH} = 2.2V	-0.5		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V		0.5	mA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$ – 0.3V t_A=85°C		4	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=60°C		1	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=25°C		400	nA	
Operating Current	I_{CCO}	$\overline{CE}$=0.6V min cycle		40	mA	

AC CHARACTERISTICS READ CYCLE (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150			ns	
Access Time	t_{ACC}			150	ns	
$\overline{OE}$ to Output Valid	t_{OE}			75	ns	
$\overline{CE}$ to Output Valid	t_{CO}			150	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			ns	
Output High-Z from Deselection	t_{OD}			75	ns	
Output Hold from Address Change	t_{OH}	15			ns	

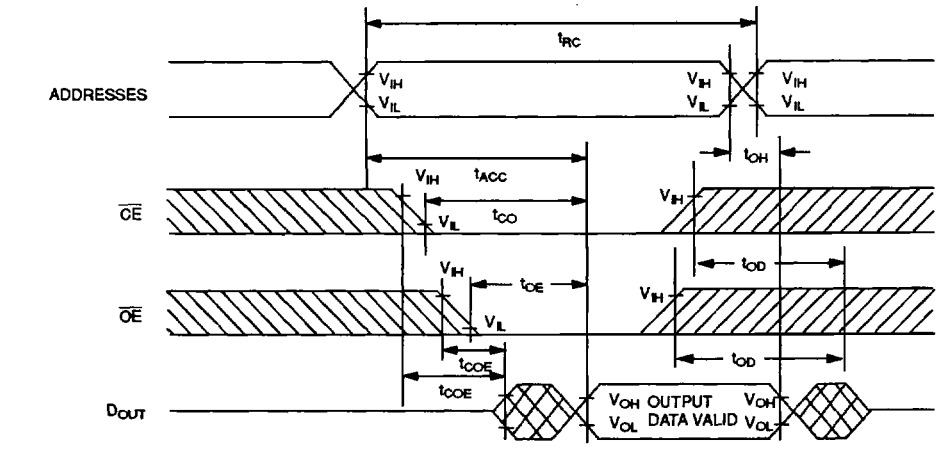
+3 VOLT OPERATION - CONTINUED

AC CHARACTERISTICS WRITE CYCLE (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	150			ns	
Write Pulse Width	t_{WP}	120			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	25			ns	
Output High-Z from $\overline{WE}$	t_{ODW}			75	ns	
Output Active from $\overline{WE}$	t_{OEW}	5			ns	
Data Setup Time	t_{DS}	100			ns	
Data Hold Time	t_{DH}	25			ns	

DATA RETENTION CHARACTERISTICS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Retention Supply Voltage	V_{DR}	2.0		5.5	V	
Data Retention Current at 5.5V	I_{CCR1}		0.1*	10	µA	
Data Retention Current at 3.5V	I_{CCR1}		0.5	4	µA	
Data Retention Current at 2.0V	I_{CCR2}		50*	2000	nA	
Chip Deselect to Data Retention	t_{CDR}	0			µA	
Recovery Time	t_R	5			ms	

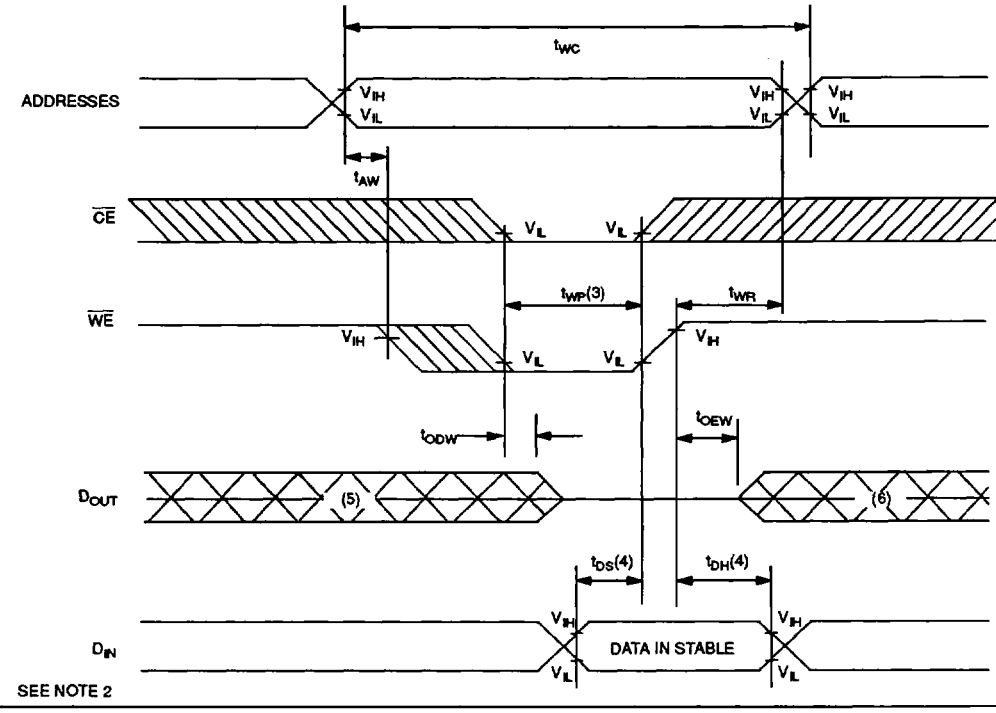
* Typical values are at 25°C

TIMING WAVEFORM: READ CYCLE



SEE NOTE 1

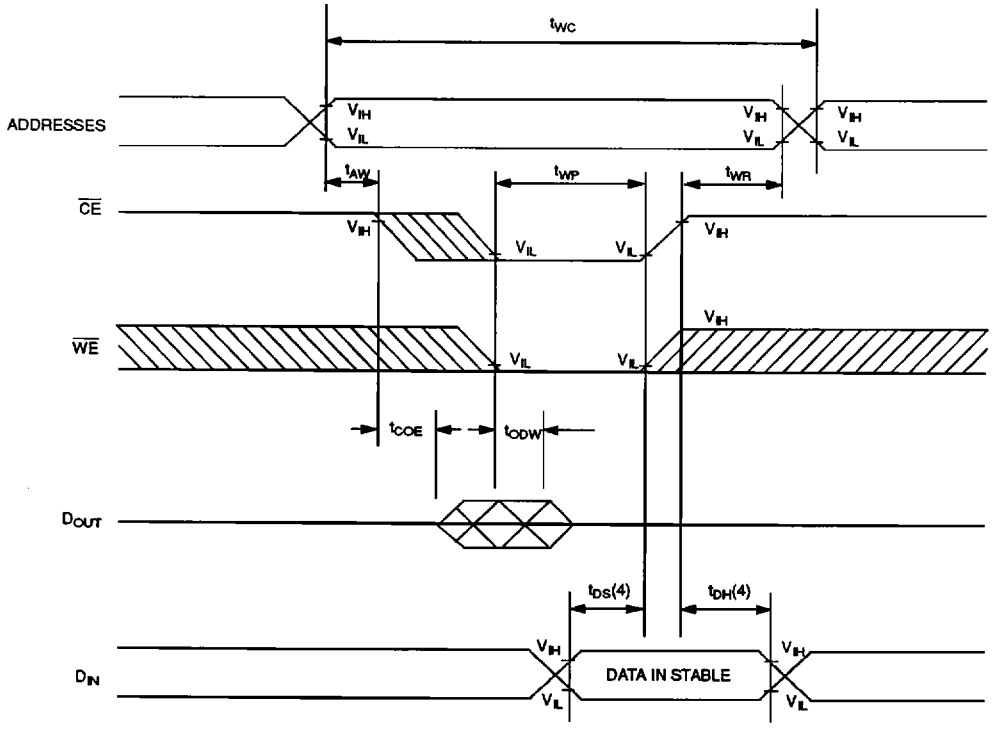
TIMING WAVEFORM: WRITE CYCLE 1



SEE NOTE 2

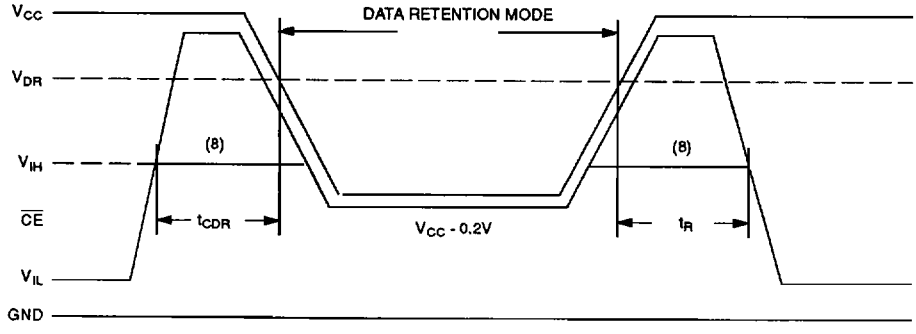
: UNKNOWN

TIMING WAVEFORM: WRITE CYCLE 2



: UNKNOWN

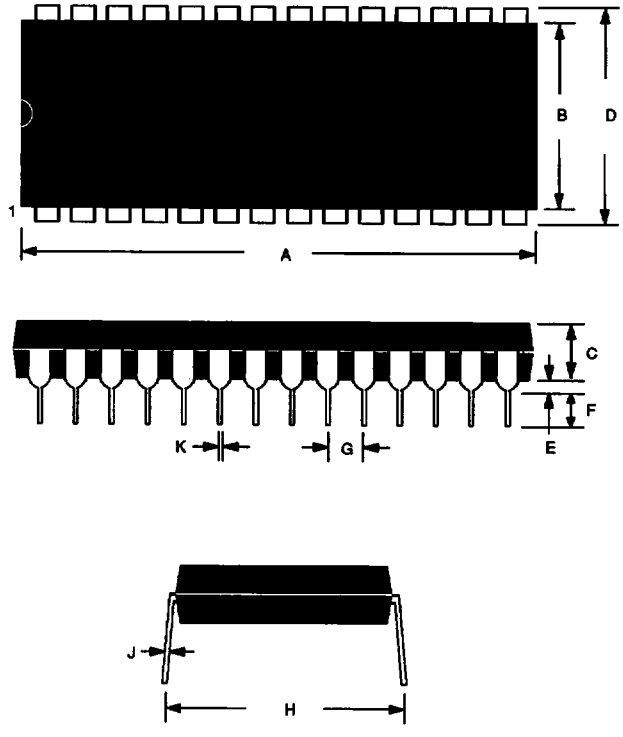
FIGURE 1: TIMING DIAGRAM: DATA RETENTION - POWER UP, POWER DOWN



NOTES

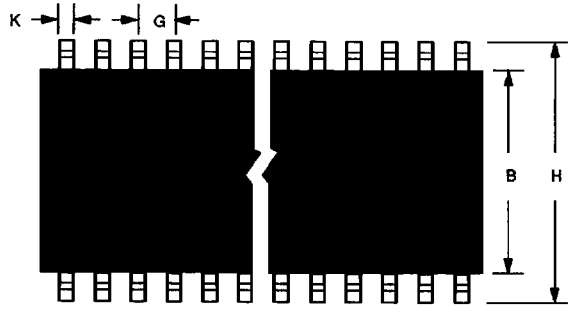
1. WE is high for read cycles.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH} and t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state.
6. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in write cycle 1, the output buffers remain in a high impedance state.
7. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state.
8. If the V_{IH} level of $\overline{CE}$ is 2.0V during the period that V_{CC} voltage is going down from 4.5V to 2.7V I_{CCS1} current flows.

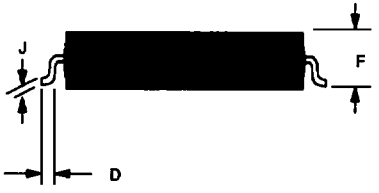
DS2257 28 PIN DIP



PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.440	1.460
MM	30.99	32.00
B IN.	0.530	0.550
MM	13.46	13.87
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.045
MM	0.380	1.02
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

DS2257S 28 PIN SOIC





PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.696 17.7	0.713 18.1
B IN. MM	0.326 8.3	0.335 8.5
C IN. MM	0.092 2.35	0.104 2.65
D IN. MM	0.039 TYP 1.0 TYP	
E IN. MM	0.004 0.100	0.012 0.300
F IN. MM	0.106 TYP 2.7 TYP	
G IN. MM	0.044 1.118	0.056 1.422
H IN. MM	0.453 11.5	0.477 12.1
J IN. MM	0.004 0.10	0.008 0.20
K IN. MM	0.012 0.300	0.020 0.500

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