intel®

PRELIMINARY

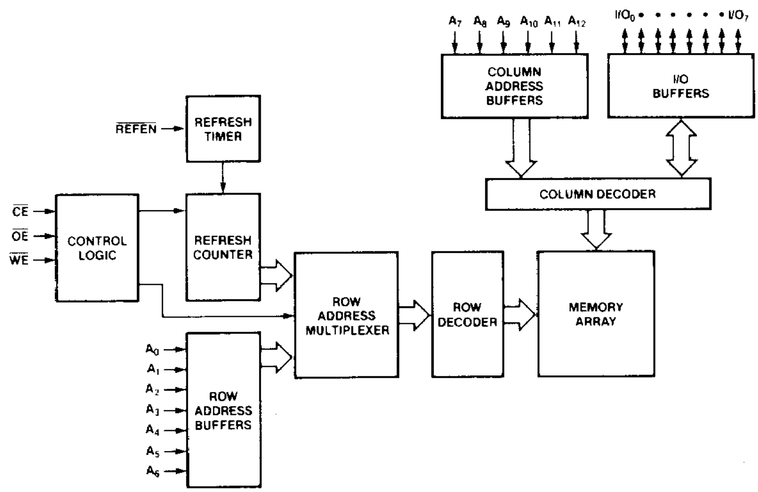
2187A FAMILY
8192 × 8 BIT INTEGRATED RAM

- Low-cost, high-volume HMOS technology
- High density one transistor cell
- Single +5V ± 10% supply
- Proven HMOS Reliability
- Low active current (70 mA)
- Simple synchronous refresh operation
- 2764 EPROM compatible pin-out
- Two-line bus control
- JEDEC standard 28-pin site
- Low standby current (20 mA)

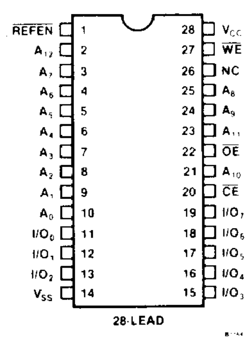
The Intel 2187 is an 8192 word by 8-bit integrated random access memory (iRAM) fabricated on Intel's proven HMOS dynamic RAM technology. Packaged in the industry standard 28-pin DIP, the 2187 conforms to the industry standard JEDEC 28-pin site.

The 2187 is particularly suited for use in microcontroller applications, incorporating many requisite system features. These include low power dissipation, automatic initialization, extended cycle operation and two-line bus control to eliminate bus contention.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

A_0-A_{12}	ADDRESS INPUTS
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O_0-I/O_7	DATA INPUT/OUTPUT
REFEN	REFRESH ENABLE
V_{CC}	+5V POWER
V_{SS}	GROUND

April, 1983

Order Number: 210859-001

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground .... −1.0V to +7V
D.C. Continuous Current per Output .... 10 mA
D.C. Maximum Data Out Current .... 50 mA
D.C. Power Dissipation .... 1.0 W

* *COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS[1]

TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Conditions	Notes
ILI	Input Load Current (All Input Pins)		10	μA	V_{IN} = VSS to VCC	
|ILO|	Output Leakage Current		10	μA	$\overline{OE}$ = VIH	
ICC	Operating Current		70	mA	Minimum Cycle Time	2
ISB	Standby Current		20	mA	$\overline{CE}$ = VIH	
VIL	Input Low Voltage	−1.0	0.8	V		3
VIH	Input High Voltage	2.4	7.0	V		
VOL	Output Low Voltage		0.45	V	IOL = 2.1 mA	
VOH	Output High Voltage	2.4		V	IOH = −1.0 mA	

NOTES FOR D.C. CHARACTERISTICS:
1. Typical limits are VCC = +5V, TA = 25°C.
2. ICC is dependent on outputs loading when the device output is selected. Specified ICC max. is measured with the outputs open.
3. Specified VIL min. is for steady state operation. During transitions the inputs may overshoot to −2.0V for periods not to exceed 20 nsec.

A.C. TEST CONDITIONS

Input Pulse and Timing
Reference Levels .... 0.8V to 2.4V
Input Rise and Fall Times .... 10 nsec.
Output Timing Reference Levels .... 0.6V and 2.4V
Output Load .... See Figure 1

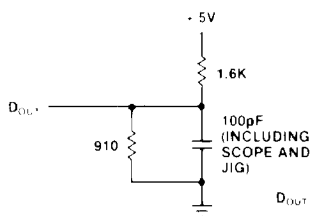


Figure 1.

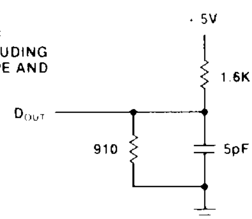


Figure 2.

(FOR HIGH IMPEDANCE MEASUREMENTS ONLY)

CAPACITANCE[4]

TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{ADD}	Address Capacitance	8	pF	V_{ADD} = 0V
$C_{I/O}$	I/O Capacitance	14	pF	$V_{I/O}$ = 0V
C_{IN}	Control Capacitance	14	pF	V_{IN} = 0V

NOTE: 4. This parameter is characterized and not 100% tested.

A.C. CHARACTERISTICS

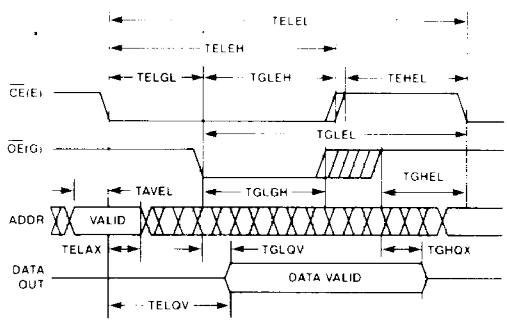
TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted

READ CYCLE ($\overline{WE}$ = VIH)

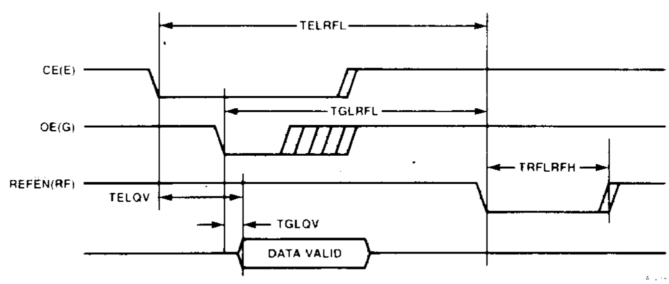
Symbol	Parameter	2187-25 Min.	2187-25 Max.	2187-30 Min.	2187-30 Max.	2187-35 Min.	2187-35 Max.	Unit	Notes
TELEL	Cycle Time	425		500		600		ns	
TELQV	Access Time from $\overline{CE}$		250		300		350	ns	
TGLQV	Access Time from $\overline{OE}$		65		70		75	ns	
TELEH	$\overline{CE}$ Pulse Width	40		40		40		ns	
TEHEL	$\overline{CE}$ High Time	40		40		40		ns	
TAVEL	Address Set-Up Time	0		0		0		ns	
TELAX	Address Hold Time	35		35		35		ns	
TGLEL	$\overline{OE}$ low to next $\overline{CE}$ low	250		275		300		ns	
TGLGH	$\overline{OE}$ Pulse Width	65		70		75		ns	
TGHEL	$\overline{OE}$ high to next $\overline{CE}$ low	40		40		40		ns	
TGHQX	$\overline{OE}$ high to Data Float	0	70	0	70	0	70	ns	1
TELGL	$\overline{CE}$ low to $\overline{OE}$ low		10,000		10,000		10,000	ns	
TGLEH	$\overline{OE}$ low to $\overline{CE}$ high	40		40		40		ns	
TELRFL	$\overline{CE}$ low to $\overline{REFEN}$ low	425		500		600		ns	
TGLRFL	$\overline{OE}$ low to $\overline{REFEN}$ low	250		275		300		ns	
TRFLRFH	$\overline{REFEN}$ Pulse Width	70	9800	70	9800	70	9800	ns	5

WAVEFORMS

READ CYCLE



READ CYCLE FOLLOWED BY REFRESH



A.C. CHARACTERISTICS

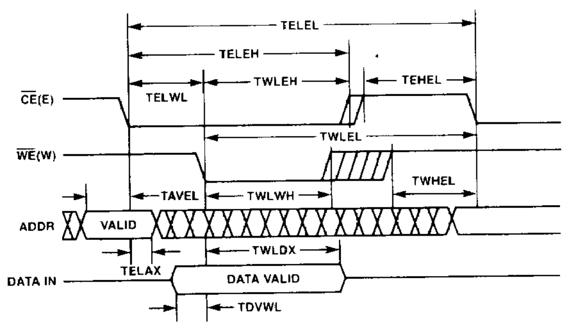
TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

WRITE CYCLE ($\overline{OE}$ = VIH)

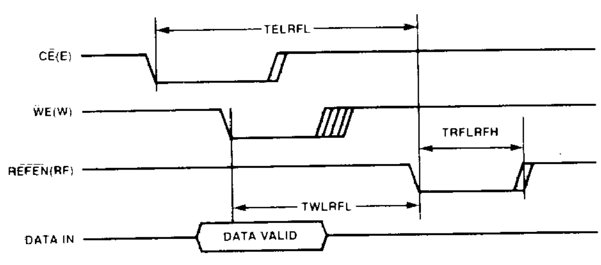
Symbol	Parameter	2187-25 Min.	2187-25 Max.	2187-30 Min.	2187-30 Max.	2187-35 Min.	2187-35 Max.	Unit	Notes
TELEL	Cycle Time	425		500		600		ns	
TELEH	$\overline{CE}$ Pulse Width	40		40		40		ns	
TEHEL	$\overline{CE}$ High Time	40		40		40		ns	
TAVEL	Address Set-Up Time	0		0		0		ns	
TELAX	Address Hold Time	35		35		35		ns	
TWLEL	$\overline{WE}$ low to next $\overline{CE}$ low	250		300		350		ns	
TWLWH	$\overline{WE}$ Pulse Width	40		40		40		ns	
TWHEL	$\overline{WE}$ high to next $\overline{CE}$ low	40		40		40		ns	
TDVWL	Data Set-Up to $\overline{WE}$ low	0		0		0		ns	
TWLDX	Data Hold from $\overline{WE}$ low	40		45		50		ns	
TELWL	$\overline{CE}$ low to $\overline{WE}$ low		10,000		10,000		10,000	ns	
TWLEH	$\overline{WE}$ low to $\overline{CE}$ high	40		40		40		ns	
TELRFL	$\overline{CE}$ low to $\overline{REFEN}$ low	425		500		600		ns	
TWLRFL	$\overline{WE}$ low to $\overline{REFEN}$ low	250		300		350		ns	
TRFLRFH	$\overline{REFEN}$ Pulse Width	70	9800	70	9800	70	9800	ns	5

WAVEFORMS

WRITE CYCLE



WRITE CYCLE FOLLOWED BY REFRESH



A.C. CHARACTERISTICS

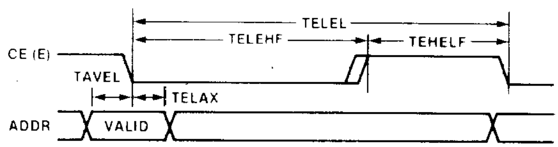
TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

FALSE MEMORY CYCLE ($\overline{OE}$ and $\overline{WE}$ = VIH)

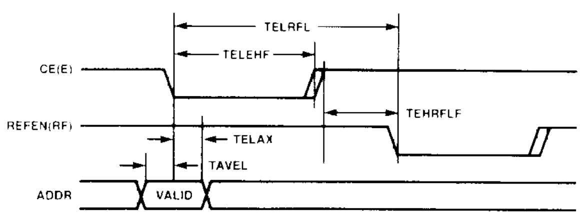
Symbol	Parameter	2187-25 Min.	2187-25 Max.	2187-30 Min.	2187-30 Max.	2187-35 Min.	2187-35 Max.	Unit	Notes
TELEL	Cycle Time	425		500		600		ns	
TELEHF	$\overline{CE}$ Pulse Width	40	10,000	40	10,000	40	10,000	ns	2
TEHELF	$\overline{CE}$ High Time during F.M.C.	200		250		275		ns	3
TAVEL	Address Set-Up Time	0		0		0		ns	
TELAX	Address Hold Time	35		35		35		ns	
TELRFL	$\overline{CE}$ low to $\overline{REFEN}$ low	425		500		600		ns	
TEHRFLF	$\overline{CE}$ high to $\overline{REFEN}$ low after F.M.C.	200		250		275		ns	

WAVEFORMS

FALSE MEMORY CYCLE



FALSE MEMORY CYCLE FOLLOWED BY A REFRESH



A.C. CHARACTERISTICS

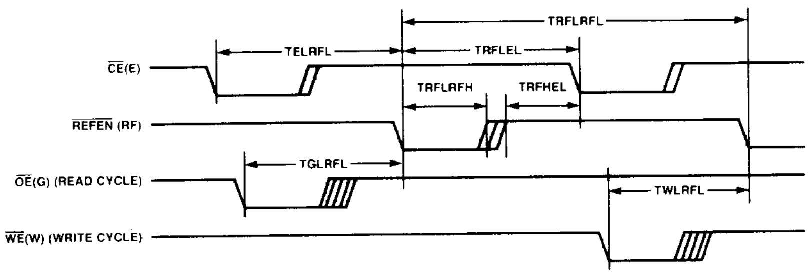
TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

REFRESH CYCLE

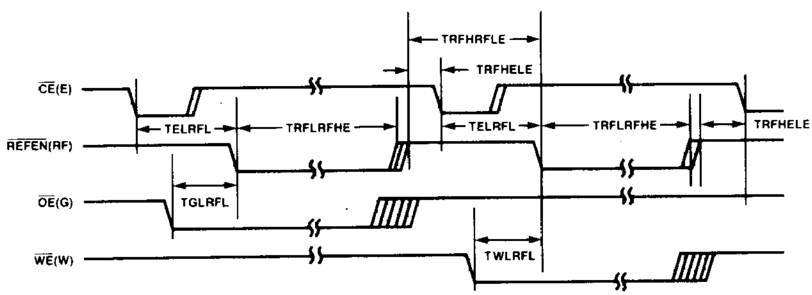
Symbol	Parameter	2187-25 Min.	2187-25 Max.	2187-30 Min.	2187-30 Max.	2187-35 Min.	2187-35 Max.	Unit	Notes
TELRFL	$\overline{\text{CE}}$ low to $\overline{\text{REFEN}}$ low	425		500		600		ns	
TRFLRFH	$\overline{\text{REFEN}}$ Pulse Width	70	9800	70	9800	70	9800	ns	5
TRFHEL	$\overline{\text{REFEN}}$ high to $\overline{\text{CE}}$ low	40		40		40		ns	
TRFLRFL	$\overline{\text{REFEN}}$ cycle time to guarantee refresh	350	15600	400	15600	450	15600	ns	
TRFLEL	$\overline{\text{REFEN}}$ low to $\overline{\text{CE}}$ low	350		400		450		ns	
TRFHELE	$\overline{\text{REFEN}}$ high to $\overline{\text{CE}}$ low — extended cycle	350		400		450		ns	4
TGLRFL	$\overline{\text{OE}}$ low to $\overline{\text{REFEN}}$ low	250		275		300		ns	
TWLRFL	$\overline{\text{WE}}$ low to $\overline{\text{REFEN}}$ low	250		300		350		ns	
TRFLRFHE	$\overline{\text{REFEN}}$ Pulse Width — extended cycle	10,000		10,000		10,000		ns	4,5
TRFHRFLE	$\overline{\text{REFEN}}$ high to $\overline{\text{REFEN}}$ low — extended cycle	425		500		600		ns	

WAVEFORMS

REFRESH CYCLE



EXTENDED CYCLE REFRESH[5]



NOTES FOR A.C. CHARACTERISTICS:

1. Transition is measured ±500 mV from steady state logic level with specified loading in Figure 2.
2. Maximum applies for F.M.C. Only.
3. Note TEHELF > TEHEL.
4. TRFHELE > TRFHEL and TRFLRFHE > TRFLRFH.
5. Extended cycles occur when the $\overline{\text{REFEN}}$ pulse width is ≥10 μsec.

FUNCTIONAL DESCRIPTION

The 2187 has four control pins: CE (Chip Enable), OE (Output Enable), WE (Write Enable), and REFEN (Refresh Enable). These control lines select and control the operation of the iRAM.

CE is the general purpose chip enable line. It is an edge triggered signal that controls several internal operations. An access cycle begins with the leading (falling) edge of CE. At this time, the external address is latched into the 2187 and is held throughout the current cycle. CE may be pulsed or it may remain low throughout the cycle.

OE selects a read cycle and controls the output data bus. When OE goes active (low) during a read cycle, the output drivers of the 2187 are enabled. Data remains valid on the output lines as long as OE is active — independent of the state of CE.

WE is the edge triggered input that defines a write cycle. During write cycles, data is latched from the external bus into the 2187 by the leading (falling) edge of WE. WE and OE may not be active during the same cycle.

REFEN initiates the internal refresh cycles of the 2187. A refresh cycle begins whenever REFEN goes active (low). An internal refresh address counter provides the refresh address. To prevent conflicts between refresh and access cycles, several timing parameters, referenced to REFEN, must be met. These parameters are specified in the timing tables of the 2187 A.C. Characteristics.

Access Cycles

READ CYCLE

A read cycle is initiated when both CE and OE go active low during the same cycle. Access times are specified from both OE and CE. After OE goes active (low), and the hold time for CE has been met (TGLEH), CE may go inactive. As long as OE remains active (low), data remains on the output lines — independent of the level of CE.

WE may not go active (low) during the read cycle.

WRITE CYCLE

A write cycle occurs when both CE and WE go active (low) in the same cycle. Once WE has gone active (low), CE may go inactive after a minimum hold time (TWLEH). The leading (falling) edge of WE latches data from the external bus into the 2187. Data must be valid at this time.

OE must not go active during the write cycle.

FALSE MEMORY CYCLE

A false memory cycle (FMC) occurs when CE goes active (low), and OE and WE remain inactive (high). No memory cycle is performed, but address set-up and hold times must be met to guarantee the integrity of internal data. During an FMC, the 2187 performs a refresh cycle on the externally addressed row.

Note that some of the CE timing specifications for an FMC differ from those of a read or write cycle.

Other Operating Modes

REFRESH OPERATION

The 2187 supports three refresh modes. Two are controlled externally. The third mode can be enabled when the 2187 is not accessed for extended periods of time (during system stand-by or extended cycle operation). An internal refresh timer guarantees refresh to maintain data integrity.

A refresh cycle is initiated by the leading (falling) edge of REFEN. Once a refresh cycle begins, cycle operation is internal and automatic. REFEN may go inactive (high) after the minimum active low pulse time has been met. Addresses are supplied by the internal refresh address counter. To guarantee internal data integrity, REFEN must be strobed at least 128 times in every 2 millisecond period. REFEN pulses may be distributed or grouped (burst mode).

CE may not go active (low) while a refresh cycle is in progress.

The 2187 may also be refreshed by read, write, or false memory cycles. To accomplish this, the user's system must cycle through each of the 128 rows in every 2 millisecond time frame. In this mode, the refresh address is comprised of the seven lowest order address bits (A_0-A_6), supplied externally.

EXTENDED CYCLE OPERATION

Extended cycle operation is useful for single-step operations and is defined by OE or WE remaining active (low) for indefinite periods of time. (CE is allowed to return high). As long as OE is active (read cycles only), data will remain valid on the output bus. During write cycles, data is latched on the leading (falling) edge of WE. Throughout the remainder of the extended cycle, data may change on the external lines without affecting the contents of the iRAM.

To guarantee refresh of the iRAM array during extended cycles, REFEN must go active (low) after CE has gone active (low). While REFEN is low, an internal timer guarantees that the iRAM array is adequately refreshed, thus ensuring data integrity. Refresh cycles will occur automatically, even if OE or WE remains low. *While REFEN is low, CE may not go active (low).* Note that if REFEN is not enabled (low), proper refresh of the 2187 array cannot be guaranteed during extended cycles.

Once $\overline{REFEN}$ returns inactive (high), there are two timing specifications that must be met before the iRAM is accessed again. These are TRFLEL and TRFHELE.

The internal refresh timer may also be enabled (by holding $\overline{REFEN}$ low) when the iRAM will not be accessed for extended periods of time. It is up to the user to ensure that when $\overline{REFEN}$ returns inactive (high), no timing specifications are violated.

Initialization

Once V_{CC} is within specification, the 2187 is initialized by holding $\overline{REFEN}$ active (low) and all other control inputs inactive (high) for 100 microseconds. This may be done any time after V_{CC} meets specification. Normal operation may begin immediately after initialization.

Interfacing Considerations

The 2187 is ideally suited for use with microcontroller systems that use external memory. Figure 1 is an illustration of the simple circuitry required to interface a 2187 and an 8051 microcontroller. In this particular design, all program memory is located in the 8051's internal ROM. External data memory is mapped into the lower 32K bytes of the 8051 address space.

The 2187 is an edge enabled RAM, therefore a stable $\overline{CE}$ clock is necessary to guarantee proper iRAM operation. The system shown in Figure 1 uses ALE (Address Latch Enable) to generate $\overline{CE}$ for the 2187. Because the 8051 generates ALE for all memory cycles, internal and external, ALE must be gated with an external address line. This ensures that the 2187 is only selected during external cycles, and not during the shorter internal cycles. To guarantee data integrity, the 2187 is refreshed whenever the 8051 performs an internal cycle. In this case, the trailing (falling) edge of ALE is used to generate the $\overline{REFEN}$ signal. Once a refresh cycle begins, it will terminate automatically. This design ensures that the 2187 is properly refreshed and that it will always be ready to respond to access cycles in systems running at speeds up to 12 MHz.

Application note 132 "Designing memory systems with the 8K x 8 iRAM", contains a detailed analysis of the iRAM interface. It also describes several designs that incorporate the iRAM into microprocessor and microcontroller systems.

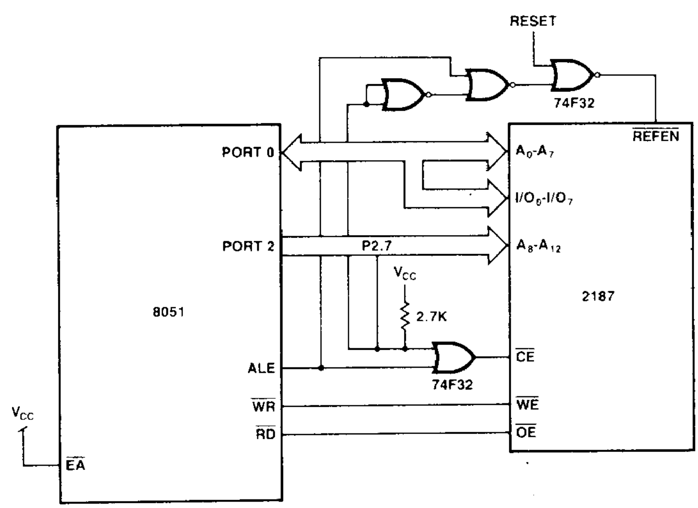


Figure 1. 8051/2187 System Interface

Layout Considerations

To ensure compatibility with other 28-pin memory devices such as EPROMs, several pins require close examination: specifically pins number 1, 26, and 27. Following is a discussion of the system level operation and the design considerations for these pins.

PIN #1

Pin 1 on all EPROMs is reserved for the high voltage programming bias V_{PP}. EPROMS are usually programmed external to the system. Therefore, in normal system operation, pin 1 is connected to V_{CC}.

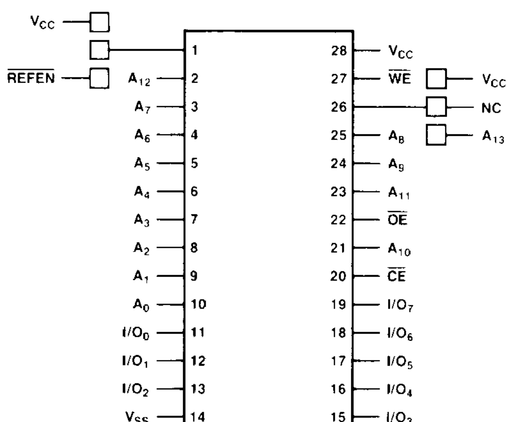
Pin 1 on the 2187 is $\overline{\text{REFEN}}$, the refresh control input. $\overline{\text{REFEN}}$ may come from a microcontroller, or a synchronous refresh timing circuit. In a system incorporating a 28 pin universal site, a trace should be run from pin 1 to the source of the refresh control signal generator, with an alternate trace running to V_{CC}. A jumper option would select $\overline{\text{REFEN}}$ when a 2187 is in the socket. V_{CC} would be selected when the site is occupied by an EPROM. (See Figure 2).

PIN #26

While pin 26 is a No Connect for both the 2186 and the 2764 EPROM, a trace to pin 26 from V_{CC} will guarantee compatibility between 24 pin and 28 pin EPROMs. Pin 26 will carry the additional address bit required to future higher density memories. For flexibility, provide a jumper for an address bit or V_{CC} on pin 26.

PIN #27

Pin 27 is labelled $\overline{\text{WE}}$ on the RAM and $\overline{\text{PGM}}$ on the EPROM. While $\overline{\text{WE}}$ is a system level control signal, $\overline{\text{PGM}}$ is only used when programming the EPROM (V_{PP} at +21V). $\overline{\text{PGM}}$ may be allowed to toggle during normal EPROM operation (V_{PP} at +5V). Therefore, $\overline{\text{WE}}$ may be bussed to every socket location with no jeopardy of illegal operation.



Jumper Matrix Connections

Pin	iRAM	EPROM		
	2187	2732	2764	27128
1	$\overline{\text{REFEN}}$	—	V_{CC}	V_{CC}
26	N.C.	V_{CC}	N.C.	A_{13}

Figure 2. Universal Site Jumper Matrix — iRAM/EPROM Interchange