MOTOROLA

MC55325
MC75325

Specifications and Applications Information

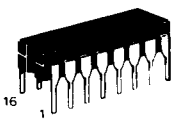
DUAL MEMORY DRIVER

The MC55325/75325 is a monolithic integrated circuit memory driver with logic inputs, and is designed for use with magnetic memories.

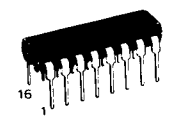
The device contains two 600-mA source-switch pairs and two 600-mA sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. With this arrangement selection of one of the four switches provides turn-on with minimum time skew of the output current rise.

- 600-mA Output Capability
- Fast Switching Times
- Input Clamp Diodes
- Dual Sink and Dual Source Outputs
- MDTL and MTTL Compatibility
- 24-Volt Output Capability

DUAL MEMORY DRIVER
SILICON MONOLITHIC INTEGRATED CIRCUIT

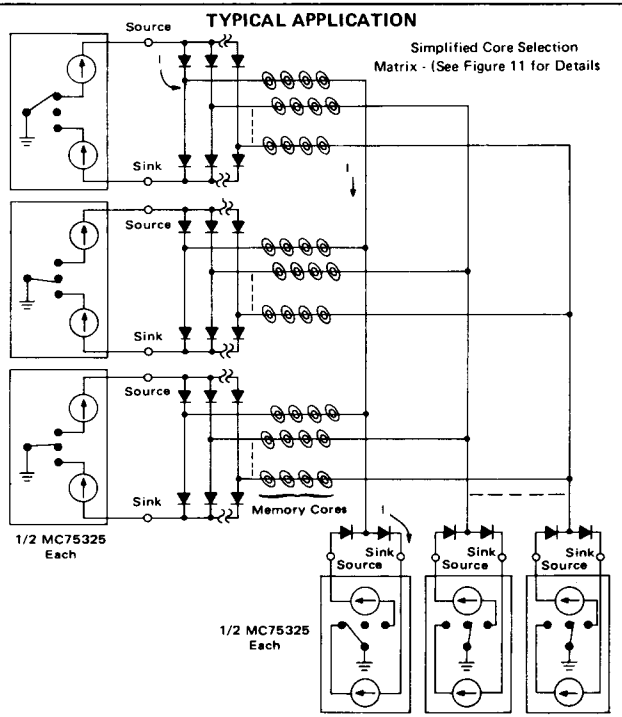


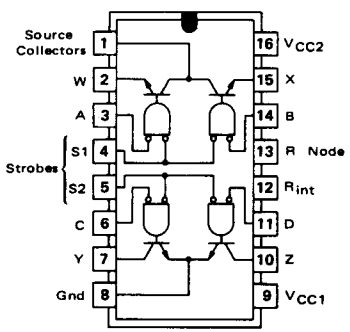
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC75325 only)

TYPICAL APPLICATION





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MAXIMUM RATINGS (T_A = 25° unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage (Note 1)	V_{CC1} V_{CC2}	7.0 25	Vdc Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation (Package Limitation) Ceramic and Plastic Packages Derate above T_A = +25°C	P_D	 1.0 6.6	 W mW/°C
Operating Ambient Temperature Range MC55325 MC75325	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. Voltage values are with respect to the network ground terminal.

TRUTH TABLE

ADDRESS INPUTS		STROBE INPUTS		STROBE INPUTS		OUTPUTS		OUTPUTS	
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	On	Off	Off	Off
H	L	X	X	L	H	Off	On	Off	Off
X	X	L	H	H	L	Off	Off	On	Off
X	X	H	L	H	L	Off	Off	Off	On
X	X	X	X	H	H	Off	Off	Off	Off
H	H	H	H	X	X	Off	Off	Off	Off

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

ELECTRICAL CHARACTERISTICS ($T_A = T_{low}$ to T_{high} unless otherwise noted(1))

Characteristic	Symbol	MC55325 Min	MC55325 Typ(2)	MC55325 Max	MC75325 Min	MC75325 Typ(2)	MC75325 Max	Unit
Input Voltage – High Logic State	V_{IH}	2.0	–	–	2.0	–	–	V
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	–	–	0.8	V
Input Clamp Voltage (V_{CC1} = 4.5 V, V_{CC2} = 24 V, I_I = -10 mA, T_A = 25°C)	V_I	–	-1.3	-1.7	–	-1.3	-1.7	V
Output Current – Off State (V_{CC1} = 4.5 V, V_{CC2} = 24 V) $T_A = T_{low}$ to T_{high}	I_{off}	–	–	500	–	–	200	μA
T_A = 25°C		–	3.0	150	–	3.0	200	
Output Voltage – High Logic State (V_{CC1} = 4.5 V, V_{CC2} = 24 V, I_O = 0)	V_{OH}	19	23	–	19	23	–	V
Saturation Voltage(3)	V_{sat}							V
Source Outputs (V_{CC1} = 4.5 V, V_{CC2} = 15 V, I_{source} ≈ -600 mA, R_L = 24 ohms, Note 4) $T_A = T_{low}$ to T_{high}		–	–	0.9	–	–	0.9	
T_A = 25°C		–	0.43	0.7	–	0.43	0.75	
Sink Outputs (V_{CC1} = 4.5 V, V_{CC2} = 15 V, I_{sink} ≈ 600 mA, R_L = 24 ohms, Note 4) $T_A = T_{low}$ to T_{high}		–	–	0.9	–	–	0.9	
T_A = 25°C		–	0.43	0.7	–	0.43	0.75	
Input Current at Maximum Input Voltage (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 5.5 V)	I_I							mA
Address Inputs		–	–	1.0	–	–	1.0	
Strobe Inputs		–	–	2.0	–	–	2.0	
Input Current – High Logic State (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 2.4 V)	I_{IH}							μA
Address Inputs		–	3.0	40	–	3.0	40	
Strobe Inputs		–	6.0	80	–	6.0	80	
Input Current – Low Logic State (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 0.4 V)	I_{IL}							mA
Address Inputs		–	-1.0	-1.6	–	-1.0	-1.6	
Strobe Inputs		–	-2.0	-3.2	–	-2.0	-3.2	
Supply Current – Output Condition Off (V_{CC1} = 5.5 V, V_{CC2} = 24 V, T_A = 25°C)	$I_{CC(off)}$							mA
From V_{CC1}		–	14	22	–	14	22	
From V_{CC2}		–	7.5	20	–	7.5	20	
Supply Current from V_{CC1}, Either Sink "On" (V_{CC1} = 5.5 V, V_{CC2} = 24 V, I_{sink} = 50 mA, T_A = 25°C)	I_{CC1}	–	55	70	–	55	70	mA
Supply Current from V_{CC2}, Either Source "On" (V_{CC1} = 5.5 V, V_{CC2} = 24 V, I_{source} = -50 mA, T_A = 25°C)	I_{CC2}	–	32	50	–	32	50	mA

(1) T_{low} = -55°C for MC55325, 0°C for MC75325
T_{high} = +125°C for MC55325, +70°C for MC75325

(2) All typical values are at T_A = 25°C

(3) Not more than one output is to be "on" at any one time.

(4) Saturation voltage must be measured using pulse techniques: Pulse Width = 200 μs, Duty Cycle ≤ 2%

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SWITCHING CHARACTERISTICS (V_{CC1} = 5.0 V, C_L = 25 pF, T_A = 25°C)

Characteristics		Symbol	MC55325/MC75325 Min	Typ	Max	Unit
Propagation Delay Time to Source Collectors						
(V_{CC2} = 15 V, R_L = 24 ohms)	Low-to-High Level	t_{PLH}	–	25	50	ns
	High-to-Low Level	t_{PHL}	–	25	50	ns
Transition Time						
(V_{CC2} = 20 V, R_L = 1 k ohms)	Low-to-High Level	t_{TLH}	–	55	–	ns
	High-to-Low Level	t_{THL}	–	7.0	–	ns
Propagation Delay Time to Sink Outputs						
(V_{CC2} = 15 V, R_L = 24 ohms)	Low-to-High Level	t_{PLH}	–	20	45	ns
	High-to-Low Level	t_{PHL}	–	20	45	ns
Transition Time						
(V_{CC2} = 15 V, R_L = 24 ohms)	Low-to-High Level Output	t_{TLH}	–	7.0	15	ns
	High-to-Low Level Output	t_{THL}	–	9.0	20	ns
Storage Time to Sink Outputs (V_{CC2} = 15 V, R_L = 24 ohms)		t_s	–	15	30	ns

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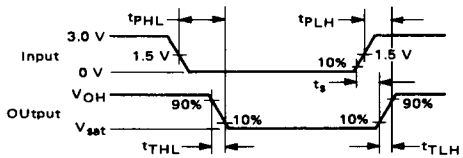
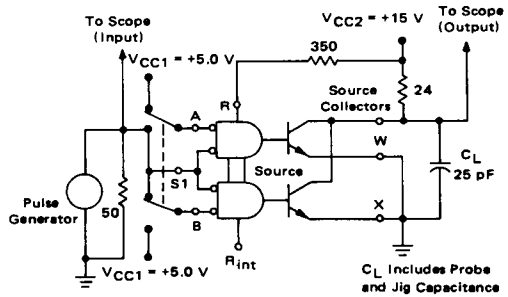
FIGURE 1 – SWITCHING TIMES TO SOURCE COLLECTORS AND SINK OUTPUTS



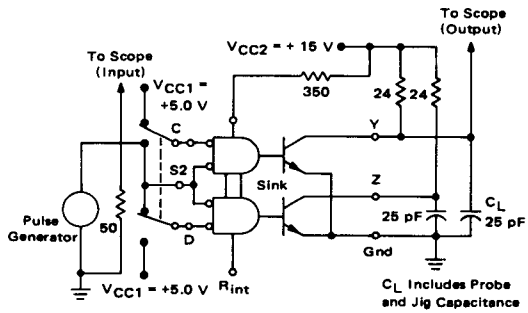
Input Pulse Characteristics:
z_o = 50Ω, Pulse Width = 200 ns,
$t_{TLH} = t_{THL} \leq 10$ ns, Duty Cycle ≤ 1%

FIGURE 2 – PROPAGATION TIME TO SOURCE COLLECTORS



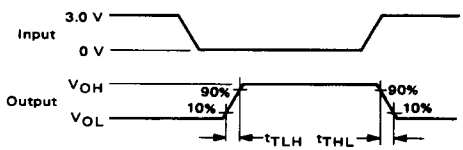
Source W Shown Under Test

FIGURE 3 – PROPAGATION TIME, TRANSITION TIME AND STORAGE TIME TO SINK OUTPUTS



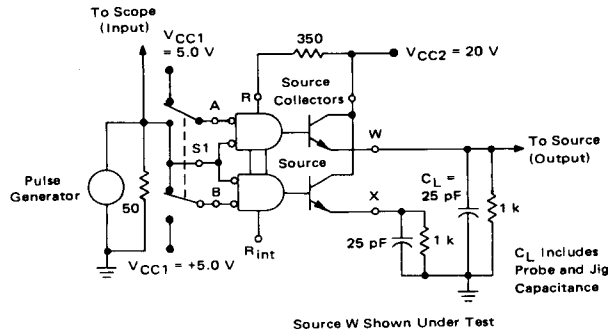
Sink Y Shown Under Test

FIGURE 4 – SWITCHING TIMES ON SOURCE OUTPUTS (See Figure 5)



Input Pulse Characteristics:
$t_{THL} = t_{TLH} \leq 10$ ns, Duty Cycle ≤ 1%
Pulse Width = 200 ns

FIGURE 5 – TRANSITION TIME ON SOURCE OUTPUTS



TYPICAL PERFORMANCE CURVES

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FIGURE 6 – SOURCE COLLECTOR CURRENT (Off-State) versus AMBIENT TEMPERATURE

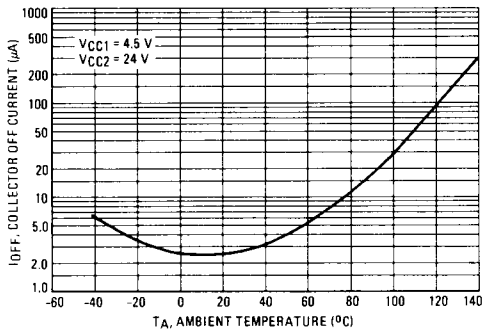


FIGURE 7 – SINK OUTPUT VOLTAGE-HIGH STATE V_{OH} versus AMBIENT TEMPERATURE

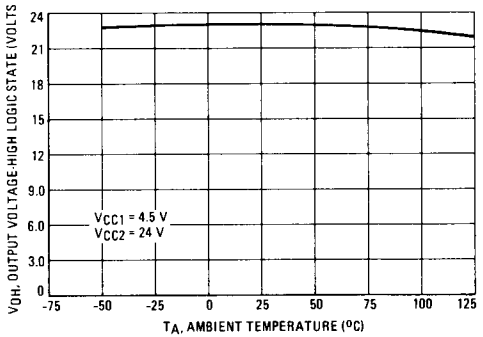


FIGURE 8 – SOURCE OR SINK SATURATION VOLTAGE versus AMBIENT TEMPERATURE

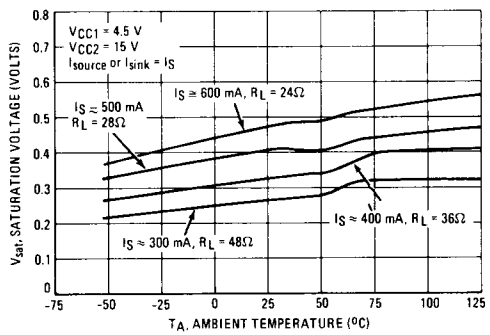
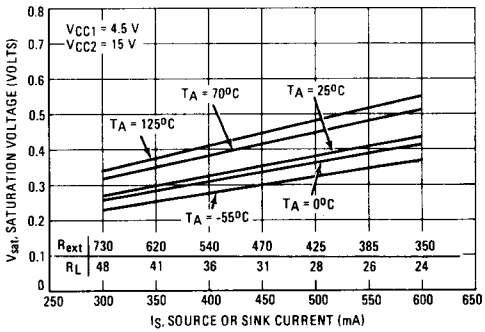


FIGURE 9 – SOURCE OR SINK SATURATION VOLTAGE versus SOURCE OR SINK CURRENT



APPLICATIONS INFORMATION

BASE DRIVE RESISTOR

An internal 575 Ω resistor connected between the V_{CC2} and the R_{int} terminals is provided in the MC55325/75325 to supply sufficient base drive for source currents to 375 mA at V_{CC2} of 15 Volts or 600 mA at V_{CC2} of 24 Volts. Connecting the R node to the R_{int} node selects this internal resistor. If source currents greater than 375 mA are required, the R_{int} node should be left open and an appropriate resistor connected between V_{CC2} and the R node. This method allows source base drive currents regulated to typically within ± 5%. This has an added advantage of removing the power dissipated in the resistor from the IC package, allowing the device to source greater currents at a given junction temperature.

The value of the required external resistor in a particular memory application may be computed using the following equation:

$$R_{ext} = \frac{16\ (V_{CC2\ min} - V_S - 2.2)}{I_L \cdot 1.6\ (V_{CC2\ min} - V_S - 2.9)} \qquad (1)$$

Where: R_{ext} = kΩ.
V_S = the source output voltage referred to ground.
I_L = mA.

During the load current pulse the power dissipated in the resistor, R_{ext} is

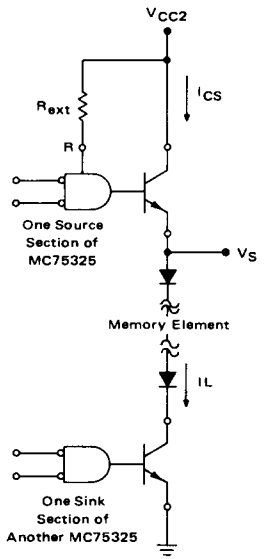
$$P_{R_{ext}} \approx \frac{I_L\ (V_{CC2\ min} - V_S - 2)}{16} \qquad (2)$$

Where: $P_{R_{ext}}$ = mW.

The source collector current I_{CS} is approximately 94% of total load current, I_L. The remaining current flows in the base of the source transistor through the external resistor R_{ext} or the source gate. See Figure 10 for added details.

An internal pull-up resistor in parallel with a clamping diode to V_{CC2} is provided at each sind-output collector to protect against voltage surges generated by switching reduction loads.

FIGURE 10 – TYPICAL CIRCUIT USED FOR R_{ext} CALCULATION



SELECTION MATRIX

The combination of current source and sink pairs within the MC75325 is often utilized to implement a selection matrix for core memory systems. A typical, simplified system is shown in Figure 11.

The selection of any particular line (line 7, for example) is made by activating a particular, unique combination of two source/sink pairs. For an example, with the Mode Select input high and $\overline{B1}$ low, current source X of #1 MC75325 will be activated. This selects lines 4-7. When input C4 goes low, on #4 MC75325, current will flow through line 7 from source X (of device #1) to sink Y of device #4.

Changing the logic state of device #1 to input $\overline{D1}$ low, device #4 to input $\overline{A4}$ low, and applying a low to the Mode Select input, reverses the direction of the current in line 7 with the #1 MC75325 sinking the current and the #4 device sourcing it.

Drive line inductance and capacitance only limits the number of drive lines a source/sink pair can drive and thus the size of a matrix possible.

FIGURE 11 – TYPICAL
APPLICATION - CORE MEMORY
SELECTION MATRIX