

CD4000-Series Ratings and Classifications

Absolute Maximum Ratings

| | |
|---|--|
| DC Supply Voltage Range, (V _{DD}) | -0.5V to +20V (Voltage Referenced to V _{SS} Terminals) |
| Input Voltage Range, All Inputs | -0.5V to V _{DD} +0.5V |
| DC Input Current, Any One Input | ±10mA |
| Operating Temperature Range (T _A) | -55°C to +125°C Package Types D, F, K, H |
| Storage Temperature Range (T _{STG}) | -65°C to +150°C |
| Lead Temperature (During Soldering) | +265°C At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum |

Reliability Information

| | | |
|---|-------------------------------|---------------|
| Thermal Resistance | θ_{ja} | θ_{jc} |
| Ceramic DIP Package | 28°C/W | TBD°C/W |
| Flatpack Package | 22°C/W | TBD°C/W |
| Maximum Package Power Dissipation (P _D) at +125°C | | |
| For T _A = -55°C to +100°C (Package Types D, F, K) | 500W | |
| For T _A = +100°C to +125°C (Package Types D, F, K) | Derate | |
| | Linearity at 12mW/°C to 200mW | |
| Device Dissipation Per Output Transistor | 100mW | |
| For T _A = Full Package Temperature Range (All Package Types) | | |
| Junction Temperature | +175°C | |

Recommended Operating Conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| | |
|---|-----------------|
| Supply Voltage Range | 3V Min, 18V Max |
| (For T _A = Full Package Temperature Range) | |

Device Classification for Leakage Current

The table below classifies the levels of device leakage as SSI, MSI-1 and MSI-2. In order to determine the limits which apply to a specific device type, consult the standard DC electrical characteristics chart.

CLASSIFICATION ACCORDING TO CIRCUIT COMPLEXITY

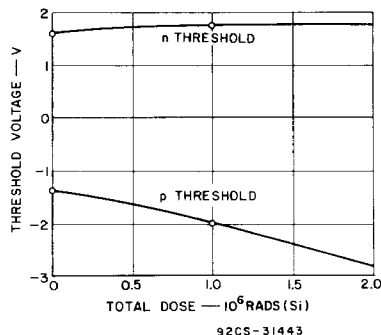
| GATES/ INVERTERS (SSI) | BUFFERS/FLIP-FLOPS/ LATCHES/MULTILEVEL GATES (MSI-1) | | COMPLEX LOGIC (MSI-2) | | |
|---------------------------|--|-----------|-----------------------|----------|-----------|
| CD4000B | CD4009UB* | CD4085B | CD4006B | CD4060B | CD4556B |
| CD4001B | CD4010B | CD4086B | CD4008B | CD4063B | CD4585B |
| CD4002B | CD4013B | CD4093B* | CD4014B | CD4067B* | CD4724B |
| CD4007UB | CD4019B | CD4095B | CD4015B | CD4076B | CD14538B |
| CD4011B | CD4027B | CD4096B | CD4017B | CD4089B | CD40100B |
| CD4012B | CD4030B | CD4098B | CD4018B | CD4094B | CD40101B |
| CD4016B* | CD4041UB* | CD4502B* | CD4020B | CD4097B* | CD40102B |
| CD4023B | CD4042B | CD4503B* | CD4021B | CD4099B | CD40103B |
| CD4025B | CD4043B | CD40106B* | CD4022B | CD4508B | CD40104B |
| CD4048B | CD4044B | CD40107B* | CD4024B | CD4510B | CD40105B |
| CD4066B* | CD4047B | CD40109B* | CD4026B | CD4511B* | CD40108B |
| CD4068B | CD4049UB* | CD40147B | CD4028B | CD4512B | CD40110B* |
| CD4069UB | CD4050B | CD40174B | CD4029B | CD4514B | CD40160B |
| CD4071B | CD4070B | CD40175B | CD4031B* | CD4515B | CD40161B |
| CD4072B | CD4077B | CD40257B | CD4033B | CD4516B | CD40162B |
| CD4073B | | | CD4034B | CD4517B | CD40163B |
| CD4075B | | | CD4035B | CD4518B | CD40181B |
| CD4078B | | | CD4040B | CD4520B | CD40182B |
| CD4081B | | | CD4046B* | CD4527B | CD40192B |
| CD4082B | | | CD4051B* | CD4532B | CD40193B |
| | | | CD4052B* | CD4536B | CD40194B |
| | | | CD4053B* | CD4555B | CD40208B |

* Indicates type for which, because of design requirements, one or more static characteristics differ from the standardized data. These differences are defined in separate DC Electrical Characteristics charts.

Radiation Resistant CD4000-Series

Harris radiation hardened CD4000-series CMOS integrated circuits tested to withstand total ionizing radiation dosages of 1×10^5 rads (Si) — R-suffix types, and 1×10^6 rads (Si) — H-suffix types. These radiation tolerances are achieved by special process controls imposed during wafer fabrication.

Harris radiation hardened types may be screened to Mil-M-38510 Class S and to level /MS. The specified levels of radiation resistance are verified per Table V group E subgroup 2 of Method 5005 and tested according to Method 1019 of Mil-Std-883. Four electrically good packaged samples from each wafer, one from each quadrant, are exposed in a Cobalt 60 source for a time period corresponding to the specified total dose. The samples are then electrically tested within one hour after exposure for threshold voltage, threshold voltage delta, I_{DD} leakage current, and functionality. Propagation delay is also measured for 38510 tested product.



TYPICAL THRESHOLD VOLTAGE VARIATIONS OF HARRIS MEGARAD CD4000-SERIES CMOS INTEGRATED CIRCUITS AS A FUNCTION OF TOTAL DOSE GAMMA RADIATION

RADIATION RESISTANT CD4000-SERIES CMOS ICs

Post Radiation Test Criteria — Maximum Limits for I_{DD} , ($V_{DD} = 18V$ for B-Series Types or $15V$ for A-Series Types)

| TYPE | I_{DD} (MAX) μA | TYPE | I_{DD} (MAX) μA | TYPE | I_{DD} (MAX) μA | TYPE | I_{DD} (MAX) μA |
|--------|------------------------|--------|------------------------|--------|------------------------|----------|------------------------|
| CD4000 | 2.5 | CD4040 | 25 | CD4078 | 2.5 | CD4555 | 25 |
| CD4001 | 2.5 | CD4041 | 7.5 | CD4081 | 2.5 | CD4556 | 25 |
| CD4002 | 2.5 | CD4042 | 7.5 | CD4082 | 2.5 | CD4585 | 25 |
| CD4006 | 25 | CD4043 | 7.5 | CD4085 | 2.5 | CD4724 | 25 |
| CD4007 | 2.5 | CD4044 | 7.5 | CD4086 | 2.5 | CD40100 | 25 |
| CD4008 | 25 | CD4046 | 25 | CD4089 | 25 | CD40101 | 25 |
| CD4009 | 7.5 | CD4047 | 25 | CD4093 | 7.5 | CD40102 | 25 |
| CD4010 | 7.5 | CD4048 | 7.5 | CD4094 | 25 | CD40103 | 25 |
| CD4011 | 2.5 | CD4049 | 7.5 | CD4095 | 7.5 | CD40104 | 25 |
| CD4012 | 2.5 | CD4050 | 7.5 | CD4096 | 7.5 | CD40105 | 25 |
| CD4013 | 7.5 | CD4051 | 25 | CD4097 | 25 | CD40106 | 7.5 |
| CD4014 | 25 | CD4052 | 25 | CD4098 | 7.5 | CD40107 | 7.5 |
| CD4015 | 25 | CD4053 | 25 | CD4099 | 25 | CD40108 | 25 |
| CD4016 | 2.5 | CD4060 | 25 | CD4502 | 7.5 | CD40109* | 7.5 |
| CD4017 | 25 | CD4063 | 25 | CD4503 | 7.5 | CD40147 | 25 |
| CD4018 | 25 | CD4066 | 2.5 | CD4504 | 7.5 | CD40160 | 25 |
| CD4019 | 7.5 | CD4067 | 25 | CD4508 | 25 | CD40161 | 25 |
| CD4020 | 25 | CD4068 | 7.5 | CD4510 | 25 | CD40162 | 25 |
| CD4021 | 25 | CD4069 | 2.5 | CD4511 | 25 | CD40163 | 25 |
| CD4022 | 25 | CD4070 | 2.5 | CD4512 | 25 | CD40174 | 7.5 |
| CD4023 | 2.5 | CD4071 | 2.5 | CD4514 | 25 | CD40175 | 7.5 |
| CD4024 | 25 | CD4072 | 2.5 | CD4515 | 25 | CD40181 | 25 |
| CD4025 | 2.5 | CD4073 | 2.5 | CD4516 | 25 | CD40182 | 25 |
| CD4026 | 25 | CD4075 | 2.5 | CD4517 | 25 | CD40192 | 25 |
| CD4027 | 7.5 | CD4076 | 25 | CD4518 | 25 | CD40193 | 25 |
| CD4028 | 25 | CD4077 | 2.5 | CD4520 | 25 | CD40194 | 25 |
| CD4029 | 25 | | | CD4527 | 25 | CD40208 | 25 |
| CD4030 | 7.5 | | | CD4532 | 25 | CD40257 | 7.5 |
| CD4031 | 25 | | | CD4536 | 25 | | |
| CD4033 | 25 | | | | | | |
| CD4034 | 25 | | | | | | |
| CD4035 | 25 | | | | | | |

Post Radiation Threshold Voltage Test Criteria ($V_{DD} = 10V$; $I = \text{Constant } 10\mu A$)

N Threshold = 0.2V min

*P Threshold = 3.5V max CD40109 and 40106

P Threshold = 2.8V max

ΔP Threshold = 1.0V max

ΔN Threshold = 1.0V max

Radiation Hardened High Reliability ICs

Radiation Hardness Assurance Testing

CD4000-Series Total Dose Testing Procedures

- **Class S Wafer Sampling**
 - ▶ Test Four Samples (High-Rel Visual Rejects)
 - ▶ One From Each Quadrant of Wafer
 - ▶ Reject If Any One Sample Fails
- **Class B Inspection Lot Sampling**
 - ▶ LT PD = 20, 11/0
18/1

CD4000-SERIES POST RADIATION TESTS

| SYMBOL | CHARACTERISTIC | JAN LIMIT | NONJAN LIMIT | VOLTAGE |
|--|-------------------------|-----------------------------|---------------|---------|
| V _{TN} | N Threshold Voltage | 0.3V Min | 0.2V Min | 10V |
| V _{TP} | P Threshold Voltage | 2.8V Max | 2.8V Max | 10V |
| ΔV _T | Delta Threshold Voltage | 1.4V Max | 1.0V Max | 10V |
| I _{SS} | Quiescent Current | 100 x Max | 100 x Max | 18V |
| | CD4000B-Series | Pre-Rad Value | Pre-Rad Value | |
| T _{PLH} , T _{PHL} | Propagation Delay | 1.35 x Max Pre-Rad Value | | 5V* |

* Worst case test condition

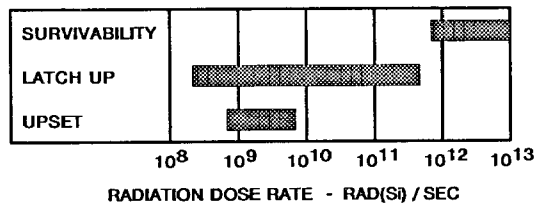
Radiation Resistant CD4000 Series

SCREENING LEVELS FOR HARRIS HIGH RELIABILITY RADIATION RESISTANT CD4000-SERIES CMOS ICs

| SCREENING LEVELS | APPLICATION | DESCRIPTION |
|---|---------------------------|---|
| PACKAGED DEVICES (D, F, K OR J SUFFIX) | | |
| /MSR /MSH | Aerospace and Missiles | For devices intended for use where maintenance and replacement are difficult and reliability is imperative |
| CHIPS (H SUFFIX) | | |
| /SR /SH | Aerospace and Missiles | For hybrid applications where maintenance and replacement are extremely difficult and reliability is imperative |

CD4000-Series CMOS ICs Transient Radiation Resistance

Samples of CD4000-series devices representing all levels of circuit complexity have been characterized for transient radiation effects. The data indicate the ranges of occurrence of upset, latchup and survivability as a function of radiation dose rate.



EFFECTS OF TRANSIENT RADIATION (10^6 RADS (Si) ON
CD4000-SERIES INTEGRATED CIRCUITS
(ALUMINUM GATE CMOS ON BULK SILICON)

Latchup

Latchup occurs because of the presence of inherent bipolar SCR structures in bulk CMOS devices. In normal operation, the parasitic bipolar SCR remains inactive. The device is said to be in the latchup state when the parasitic SCR structures become activated, thereby creating a low impedance path from V_{DD} to V_{SS} . In the "ON" condition, the SCR can conduct heavily at low voltages. Latchup may be induced by the resultant photocurrents of high intensity transient ionizing radiation or by applying excessive voltage. Once turned on, the SCR can be rendered dormant again only by removing the power supply. Burn-out of the device may result if the current is not limited in some way.

The region of occurrence of the latch condition in CMOS ICs under high intensity transient radiation is quite wide. Only two known device types latch below the 1×10^9 RAD (Si)/s level. A significant number of device types do not latch above dose rates of 1×10^{11} RADs (Si)/s.

Latchup Protection

Latchup protection in bulk CMOS devices can be achieved by taking advantage of the effects of neutron irradiation. Neutron irradiation will reduce minority-carrier lifetime, which, in turn attenuates the current gains, or betas, of bipolar transistors. To turn on the SCR structure of CMOS devices, it is necessary for the beta product of its bipolar transistors are majority-carrier devices, normal CMOS performance is generally unaffected by neutron irradiation. Therefore, neutron irradiation is a suitable method for precluding latchup in CMOS devices. In addition, neutron-irradiated CMOS devices are less susceptible to logic upset due to transient radiation.

Neutron-Irradiated CMOS

Harris offers custom CD4000-series devices which are made from wafers that are exposed to a neutron fluence of approximately 1×10^{14} n/cm². After neutron irradiation, wafers can be assembled and screened to all requirements of the Harris level product.

Survivability

Survivability level is the maximum transient-radiation level at which damage does not occur. Above this level photocurrents are created to the extent that excessive dissipation is caused, resulting in permanent damage to the device.

Standard DC Electrical Characteristics

Standard "B" Series Devices

The following table contains electrical characteristics for devices. These parameters are 100% tested except where indicated.

| Static Electrical Parameters | Conditions | | | Limits at Indicated Temperatures | | | | | | Units | Notes |
|---|----------------|-----------------|-----------------|----------------------------------|-------|-------|-------|--------|-------|-------|-------|
| | | | | -55°C | | +25°C | | +125°C | | | |
| | V _O | V _{IN} | V _{DD} | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Functional Test* | — | — | — | — | — | — | — | — | — | | 4 |
| Quiescent device current I _{DD} | — | 0,5 | 5 | — | 0.25* | — | 0.25* | — | 7.5* | μA | 1 |
| SSI Types | — | 0,10 | 10 | — | 0.5* | — | 0.5* | — | 15* | | |
| See Classification Chart | — | 0,15 | 15 | — | 1* | — | 1* | — | 30* | | |
| MSI-1 | — | 0,5 | 5 | — | 1* | — | 1* | — | 30* | μA | 1, 2 |
| See Classification Chart | — | 0,10 | 10 | — | 2* | — | 2* | — | 60* | | |
| | — | 0,15 | 15 | — | 4* | — | 4* | — | 120* | | |
| | — | 0,20 | 20 | — | 20* | — | 20* | — | 600* | | |
| MSI-2 | — | 0,5 | 5 | — | 5* | — | 5* | — | 150* | μA | 1 |
| See Classification Chart | — | 0,10 | 10 | — | 10* | — | 10* | — | 300* | | |
| | — | 0,15 | 15 | — | 20* | — | 20* | — | 600* | | |
| | — | 0,20 | 20 | — | 100* | — | 100* | — | 3000* | | |
| Output low drive current I _{OL} min. | 0.4 | 0,5 | 5 | 0.64* | — | 0.51 | — | 0.36* | — | mA | |
| | 0.5 | 0,10 | 10 | 1.6* | — | 1.3 | — | 0.9* | — | | |
| | 1.5 | 0,15 | 15 | 4.2* | — | 3.4 | — | 2.4* | — | | |
| Output high drive current I _{OH} min. | 4.6 | 0,5 | 5 | -0.64 | — | -0.51 | — | -0.36* | — | mA | |
| | 2.5 | 0,5 | 5 | -2.0 | — | -1.6 | — | -1.15* | — | | |
| | 9.5 | 0,10 | 10 | -1.6 | — | -1.3 | — | -0.9* | — | | |
| | 13.5 | 0,15 | 15 | -4.2 | — | -3.4 | — | -2.4* | — | | |
| Output voltage low-level V _{OL} max. | — | 0,5 | 5 | — | 0.05* | — | 0.05* | — | 0.05* | V | |
| | — | 0,10 | 10 | — | 0.05* | — | 0.05* | — | 0.05* | | |
| Output voltage high-level V _{OH} min. | — | 0,5 | 5 | 4.95* | — | 4.95* | — | 4.95 | — | V | |
| | — | 0,10 | 10 | 9.95* | — | 9.95* | — | 9.95 | — | | |
| | — | 0,15 | 15 | 14.95 | — | 14.95 | — | 14.95 | — | | |
| Input low voltage V _{IL} max. | 4.5 | — | 5 | — | 1.5 | — | 1.5 | — | 1.5 | V | |
| Buffered (B) | 9 | — | 10 | — | 3* | — | 3 | — | 3 | | |
| | 13.5 | — | 15 | — | 4 | — | 4 | — | 4 | | |
| Unbuffered (UB) | 4.5 | — | 5 | — | 1* | — | 1 | — | 1 | V | |
| | 9 | — | 10 | — | 2 | — | 2 | — | 2 | | |
| | 13.5 | — | 15 | — | 2.5 | — | 2.5 | — | 2.5 | | |
| Input high voltage V _{IH} min. | 0.5, 4.5 | — | 5 | 3.5 | — | 3.5 | — | 3.5 | — | V | |
| Buffered (B) | 1, 9 | — | 10 | 7 | — | 7 | — | 7 | — | | |
| | 1.5, 13.5 | — | 15 | 11 | — | 11 | — | 11 | — | | |
| Unbuffered (UB) | 0.5, 4.5 | — | 5 | 4 | — | 4 | — | 4 | — | V | |
| | 1, 9 | — | 10 | 8 | — | 8 | — | 8 | — | | |
| | 1.5, 13.5 | — | 15 | 12.5 | — | 12.5 | — | 12.5 | — | | |
| Input current I _{IN} | — | 0,20 | 20 | — | ± 0.1 | — | ± 0.1 | — | ± 1 | μA | 1 |
| 3-state output leakage current I _{OUT} | 0,20 | 0,20 | 20 | — | ± 0.4 | — | ± 0.4 | — | ± 12 | μA | 1, 3 |

* These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

NOTES:

- At -55°C test is performed with V_{DD} of 18V.
- CD4047B - Maximum DC supply voltage V_{DD} is 13V for radiation hardened version of this type when operating with RC network.
- For applicable devices only.
- At 25°C V_{IN} = 0 - 20V, V_{DD} = 20V; 125°C V_{IN} = 0 - 18V, V_{DD} = 18V; and at -55°C V_{IN} = 0 - 3V, V_{DD} = 3V.

Non-Standard DC Electrical Characteristics

Non-Standard "B" Series Devices

The table below indicates all devices which are considered to be non-standard. Non-standard devices are types such as bilateral switches (CD4066B), multiplexers (CD4051B), special sink or source currents (CD4049UB, CD4050B), and open drain buffer/drivers (CD40107B) which exhibit non-standard outputs or special parameters. This table shows the

100% electrical tests that are performed on these specialized devices. These tests take the place of corresponding parameters in the Standard Electrical Characteristics table. For the types listed with R_{ON} tests, drive current and output voltage tests should be deleted from the Standard Electrical Characteristics table.

| Static Electrical Parameters | Conditions | | | Limits at Indicated Temperatures | | | | Units |
|---|--------------------------------|----------|----------|----------------------------------|-------|------|-----------|-------|
| | | | | -55°C | +25°C | | +125°C | |
| | V_O | V_{IN} | V_{DD} | Min./Max. | Min. | Max. | Min./Max. | |
| CD4009UB, CD4010B | | | | | | | | |
| Output low drive current I_{OL} min. | 0.4 | 0.5 | 4.5 | 3.2* | 2.6* | — | 1.8* | mA |
| | 0.4 | 0.5 | 5 | 3.75* | 3 | — | 2.1* | |
| | 0.5 | 0.10 | 10 | 10.0* | 8 | — | 5.6* | |
| | 1.5 | 0.15 | 15 | 30.0* | 24 | — | 16.0* | |
| Output high drive current I_{OH} min. | 4.6 | 0.5 | 5 | -0.25* | -0.2 | — | -0.15* | mA |
| | 2.5 | 0.5 | 5 | -1.0* | -0.8 | — | -0.58* | |
| | 9.5 | 0.10 | 10 | -0.55* | -0.45 | — | -0.33* | |
| | 13.5 | 0.15 | 15 | -1.65* | -1.5 | — | -1.1* | |
| CD4016B | | | | | | | | |
| Control Input voltage low V_{IL} max. | $V_{IS}=V_{SS}, V_{OS}=V_{DD}$ | | 5 | 0.9 | — | 0.7 | 0.4 | V |
| | $V_{IS}=V_{DD}, V_{OS}=V_{SS}$ | | 10 | 0.9* | — | 0.7 | 0.4* | |
| | $ I_{IS} < 10\mu A$ | | 15 | 0.9 | — | 0.7 | 0.4 | |
| Control Input voltage high V_{IH} min. | — | | 5 | 3.5 | 3.5 | — | 3.5 | V |
| | — | | 10 | 7.0* | 7.0* | — | 7.0* | |
| | — | | 15 | 11.0 | 11.0 | — | 11.0 | |
| On-state resistance R_{ON} max. $R_L = 10k$ returned to $V_{DD}-V_{SS}/2$ | $V_{IS}=V_{DD}$ or V_{SS} | | 10 | 600 | — | 660 | 960 | ohms |
| | $V_{IS}=4.75$ or 5.75 | | 10 | 1870 | — | 2000 | 2600 | |
| | $V_{IS}=V_{DD}$ or V_{SS} | | 15 | 360 | — | 400 | 600 | |
| | $V_{IS}=7.25$ or 7.75 | | 15 | 775 | — | 850 | 1230 | |
| CD4031B | | | | | | | | |
| Output low drive current I_{OL} min. Q | 0.4 | 0.5 | 5 | 2.56* | 2.04 | — | 1.44* | mA |
| | 0.5 | 0.10 | 10 | 6.4* | 5.2 | — | 3.6* | |
| | 1.5 | 0.15 | 15 | 16.8* | 13.6 | — | 9.6* | |
| \bar{Q}, Q', CLd | 0.4 | 0.5 | 5 | 0.64* | 0.51 | — | 0.36* | mA |
| | 0.5 | 0.10 | 10 | 1.6* | 1.3 | — | 0.9* | |
| | 1.5 | 0.15 | 15 | 4.2* | 3.4 | — | 2.4* | |
| Output high drive current I_{OH} min. Q, \bar{Q}, Q', CLd | 4.6 | 0.5 | 5 | -0.64* | -0.51 | — | -0.36* | mA |
| | 2.5 | 0.5 | 5 | -2.0* | -1.6 | — | -1.15* | |
| | 9.5 | 0.10 | 10 | -1.6* | -1.3 | — | -0.9* | |
| | 13.5 | 0.15 | 15 | -4.2* | -3.4 | — | -2.4* | |
| CD4041UB | | | | | | | | |
| Output low drive current I_{OL} min. | 0.4 | 0.5 | 5 | 2.1* | 1.6 | — | 1.2* | mA |
| | 0.5 | 0.10 | 10 | 6.25* | 5 | — | 3.5* | |
| | 1.5 | 0.15 | 15 | 24* | 19 | — | 13* | |
| Output high drive current I_{OH} min. | 4.6 | 0.5 | 5 | -2.1* | -1.6 | — | -1.2* | mA |
| | 2.5 | 0.5 | 5 | -8.4* | -6.4 | — | -4.6* | |
| | 9.5 | 0.10 | 10 | -6.25* | -5.0 | — | -3.5* | |
| | 13.5 | 0.15 | 15 | -24* | -19 | — | -13* | |

Limits with black dots (*) are tested 100%.

- These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

High Reliability CD4000B-Series CMOS ICs

Non-Standard DC Electrical Characteristics (Continued)

| Static Electrical Parameters | Conditions | | | Limits at Indicated Temperatures | | | | Units |
|--|--|--------------------|-----------------|----------------------------------|-------|--------|-----------|-------|
| | | | | -55°C | +25°C | | +125°C | |
| | V _O | V _{IN} | V _{DD} | Min./Max. | Min. | Max. | Min./Max. | |
| CD4046B | | | | | | | | |
| Zener diode voltage (V _Z) | I _Z = 50 μA | | | — | 4.45* | 6.5* | — | V |
| Quiescent leakage phase comparator pin 14 open pin 5 = V _{DD} | — | 0,5 | 5 | 0.2 | — | 0.2 | — | mA |
| | — | 0,10 | 10 | 1.0 | — | 1.0 | — | |
| | — | 0,15 | 15 | 1.5 | — | 1.5 | — | |
| | — | 0,20 | 20 | 4.0 | — | 4.0* | — | |
| Quiescent leakage phase comparator pin 14 = V _{SS} or V _{DD} pin 5 = V _{DD} | — | 0,5 | 5 | 20 | — | 20 | — | μA |
| | — | 0,10 | 10 | 40 | — | 40 | — | |
| | — | 0,15 | 15 | 80 | — | 80 | — | |
| | — | 0,20 | 20 | 160 | — | 160* | — | |
| CD4049UB, CD4050B | | | | | | | | |
| Output low drive current I _{OL} min. | 0.4 | 0,5 | 4.5 | 3.3 | 2.6* | — | 1.8 | mA |
| | 0.4 | 0,5 | 5 | 4.0 | 3.2* | — | 2.4 | |
| | 0.5 | 0,10 | 10 | 10 | 8.0* | — | 5.6 | |
| | 1.5 | 0,15 | 15 | 26 | 24* | — | 18 | |
| Output high drive current I _{OH} min. | 4.6 | 0,5 | 5 | -0.81 | -0.8* | — | -0.48 | mA |
| | 2.5 | 0,5 | 5 | -2.6 | -3.2* | — | -1.55 | |
| | 9.5 | 0,10 | 10 | -2.0 | -1.8* | — | -1.18 | |
| | 13.5 | 0,15 | 15 | -5.2 | -6.0* | — | -3.1 | |
| CD4051B, CD4052B, CD4053B, CD4067B, CD4097B | | | | | | | | |
| On-state resistance R _{ON} max. | R _L = 10k returned to V _{DD} -V _{SS} /2 | | 5 | 800 | — | 1050* | 1300* | ohms |
| | V _{IS} = V _{SS} to V _{DD} | | 10 | 310 | — | 400* | 500* | |
| | | | 15 | 200 | — | 240* | 320* | |
| Input voltage low V _{IL} max. | V _{EE} = V _{SS} | | 5 | 1.5* | — | 1.5* | 1.5* | Volts |
| | R _L = 1k to V _{SS} | | 10 | 3.0 | — | 3.0 | 3.0 | |
| | I _{IS} < 2 μA | | 15 | 4.0* | — | 4.0* | 4.0* | |
| Input voltage high V _{IH} min. | V _{EE} = V _{SS} | | 5 | 3.5* | 3.5* | — | 3.5* | Volts |
| | R _L = 1k to V _{SS} | | 10 | 7.0 | 7.0 | — | 7.0 | |
| | I _{IS} < 2 μA | | 15 | 11.0* | 11.0* | — | 11.0* | |
| Off channel leakage current Any channel off max. | V _{SS} -V | V _{EE} -V | 18 | ± 100* | — | ± 100* | ± 1000* | nA |
| | 0 | 0 | | | | | | |
| All channels (common out/in) off max. | | | | | | | | |

* These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

High Reliability CD4000B-Series CMOS ICs

Non-Standard DC Electrical Characteristics (Continued)

| Static Electrical Parameters | Conditions | | | Limits at Indicated Temperatures | | | | Units |
|---|--|-----------------|-----------------|----------------------------------|-------|-------|-----------|-------|
| | | | | -55°C | +25°C | | +125°C | |
| | V _O | V _{IN} | V _{DD} | Min./Max. | Min. | Max. | Min./Max. | |
| CD4066B | | | | | | | | |
| On-state resistance R _{ON} max. | R _L = 10k returned to V _{DD} -V _{SS} /2 V _{IS} = V _{SS} to V _{DD} | | 5 | 800* | — | 1050* | 1300* | ohms |
| | | | 10 | 310* | — | 400* | 550* | |
| | | | 15 | 200* | — | 240* | 320* | |
| Control Input Voltage Low V _{ILC} max. | V _{IS} = V _{SS} , V _{OS} = V _{DD} V _{IS} = V _{DD} , V _{OS} = V _{SS} I _{IS} < 10 μA | | 5 | 1.0* | — | 1.0* | 1.0* | Volts |
| | | | 10 | 2.0 | — | 2.0 | 2.0 | |
| | | | 15 | 2.0* | — | 2.0* | 2.0* | |
| Control Input Voltage High V _{IHC} min. | — | | 5 | 3.5* | 3.5* | — | 3.5* | Volts |
| | | | 10 | 7.0 | 7.0 | — | 7.0 | |
| | | | 15 | 11.0* | 11.0* | — | 11.0* | |
| Input output leakage current (switch off) Effective off resistance V _C = V _{SS} | 0 | 0 | 18 | ± 100 | — | ± 100 | ± 1000 | nA |
| CD4093B | | | | | | | | |
| Positive Trigger Threshold Voltage V _P min. | — | a | 5 | 2.2* | 2.2* | — | 2.2* | V |
| | — | a | 10 | 4.6 | 4.6 | — | 4.6 | |
| | — | a | 15 | 6.8* | 6.8* | — | 6.8* | |
| | — | b | 5 | 2.6* | 2.6* | — | 2.6* | |
| | — | b | 10 | 5.6 | 5.6 | — | 5.6 | |
| | — | b | 15 | 6.3 | 6.3 | — | 6.3 | |
| V _P max. | — | a | 5 | 3.6* | — | 3.6* | 3.6* | V |
| | — | a | 10 | 7.1 | — | 7.1 | 7.1 | |
| | — | a | 15 | 10.8* | — | 10.8* | 10.8* | |
| | — | b | 5 | 4* | — | 4* | 4* | |
| | — | b | 10 | 8.2 | — | 8.2 | 8.2 | |
| | — | b | 15 | 12.7 | — | 12.7 | 12.7 | |
| Negative Trigger Threshold Voltage V _N min. | — | a | 5 | 0.9* | 0.9* | — | 0.9* | V |
| | — | a | 10 | 2.5 | 2.5 | — | 2.5 | |
| | — | a | 15 | 4* | 4* | — | 4* | |
| | — | b | 5 | 1.4* | 1.4* | — | 1.4* | |
| | — | b | 10 | 3.4 | 3.4 | — | 3.4 | |
| | — | b | 15 | 4.8 | 4.8 | — | 4.8 | |
| V _N max. | — | a | 5 | 2.8* | — | 2.8* | 2.8* | V |
| | — | a | 10 | 5.2 | — | 5.2 | 5.2 | |
| | — | a | 15 | 7.4* | — | 7.4* | 7.4* | |
| | — | b | 5 | 3.2* | — | 3.2* | 3.2* | |
| | — | b | 10 | 6.6 | — | 6.6 | 6.6 | |
| | — | b | 15 | 9.6 | — | 9.6 | 9.6 | |
| Hysteresis Voltage V _H min. | — | a | 5 | 0.3* | 0.3* | — | 0.3* | V |
| | — | a | 10 | 1.2 | 1.2 | — | 1.2 | |
| | — | a | 15 | 1.6* | 1.6* | — | 1.6* | |
| | — | b | 5 | 0.3* | 0.3* | — | 0.3* | |
| | — | b | 10 | 1.2 | 1.2 | — | 1.2 | |
| | — | b | 15 | 1.6 | 1.6 | — | 1.6 | |
| V _H max. | — | a | 5 | 1.6 | — | 1.6* | 1.6* | V |
| | — | a | 10 | 3.4 | — | 3.4 | 3.4 | |
| | — | a | 15 | 5* | — | 5* | 5* | |
| | — | b | 5 | 1.6 | — | 1.6* | 1.6* | |
| | — | b | 10 | 3.4 | — | 3.4 | 3.4 | |
| | — | b | 15 | 5 | — | 5 | 5 | |

* Input on terminals 1, 5, 8, 12, or 2, 6, 9, 13; other inputs to V_{DD}.

^b Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.

* These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

High Reliability CD400B-Series CMOS ICs

Non-Standard DC Electrical Characteristics (Continued)

| Static Electrical Parameters | Conditions | | | Limits at Indicated Temperatures | | | | Units | | |
|--|---------------|----------|----------|----------------------------------|--------|-------|-----------|-------|------|---|
| | | | | -55°C | +25°C | | +125°C | | | |
| | V_O | V_{IN} | V_{DD} | Min./Max. | Min. | Max. | Min./Max. | | | |
| CD4502B | | | | | | | | | | |
| Output low drive current I_{OL} min. | 0.4 | 0,5 | 5 | 3.84 | 3.06* | — | 2.16 | mA | | |
| | 0.5 | 0,10 | 10 | 9.6 | 7.8* | — | 5.4 | | | |
| | 1.5 | 0,15 | 15 | 25.2 | 20.4* | — | 14.4 | | | |
| CD4503B | | | | | | | | | | |
| Output low drive current I_{OL} min. | 0.4 | 0 | 5 | 2.6 | 2.1* | — | 1.3 | mA | | |
| | 0.5 | 0 | 10 | 6.5 | 5.5* | — | 3.8 | | | |
| | 1.5 | 0 | 15 | 19.2 | 16.1* | — | 11.2 | | | |
| Output high drive current I_{OH} min. | 4.6 | 5 | 5 | -1.2 | -1.02* | — | -0.7 | mA | | |
| | 2.5 | 5 | 5 | -5.8 | -4.8* | — | -3.0 | | | |
| | 9.5 | 10 | 10 | -3.1 | -2.6* | — | -1.8 | | | |
| | 13.5 | 15 | 15 | -8.2 | -6.8* | — | -4.8 | | | |
| CD4504B | | | | | | | | | | |
| Input low voltage V_{IL} max. | TTL-CMOS | V_{CC} | — | 10 | 0.8 | — | 0.8 | 0.8 | V | |
| | TTL-CMOS | 5 | — | 15 | 0.8* | — | 0.8* | 0.8* | | |
| | CMOS-CMOS | 5 | — | 10 | 1.5* | — | 1.5* | 1.5* | | |
| | CMOS-CMOS | 5 | 1.5 | — | 15 | 1.5 | — | 1.5 | | |
| | CMOS-CMOS | 10 | 1.5 | — | 15 | 3* | — | 3* | | |
| Input high voltage V_{IH} min. | TTL-CMOS | 5 | 9 | — | 10 | 2 | — | 2 | | |
| | TTL-CMOS | 5 | 13.5 | — | 15 | 2* | — | 2* | | |
| | CMOS-CMOS | 5 | 9 | — | 10 | 3.5* | — | 3.5* | | |
| | CMOS-CMOS | 5 | 13.5 | — | 15 | 3.5 | — | 3.5 | | |
| | CMOS-CMOS | 10 | 13.5 | — | 15 | 7* | — | 7* | | |
| CD4511B | | | | | | | | | | |
| Output voltage high-level V_{OH} min. | — | 0, 5 | 5 | 4 | 4.1 | — | 4.2 | V | | |
| | — | 0, 10 | 10 | 9 | 9.1 | — | 9.2 | | | |
| | — | 0, 15 | 15 | 14* | 14.1* | — | 14.2* | | | |
| Output drive voltage high level V_{OH} min. | I_{OH} (mA) | 0 | — | — | 5 | 4.0 | 4.10 | — | 4.20 | V |
| | | 5 | — | — | 5 | — | — | — | — | |
| | | 10 | — | — | 5 | 3.80 | 3.90 | — | 3.90 | |
| | | 15 | — | — | 5 | — | — | — | 3.50 | |
| | | 20 | — | — | 5 | 3.55 | 3.40* | — | — | |
| | 25 | — | — | 5 | 3.40 | 3.10 | — | — | | |
| | 0 | — | — | 10 | 9.0 | 9.10 | — | 9.20 | V | |
| | 5 | — | — | 10 | — | — | — | — | | |
| | 10 | — | — | 10 | 8.85 | 9.0 | — | 9.0 | | |
| | 15 | — | — | 10 | — | — | — | — | | |
| | 20 | — | — | 10 | 8.70 | 8.60* | — | 8.40 | | |
| | 25 | — | — | 10 | 8.60 | 8.30 | — | — | | |
| | 0 | — | — | 15 | 14.0 | 14.10 | — | 14.20 | V | |
| | 5 | — | — | 15 | — | — | — | — | | |
| | 10 | — | — | 15 | 13.90 | 14.0 | — | 14.0 | | |
| 15 | — | — | 15 | — | — | — | — | | | |
| 20 | — | — | 15 | 13.75 | 13.70* | — | 13.50 | | | |
| 25 | — | — | 15 | 13.65 | 13.50 | — | — | | | |

* These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

Non-Standard DC Electrical Characteristics (Continued)

| Static Electrical Parameters | Conditions | | | Limits at Indicated Temperatures | | | | Units |
|---|----------------------------|----------------|-----------------|----------------------------------|-------|-------|-----------|-------|
| | | | | -55°C | +25°C | | +125°C | |
| | V _O | V _N | V _{DD} | Min./Max. | Min. | Max. | Min./Max. | |
| CD40106B | | | | | | | | |
| Positive trigger threshold voltage V _P min. | — | — | 5 | 2.2• | 2.2• | — | 2.2• | V |
| | — | — | 10 | 4.6• | 4.6• | — | 4.6• | |
| | — | — | 15 | 6.8• | 6.8• | — | 6.8• | |
| V _P max. | — | — | 5 | 3.6• | — | 3.6• | 3.6• | V |
| | — | — | 10 | 7.1• | — | 7.1• | 7.1• | |
| | — | — | 15 | 10.8• | — | 10.8• | 10.8• | |
| Negative trigger threshold voltage V _N min. | — | — | 5 | 0.9• | 0.9• | — | 0.9• | V |
| | — | — | 10 | 2.5• | — | 2.5• | 2.5• | |
| | — | — | 15 | 4• | — | 4• | 4• | |
| V _N max. | — | — | 5 | 2.8• | — | 2.8• | 2.8• | V |
| | — | — | 10 | 5.2• | — | 5.2• | 5.2• | |
| | — | — | 15 | 7.4• | — | 7.4• | 7.4• | |
| Hysteresis voltage V _H min. | — | — | 5 | 0.3• | 0.3• | — | 0.3• | V |
| | — | — | 10 | 1.2• | — | 1.2• | 1.2• | |
| | — | — | 15 | 1.6• | — | 1.6• | 1.6• | |
| V _H max. | — | — | 5 | 1.6• | — | 1.6• | 1.6• | V |
| | — | — | 10 | 3.4• | — | 3.4• | 3.4• | |
| | — | — | 15 | 5• | — | 5• | 5• | |
| CD40107B | | | | | | | | |
| Output low current I _{OL} min. | 0.4 | 0.5 | 5 | 21 | 16• | — | 12 | mA |
| | 1 | 0.5 | 5 | 44 | 34• | — | 25 | |
| | 0.5 | 0.10 | 10 | 49 | 37• | — | 28 | |
| | 1 | 0.10 | 10 | 89 | 68• | — | 51 | |
| | 0.5 | 0.15 | 15 | 66 | 50• | — | 38 | |
| Output high current I _{OH} min. | NO INTERNAL PULL-UP DEVICE | | | | | | | |
| Input low voltage V _{IL} max. * | 4.5 | — | 5 | 1.5• | — | 1.5• | 1.5• | V |
| | 9 | — | 10 | 3 | — | 3 | 3 | |
| | 13.5 | — | 15 | 4• | — | 4• | 4• | |
| Input high voltage V _{IH} min. * | 0.5, 4.5 | — | 5 | 3.5• | 3.5• | — | 3.5• | V |
| | 1.9 | — | 10 | 7 | 7 | — | 7 | |
| | 1.5, 13.5 | — | 15 | 11• | 11• | — | 11• | |

* Measured with external pull-up resistor, R_L = 10kΩ to V_{DD}

• These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

† At -55°C test is performed with V_{DD} of 18V

High Reliability CD4000B-Series CMOS ICs

Non-Standard DC Electrical Characteristics (Continued)

| Static Electrical Parameters | Conditions | | | Limits at Indicated Temperatures | | | | Units |
|--|------------------|-----------------|-----------------|----------------------------------|------------|------------|------------|-------|
| | | | | -55°C | +25°C | | +125°C | |
| | V _O | V _{CC} | V _{DD} | Min./Max. | Min. | Max. | Min./Max. | |
| CD40109B | | | | | | | | |
| Input low voltage V _{IL} max. | 1,9 1.5, 13.5 | 5 10 | 10 15 | 1.5• 3• | — — | 1.5• 3• | 1.5• 3• | V |
| Input high voltage V _{IH} max. | 1,9 1.5, 13.5 | 5 10 | 10 15 | 3.5• 7• | 3.5• 7• | — — | 3.5• 7• | V |
| CD40110B | | | | | | | | |
| Output Voltage Low-Level V _{OL} max. | I _{OH} | V _{OH} | V _{IN} | V _{DD} | | | | |
| | — | — | 0,5 | 5 | 0.05 | — | 0.05 | 0.05 |
| | — | — | 0,10 | 10 | 0.05 | — | 0.05 | 0.05 |
| High-Level V _{OH} min. | — | — | 0,5 | 5 | — | — | — | — |
| | — | — | 0,10 | 10 | — | — | — | — |
| | — | — | 0,15 | 15 | — | — | — | — |
| 7-Segment Outputs Output Drive Voltage, High V _{OH} min. | ■ | — | — | 5 | 3.9 | 3.9 | — | 4 |
| | -5 | — | — | 5 | 3.65 | 3.7 | — | 3.7 |
| | -10 | — | — | 5 | 3.55 | 3.65 | — | 3.65 |
| | -15 | — | — | 5 | 3.5 | 3.6 | — | 3.5 |
| | -20 | — | — | 5 | 3.45 | 3.45• | — | 3.35 |
| | -25 | — | — | 5 | 3.4 | 3.4 | — | 3.3 |
| | ■ | — | — | 10 | 8.75 | 8.75 | — | 8.85 |
| | -5 | — | — | 10 | 8.45 | 8.55 | — | 8.55 |
| | -10 | — | — | 10 | 8.42 | 8.5 | — | 8.5 |
| | -15 | — | — | 10 | 8.4 | 8.47 | — | 8.47 |
| | -20 | — | — | 10 | 8.4 | 8.45• | — | 8.40 |
| | -25 | — | — | 10 | 8.3 | 8.3 | — | 8.25 |
| | ■ | — | — | 15 | 13.8 | 13.8 | — | 13.9 |
| | -5 | — | — | 15 | 13.65 | 13.75 | — | 13.75 |
| | -10 | — | — | 15 | 13.6 | 13.72 | — | 13.72 |
| -15 | — | — | 15 | 13.6 | 13.7 | — | 13.7 | |
| -20 | — | — | 15 | 13.6 | 13.65• | — | 13.6 | |
| -25 | — | — | 15 | 13.3 | 13.3 | — | 13.25 | |
| 7-Segment Outputs Output Low (Sink) Current I _{OL} min. | — | 0,4 | 0,5 | 5 | 1.28 | 1• | — | 0.72 |
| | — | 0.5 | 0,10 | 10 | 3.2 | 2.6• | — | 1.8 |
| | — | 1.5 | 0,15 | 15 | 8.4 | 6.8• | — | 4.8 |

• These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

■ 0 (10μA)

High Reliability CD400B-Series CMOS ICs

Switching Characteristics at 25°C

The chart below lists all Harris high reliability CD400B-series devices and shows which switching parameters are 100% tested at final electrical and Group A. In general, Harris tests propagation delay, transition time, and maximum clock frequency at 5V where applicable.

Harris warrants all other switching parameters shown in the appropriate commercial data sheet. Harris high reliability switching tests are performed on a one-input to one-output basis only.

| TYPE | CONDITIONS* V _{DD} = 5V, C _L = 50pF | PROP DELAY (ns) | TRANS. TIME (ns) | MAX CLOCK INPUT FREQ. (MHz) |
|----------|--|-----------------|------------------|-----------------------------|
| CD4000B | - | 250 | 200 | - |
| CD4001B | - | 250 | 200 | - |
| CD4002B | - | 250 | 200 | - |
| CD4006B | - | 400 | 200 | 2.5 |
| CD4007UB | - | 110 | 200 | - |
| CD4008B | Sum In to Sum Out | 800 | 200 | - |
| | Carry In to Sum Out | 740 | - | - |
| | Sum In to Carry Out | 400 | - | - |
| | Carry In to Carry Out | 200 | - | - |
| CD4009UB | - | 140* | 350* | - |
| | - | 60▲ | 70▲ | - |
| CD4010B | - | 200* | 350* | - |
| | - | 130▲ | 70▲ | - |
| CD4011B | - | 250 | 200 | - |
| CD4012B | - | 250 | 200 | - |
| CD4013B | Clock to Q or \bar{Q} | 300 | 200 | 3.5 |
| | Set to Q or Reset to \bar{Q} | 300* | - | - |
| | Set to \bar{Q} or Reset to Q | 400▲ | - | - |
| CD4014B | - | 320 | 200 | 3 |
| CD4015B | Clock to Q | 320 | 200 | 3 |
| | Reset to Q | 400▲ | - | - |
| CD4016B | Sig. Input to Sig. Output | 100 | - | - |
| | Turn On | 70 | - | - |
| CD4017B | Clock to Out | 650 | 200 | 2.5 |
| | Clock to Carry Out | 600 | - | - |
| | Reset to Out | 530 | - | - |
| CD4018B | Clock to Q | 400 | 200 | 3 |
| | Preset/Reset to Q | 550 | - | - |
| CD4019B | - | 300 | 200 | - |
| CD4020B | ϕ to Q1 | 360 | 200 | 3.5 |
| | Qn to Qn + 1 | 330 | - | - |
| | Reset to Q | 280▲ | - | - |
| CD4021B | - | 320 | 200 | 3 |
| CD4022B | Clock to Carry Out | 600 | 200 | 2.5 |
| | Clock to Decode Out | 650 | - | - |
| | Reset to Output | 530 | - | - |
| CD4023B | - | 250 | 200 | - |

* t_{TLH} or t_{PLH}

▲ t_{THL} or t_{PHL}

| TYPE | CONDITIONS* V _{DD} = 5V, C _L = 50pF | PROP DELAY (ns) | TRANS. TIME (ns) | MAX CLOCK INPUT FREQ. (MHz) |
|----------|---|-----------------|------------------|-----------------------------|
| CD4024B | ϕ to Q1 | 360 | 200 | 3.5 |
| | Qn to Qn + 1 | 330 | - | - |
| | Reset to Q | 280▲ | - | - |
| CD4025B | - | 250 | 200 | - |
| CD4026B | Clock to Carry Out | 500 | 200 | 2.5 |
| | Clock to Decode Out | 700 | - | - |
| | Reset to Carry Out | 550* | - | - |
| | Reset to Decode Out | 600 | - | - |
| CD4027B | Clock to Q or \bar{Q} | 300 | 200 | 3.5 |
| | Set to Q or Reset to \bar{Q} | 300* | - | - |
| | Set to \bar{Q} or Reset to Q | 400▲ | - | - |
| CD4028B | - | 350 | 200 | - |
| CD4029B | Q Output | 500 | 200 | 2 |
| | Carry Output | 560 | - | - |
| | Preset Enable to Q | 470 | - | - |
| | Preset Enable to Carry Out | 640 | - | - |
| CD4030B | - | 280 | 200 | - |
| | - | 280 | 200 | - |
| CD4031B | Clock to \bar{Q} | 500 | 200 | 2 |
| | Clock to Q | 500* | - | - |
| | Clock to Q | 380▲ | - | - |
| | Clock to Q' | 380 | - | - |
| | Clock to CL _D | 200 | - | - |
| CD4033B | Clock to Carry Out | 500 | 200 | 2.5 |
| | Clock to Decode Out | 700 | - | - |
| | Reset to Carry Out | 550* | - | - |
| | Reset to Decode Out | 600 | - | - |
| CD4034B | Parallel In to Parallel Out | 700 | 200 | 2 |
| CD4035B | AE to "A" Out t _{PLZ} , t _{PZL} , t _{PHZ} , t _{PZH} | 400 | - | - |
| | Clock to Q | 500 | 200 | 2 |
| CD4040B | Reset to Q | 460 | - | - |
| | ϕ to Q1 | 360 | 200 | 3.5 |
| | Qn to Qn + 1 | 330 | - | - |
| CD4041UB | Reset to Q | 280▲ | - | - |
| | - | 120 | 80 | - |

High Reliability CD4000B-Series CMOS ICs

Switching Characteristics at 25°C

| TYPE | CONDITIONS* V _{DD} = 5V, C _L = 50pF | PROP. DELAY (ns) | TRANS. TIME (ns) | MAX. CLOCK INPUT FREQ. (MHz) |
|-------------------|--|------------------|------------------|------------------------------|
| CD4042B | Data In to Q | 220 | 200 | - |
| | Data In to \bar{Q} | 300 | - | - |
| | Clock to Q | 450 | - | - |
| | Clock to \bar{Q} | 500 | - | - |
| CD4043B, 44B | Set or Reset to Q | 300 | 200 | - |
| | Enable to Q - t _{PHZ} , t _{PZH} | 230 | - | - |
| | Enable to Q - t _{PLZ} , t _{PZL} | 180 | - | - |
| CD4046B | AC Coupled Signal Input Voltage Sensitivity (Peak to Peak) f _{IN} = 100kHz Sine Wave | 360mV Max | | |
| CD4047B | t _R to Q, \bar{Q} | 1000 | 200 | - |
| | Astable to Q, \bar{Q} | 700 | - | - |
| | Retrigger to Q, \bar{Q} | 600 | - | - |
| | Astable to Oscillator | 400 | - | - |
| | Reset to Q, \bar{Q} | 500 | - | - |
| CD4048B | Ka to Output | 600 | 200 | - |
| CD4049UB | - | 120* | 160* | - |
| | - | 65▲ | 60▲ | - |
| CD4050B | - | 140* | 160* | - |
| | - | 110▲ | 60▲ | - |
| CD4051B, 52B, 53B | Add to Signal Out | 720 | - | - |
| | Inhibit to Signal Out - Channel On | 720 | - | - |
| | Inhibit to Signal Out - Channel Off | 450 | - | - |
| CD4060B | Input Pulse Operation $\phi 1$ to Q4 | 740 | 200 | 3.5 |
| | Qn to Qn = 1 | 200 | - | - |
| | Reset Operation | 360▲ | - | - |
| CD4063B | Comparator Input to Output | 1250 | 200 | - |
| | Cascade Input to Output | 1000 | - | - |
| CD4066B | Signal Input to Signal Output R _L = 200k, V _C = V _{DD} , V _{SS} = GND, V _{IS} = Square Wave \approx 5V and t _r , t _f = 20ns | 40 | - | - |
| | t _{pdC} t _{rC} , t _{fC} = 20ns, R _L = 1k & V _{IS} < 5V | 70 | - | - |
| CD4067B | Add or inhibit to Signal Out Channel On | 650 | - | - |
| | Signal In to Out | 60 | - | - |
| CD4068B | - | 300 | 200 | - |
| CD4070B | - | 280 | 200 | - |

* t_{TLH} or t_{PLH}

▲ t_{THL} or t_{PHL}

| TYPE | CONDITIONS* V _{DD} = 5V, C _L = 50pF | PROP. DELAY (ns) | TRANS. TIME (ns) | MAX. CLOCK INPUT FREQ. (MHz) |
|--|---|------------------|------------------|------------------------------|
| CD4071B, 72B, 73B, 75B | - | 250 | 200 | - |
| | Clock to Q | 600 | 200 | - |
| | - | 280 | 200 | - |
| CD4077B | - | 280 | 200 | - |
| CD4078B | - | 300 | 200 | 3 |
| CD4081B, 82B | - | 250 | 200 | - |
| CD4085B, 86B | Data | 450▲ 620* | 200 | - |
| | Inhibit | 300▲ | - | - |
| | | 500* | - | - |
| CD4089B | Clock to Out | 300 | 200 | 1.2 |
| | Clear to Out | 760 | - | - |
| | Cascade to Out | 180 | - | - |
| CD4093B | - | 380 | 200 | - |
| CD4094B | Clock to Serial Out Qs | 600 | 200 | 1.25 |
| | Clock to Serial Out Q's | 460 | - | - |
| | Clock to Parallel Out | 840 | - | - |
| | Strobe to Parallel Out | 580 | - | - |
| | Out Enable to Parallel Out, t _{PHZ} , t _{PZH} | 280 | - | - |
| | Out Enable to Parallel Out, t _{PLZ} , t _{PZL} | 200 | - | - |
| CD4095B, 96B | Clock to Output | 500 | 200 | 3.5 |
| | Set or Reset | 300 | - | - |
| CD4097B | Address or Inhibit to Sig. Out - Channel On | 650 | - | - |
| | Signal In to Out | 60 | - | - |
| CD4098B | Trigger to Q, \bar{Q} | 500 | 200 | - |
| CD4099B | Data to Output | 400 | 200 | - |
| CD4502B | Data or Inhibit Delay Time | 380* | 200* | - |
| | | 270▲ | 120▲ | - |
| | Disable Delay Time - t _{PHZ} | 120 | - | - |
| | Disable Delay Time - t _{PZH} | 220 | - | - |
| Disable Delay Time - t _{PLZ} , t _{PZL} | 250 | - | - | |
| CD4503B | - | 150* | 90* | - |
| | - | 110▲ | 70▲ | - |
| | t _{PHZ} , t _{PZH} | 140 | - | - |
| t _{PLZ} , t _{PZL} | 180 | - | - | |

High Reliability CD4000B-Series CMOS ICs

Switching Characteristics at 25°C

| TYPE | CONDITIONS* V _{DD} = 5V, C _L = 50pF | | | PROP. DELAY (ns) | TRANS. TIME (ns) | MAX. CLOCK INPUT FREQ. (MHz) |
|-----------------|---|-----------------|-----------------|------------------|------------------|------------------------------|
| | SHIFT MODE | V _{CC} | V _{DD} | | | |
| CD4504B | TTL to CMOS V _{DD} > V _{CC} | 5 | 10 | 280▲ | - | - |
| | CMOS to CMOS V _{DD} > V _{CC} | 5 | 10 | 240▲ | - | - |
| | CMOS to CMOS V _{CC} > V _{DD} | 10 | 5 | 550▲ | - | - |
| | TTL to CMOS V _{DD} > V _{CC} | 5 | 10 | 280* | - | - |
| | CMOS to CMOS V _{DD} > V _{CC} | 5 | 10 | 240* | - | - |
| | CMOS to CMOS V _{CC} > V _{DD} | 10 | 5 | 400* | - | - |
| | All Modes t _{THL} , t _{TLH} | - | 5 | 200 | - | - |
| | | | 10 | 100 | - | - |
| CD4508B | Strobe In to Data Out | | | 260 | 200 | - |
| CD4510B | Clock to Q Output | | | 400 | 200 | 2 |
| | Preset or Reset to Q | | | 420 | - | - |
| | Clock to Carry Out | | | 480 | - | - |
| | Carry In to Carry Out | | | 250 | - | - |
| CD4511B | Data to Output | | | 1040▲ | 310▲ | - |
| | - | | | 1320* | 80* | - |
| CD4512B | Inhibit to Output | | | 280 | 200 | - |
| | "A" Select to Output | | | 400 | - | - |
| | Data to Output | | | 360 | - | - |
| | t _{PHZ} , t _{PZH} | | | 120 | - | - |
| CD4514B, 15B | Strobe or Data | | | 970 | 200 | - |
| | Inhibit | | | 500 | - | - |
| CD4516B | Clock to Q Output | | | 400 | 200 | 2 |
| | Preset or Reset to Q | | | 420 | - | - |
| | Clock to Carry Out | | | 480 | - | - |
| | Carry In to Carry Out | | | 250 | - | - |
| | Preset or Reset to Carry Out | | | 640 | - | - |
| CD4517B | Clock to Q16 | | | 400 | 200 | 3 |
| CD4518B, 20B | Clock to Output | | | 560 | 200 | 1.5 |
| | Reset to Output | | | 650▲ | - | - |
| CD4527B | Clock to Out | | | 300 | 200 | 1.2 |
| | Clear to Out | | | 760 | - | - |
| | Cascade to Out | | | 180 | - | - |
| CD4532B | E ₁ to E _O , E ₁ to G _s | | | 220 | 200 | - |
| | D _n to Q _m | | | 440 | - | - |
| | D _n to G _s , E ₁ to Q _m | | | 340 | - | - |

* t_{TLH} or t_{PLH}

▲ t_{THL} or t_{PHL}

| TYPE | CONDITIONS* V _{DD} = 5V, C _L = 50pF | PROP. DELAY (ns) | TRANS. TIME (ns) | MAX. CLOCK INPUT FREQ. (MHz) |
|-------------------|--|------------------|------------------|------------------------------|
| | | | | |
| | Clock to Q1 8 Bypass Low | 5000 | - | - |
| | Clock to Q16 | 8000 | - | - |
| | Reset to Q _n | 6000▲ | - | - |
| CD4555B, 56B | Select to Any Output | 440 | 200 | - |
| | Enable to Any Output | 400 | - | - |
| CD4585B | Comparator Inputs to Outputs | 600 | 200 | - |
| | Cascade Inputs to Outputs | 400 | - | - |
| CD4724B | Data to Outputs | 400 | 200 | - |
| | Write Disable to Output | 400 | - | - |
| | Reset to Output | 350▲ | - | - |
| | Address to Output | 450 | - | - |
| CD1438B | Trigger to Q, \bar{Q} | 600 | 200 | - |
| | Reset to Q or \bar{Q} | 500 | - | - |
| CD40100B | - | 720 | 200 | 1 |
| CD40101B | Data In to Output | 700 | 200 | - |
| | Inhibit In to Output | 280 | - | - |
| CD40102B, 103B | Clock to Output | 600 | 200 | 0.7 |
| | Carry In/Counter Enable to Output | 400 | - | - |
| | Asynchronous Preset Enable to Output | 1300* | - | - |
| | Clear to Output | 750▲ | - | - |
| CD40104B | Clock to Q | 440 | 200 | 3 |
| | t _{PZH} , t _{PLZ} , t _{PZL} | 160 | - | - |
| | t _{PHZ} | 90 | - | - |
| CD40105B | Shift Out or Reset to Data Out Ready | 370▲ | 200 | 1.5 |
| | Shift In to Data In Ready | 320▲ | - | - |
| | 3-State Control to Data Out t _{PZH} | 280 | - | - |
| | Ripple Thru Delay Input to Out t _{PLH} | 4000* | - | - |
| CD40106B | - | 280 | 200 | - |
| CD40107B | R _L = 120Ω | 200 | 100 | - |
| CD40108B | Clock or Write Enable to Q | 720 | 200 | 1.5 |
| | Read or Write Address to Q | 600 | - | - |
| | Disable Delay Time t _{PZH} , t _{PHZ} | 200 | - | - |
| | Disable Delay Time t _{PZL} , t _{PLZ} | 260 | - | - |

High Reliability CD4000B-Series CMOS ICs

Switching Characteristics at 25°C

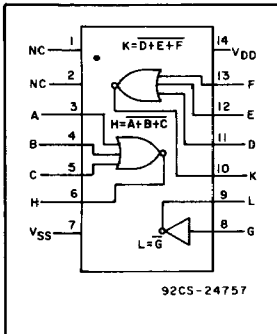
| TYPE | CONDITIONS* V _{DD} = 5V, C _L = 50pF | | | | PROP. DELAY (ns) | TRANS. TIME (ns) | MAX. CLOCK INPUT FREQ. (MHz) | |
|----------------------------------|--|-----------------|-----------------|-----------------|------------------|------------------|------------------------------|-----|
| CD40109B | Data Input to Output | | | | | | | |
| | SHIFT MODE | V _{CC} | V _{DD} | | | | | |
| | | | | | | | | L-H |
| | L-H | 5V | 10V | 260* | - | - | - | |
| | H-L | 10V | 5V | 500▲ | 200 | - | - | |
| | H-L | 10V | 5V | 460* | - | - | - | |
| | 3-State Disable Delay R _L = 1kΩ | | | | | | | |
| | t _{PHZ} | SHIFT MODE | V _{CC} | V _{DD} | | | | |
| | | | | | | | | |
| | t _{PHZ} | H-L | 10V | 5V | 400 | - | - | - |
| | t _{PLZ} | L-H | 5V | 10V | 740 | - | - | - |
| | t _{PLZ} | H-L | 10V | 5V | 500 | - | - | - |
| | t _{PZH} | L-H | 5V | 10V | - | - | - | - |
| | t _{PZH} | H-L | 10V | 5V | 600 | - | - | - |
| t _{PZL} | L-H | 5V | 10V | 200 | - | - | - | |
| t _{PZL} | H-L | 10V | 5V | 400 | - | - | - | |
| CD40110B | Clock to Carry or Borrow | | | | 600 | - | 1.0 | |
| CD40147B | In-Phase Output | | | | 900 | 200 | - | |
| CD40160B, 161B, 162B, 163B | Clock to Q | | | | 400 | 200 | 2 | |
| | Clock to C _{OUT} | | | | 450 | - | - | |
| | T _E to C _{OUT} | | | | 250 | - | - | |
| CD40174B | Clear to Q (CD40160B & CD 40161B only) | | | | 500▲ | - | - | |
| | Clear to Output | | | | 200▲ | - | - | |
| CD40175B | Clock to Q Output | | | | 400 | 200 | 2.0 | |
| | Clear to Q Output | | | | 500▲ | - | - | |

* t_{TLH} or t_{PLH}

▲ t_{THL} or t_{PHL}

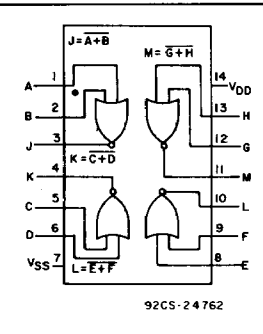
| TYPE | CONDITIONS* V _{DD} = 5V, C _L = 50pF | PROP. DELAY (ns) | TRANS. TIME (ns) | MAX. CLOCK INPUT FREQ. (MHz) |
|-------------------|--|------------------|------------------|------------------------------|
| CD40181B | A or B to F (Logic Mode) A or B to G or P | 800 | 200 | - |
| | A or B to F, C _n + 4, or A = B | 1000 | - | - |
| | C _n to F | 640 | - | - |
| | C _n to C _n + 4 | 400 | - | - |
| CD40182B | P, G _{IN} to P, G _{OUT} and Carry Outs | 400 | 200 | - |
| | C _n to Carry Outs | 480 | - | - |
| CD40192B, 193B | Clock Up or Clock Down to Q, Reset Q | 500 | 200 | 2 |
| | \overline{PE} to Q | 400 | - | - |
| | Clock Up to Carry, Clock Down to Borrow | 320 | - | - |
| | Reset or \overline{PE} to Borrow or Carry | 600 | - | - |
| CD40194B | Clock to Q | 440 | 200 | 3 |
| | Reset to Q | 460▲ | - | - |
| CD40208B | Clock or Write Enable to Q | 720 | 200 | 1.5 |
| | Read or Write Address to Q | 600 | - | - |
| | 3-State Disable Delay Time | 200 | - | - |
| CD40257B | t _{PZH} , t _{PHZ} | 260 | - | - |
| | t _{PZL} , t _{PLZ} | 260 | - | - |
| | Data Input to Output | 300 | 200 | - |
| | Select to Output | 380 | - | - |
| | Output Disable to Output | - | - | - |
| | t _{PZH} , t _{PHZ} | 190 | - | - |
| | t _{PZL} , t _{PLZ} | 190 | - | - |

Functional Diagrams



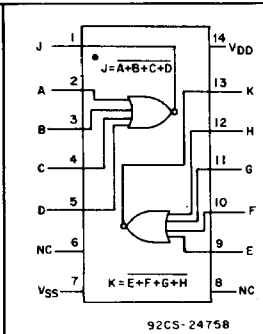
Dual 3-Input NOR Gate Plus Inverter

CD4000B (File No. 985)



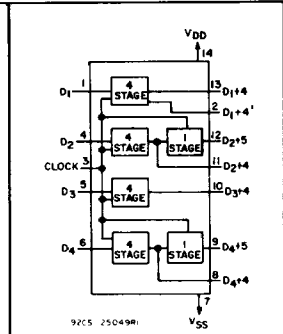
Quad 2-Input NOR Gate

CD4001B (File No. 985)
(File No. 945)



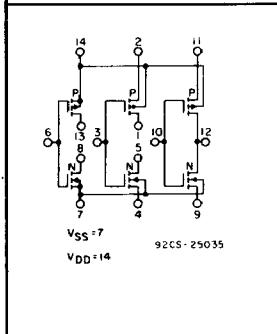
Dual 4-Input NOR Gate

CD4002B (File No. 985)



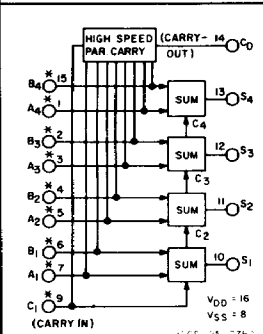
18-Stage Static Shift Register

CD4006B (File No. 1033)



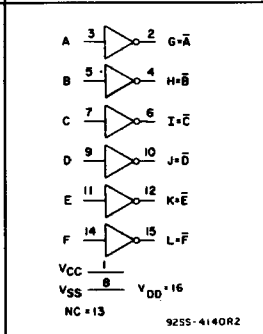
Dual Complementary Pair Plus Inverter

CD4007UB (File No. 977)



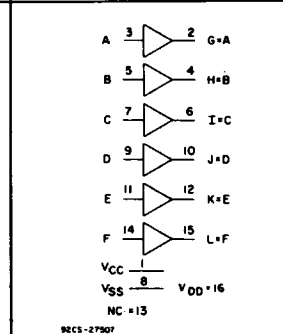
4-Bit Full Adder with Parallel Carry Out

CD4008B (File No. 951)



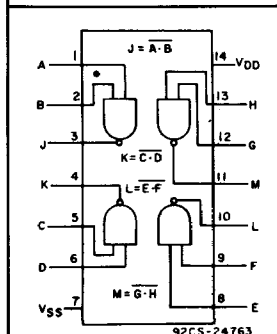
Hex Buffer/Converter Inverting Type

CD4009UB (File No. 940)



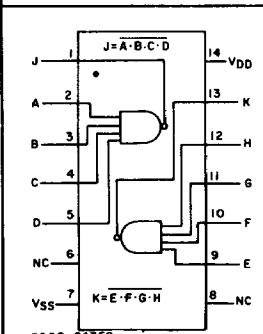
Hex Buffer/Converter Non-Inverting Type

CD4010B (File No. 940)



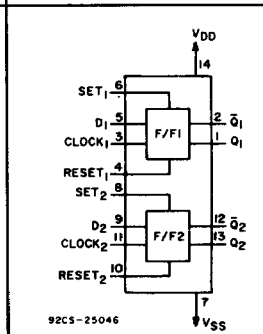
Quad 2-Input NAND Gate

CD4011B (File No. 986)



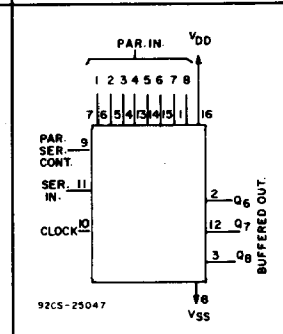
Dual 4-Input NAND Gate

CD4012B (File No. 986)



Dual "D" Flip-Flop with Set/Reset Capability

CD4013B (File No. 936)



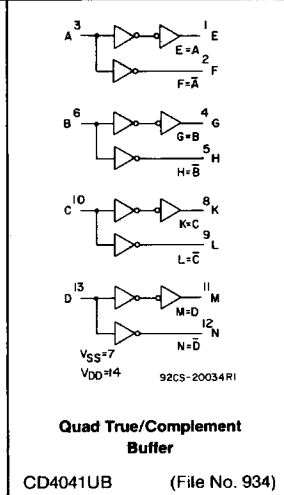
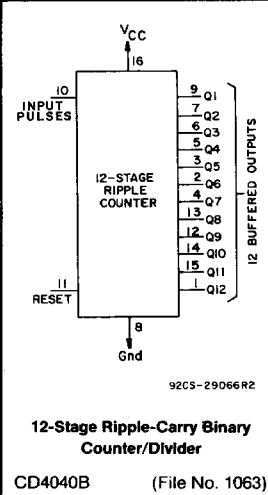
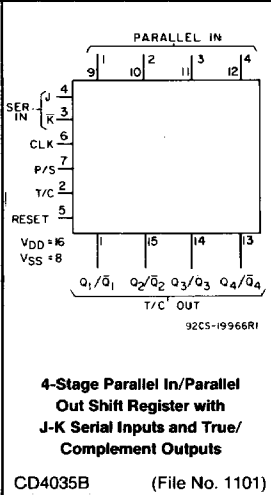
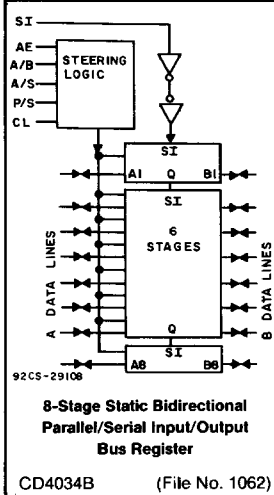
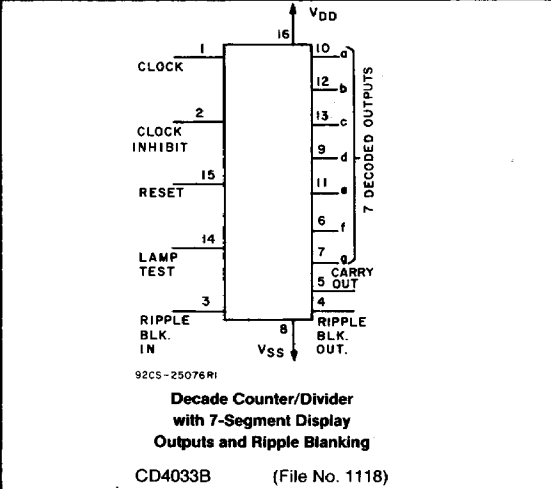
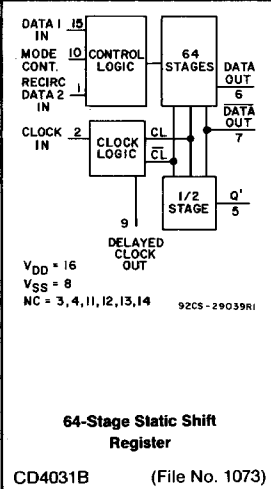
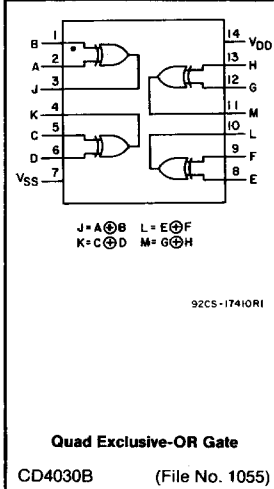
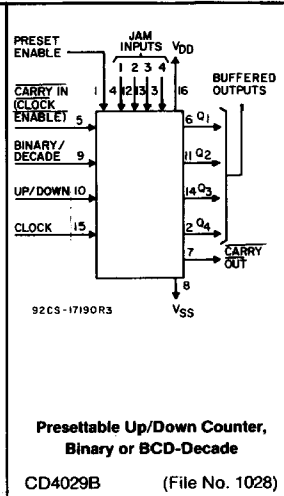
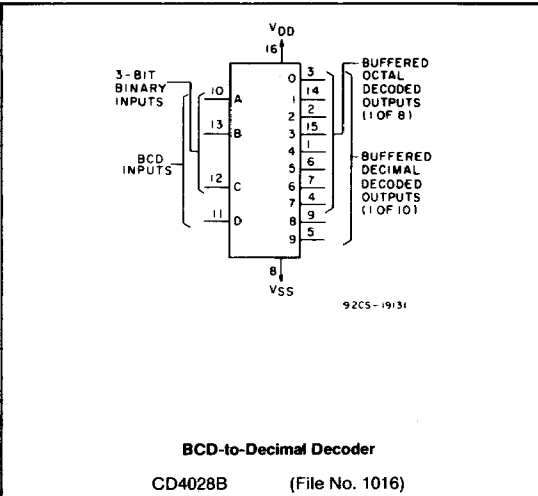
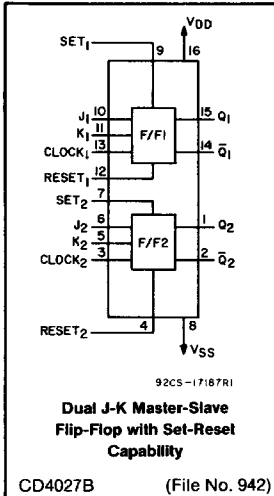
8-State Synchronous Shift Register with Parallel or Serial Input/Serial Output

CD4014B (File No. 1043)

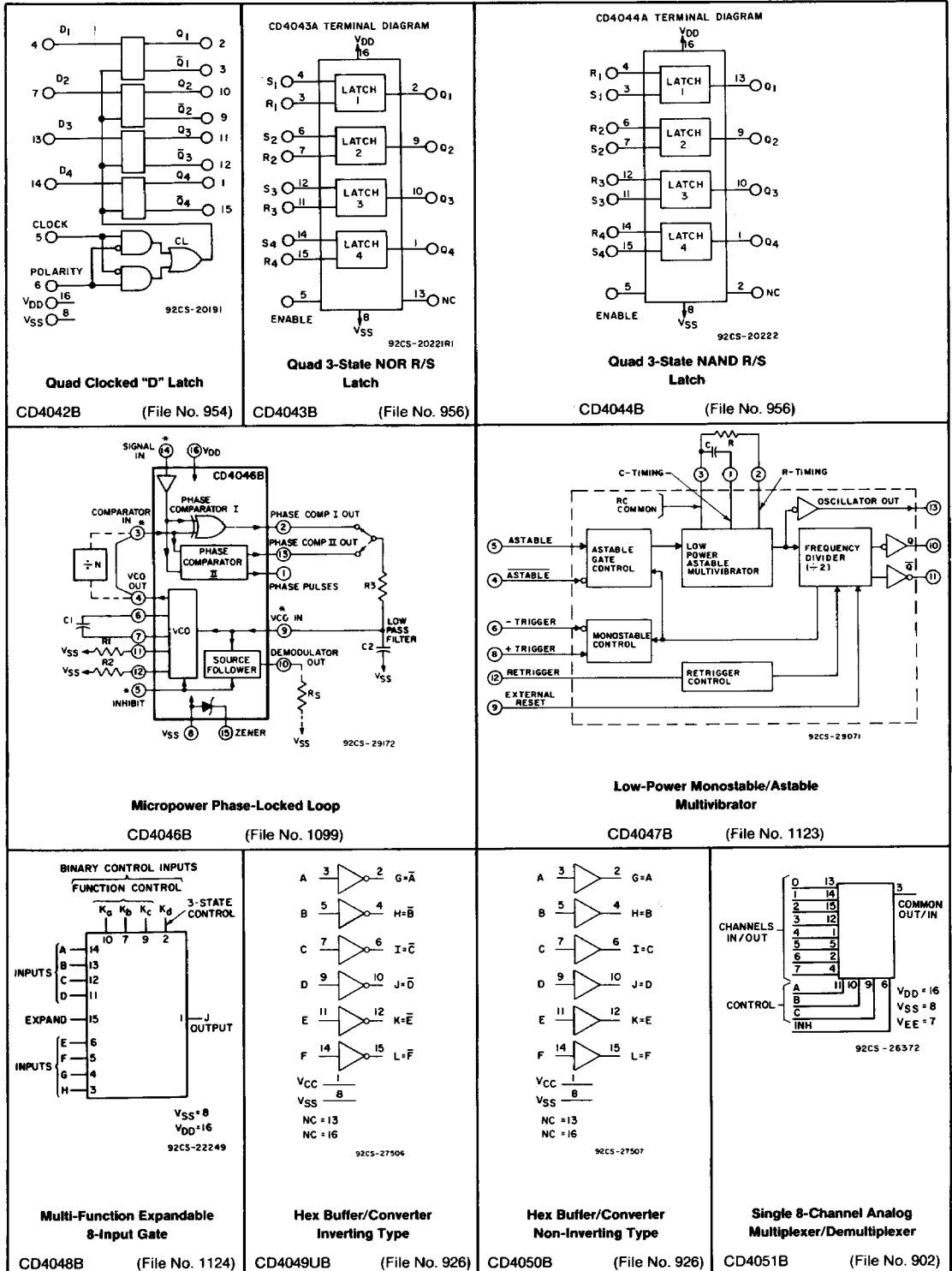
Functional Diagrams

| | | | |
|---|--|--|--|
| <p>Dual 4-Stage Static Shift Register with Serial Input/Parallel Output</p> <p>CD4015B (File No. 1024)</p> | <p>Quad Bilateral Switch</p> <p>CD4016B (File No. 953)</p> | <p>Decade Counter/Divider with 10 Decoded Decimal Outputs</p> <p>CD4017B (File No. 1113)</p> | <p>Presettable Divide-by-"N" Counter Fixed or Programmable</p> <p>CD4018B (File No. 1034)</p> |
| <p>Quad AND/OR Select Gate</p> <p>CD4019B (File No. 1045)</p> | <p>14-Stage Binary Ripple Counter</p> <p>CD4020B (File No. 1063)</p> | <p>8-Stage Static Shift Register Asynchronous Parallel or Synchronous Serial Input/Serial Output</p> <p>CD4021B (File No. 1043)</p> | <p>Divide-by-8 Counter/Divider with 8 Decoded Decimal Outputs</p> <p>CD4022B (File No. 1113)</p> |
| <p>Triple 3-Input NAND Gate</p> <p>CD4023B (File No. 986)</p> | <p>7-Stage Ripple-Carry Binary Counter/Divider</p> <p>CD4024B (File No. 1063)</p> | <p>Triple 3-Input NOR Gate</p> <p>CD4025B (File No. 985)</p> | <p>Decade Counter/Divider with 7-Segment Display Output and Display Enable</p> <p>CD4026B (File No. 1118)</p> |

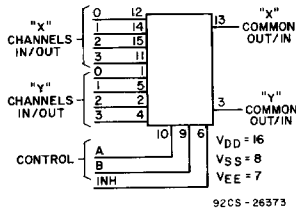
Functional Diagrams



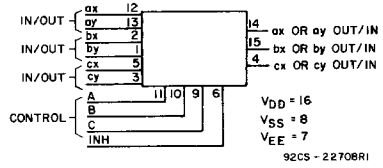
Functional Diagrams



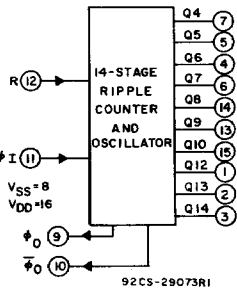
Functional Diagrams



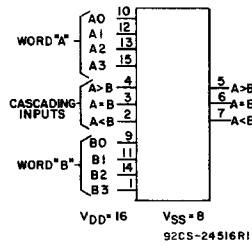
Differential 4-Channel Analog Multiplexer/Demultiplexer
CD4052B (File No. 902)



Triple 2-Channel Multiplexer/Demultiplexer
CD4053B (File No. 902)

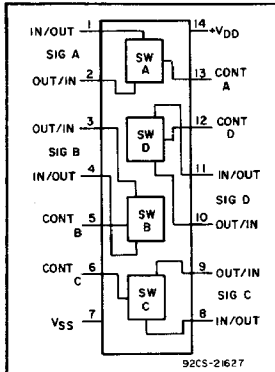


14-Stage Ripple-Carry Binary Counter/Divider and Oscillator
CD4060B (File No. 1120)



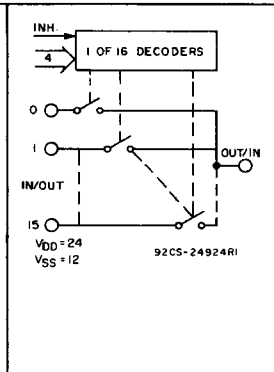
4-Bit Magnitude Comparator
CD4063B (File No. 805)

Functional Diagrams



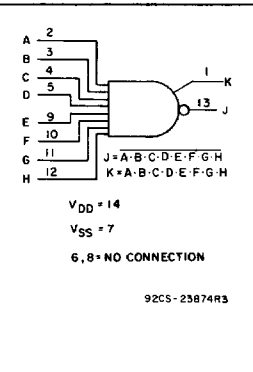
Quad Bilateral Switch

CD4066B (File No. 1114)



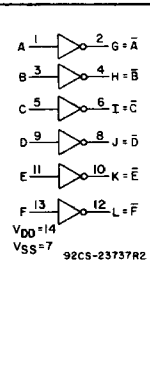
16-Channel Multiplexer/Demultiplexer

CD4067B (File No. 909)



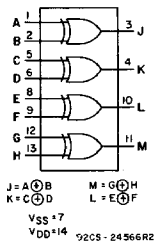
8-Input NAND/AND Gate

CD4068B (File No. 809)



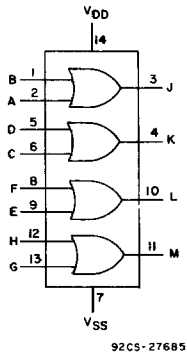
Hex Inverter

CD4069UB (File No. 804)



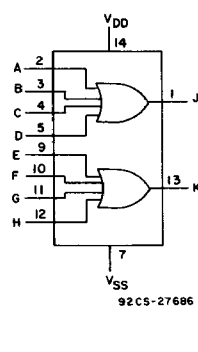
Quad Exclusive-OR Gate

CD4070B (File No. 910)



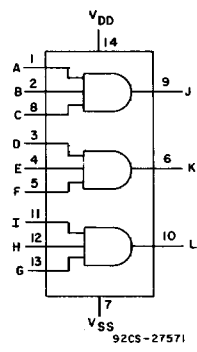
Quad 2-Input OR Gate

CD4071B (File No. 807)



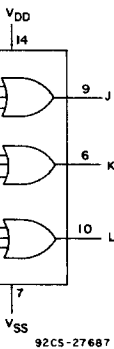
Dual 4-Input OR Gate

CD4072B (File No. 807)



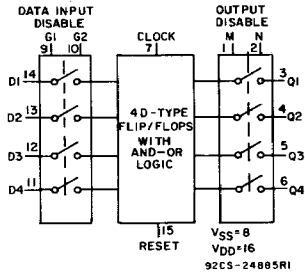
Triple 3-Input AND Gate

CD4073B (File No. 806)



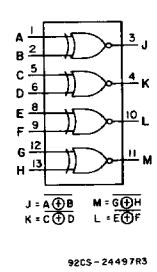
Triple 3-Input OR Gate

CD4075B (File No. 807)



4-Bit D-Type Register

CD4076B (File No. 903)



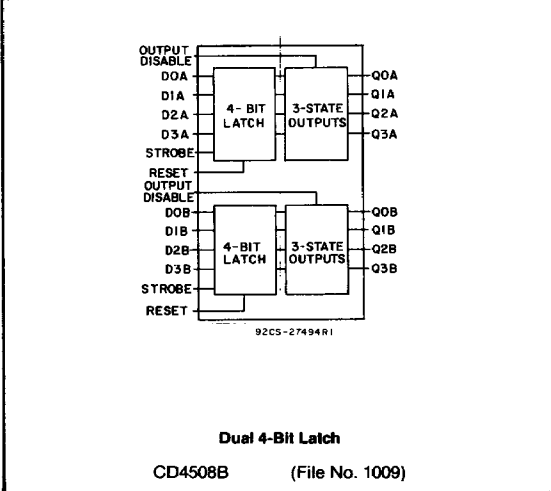
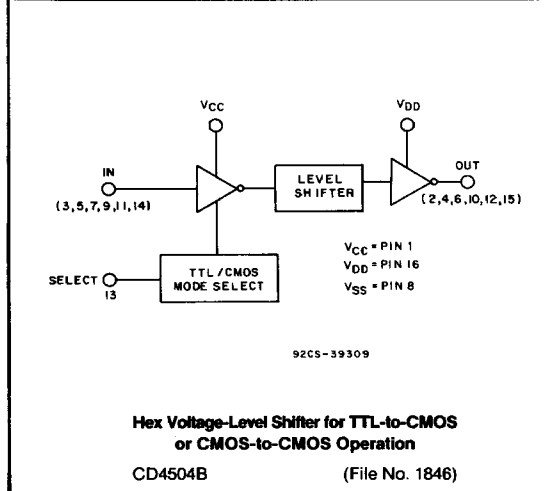
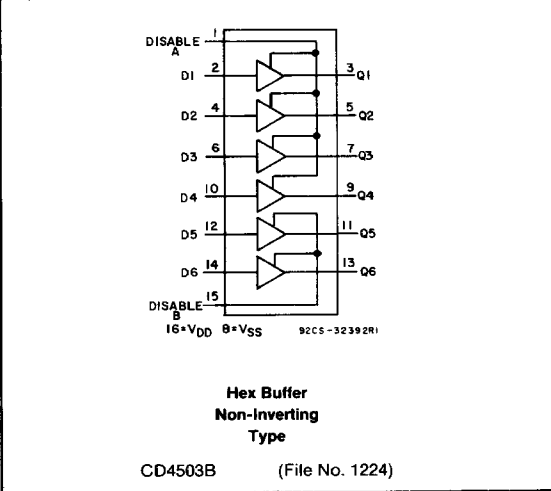
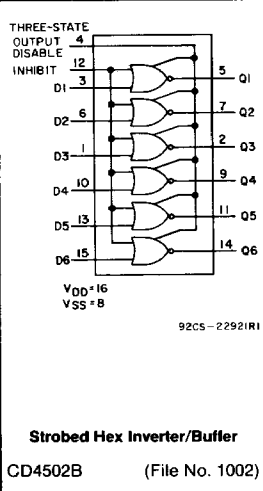
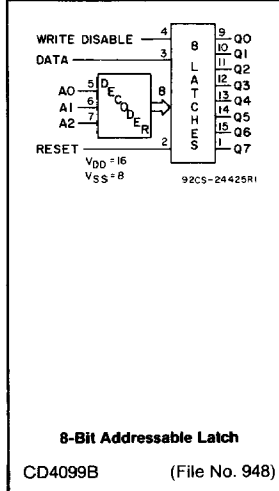
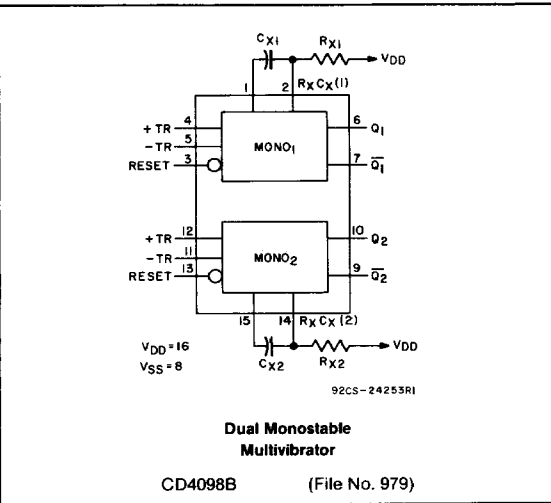
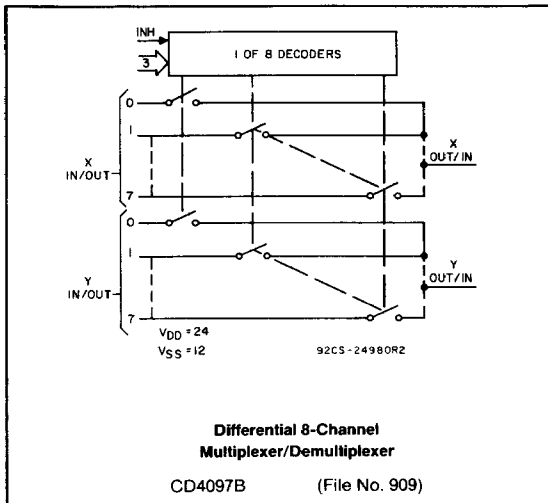
Quad Exclusive-NOR Gate

CD4077B (File No. 910)

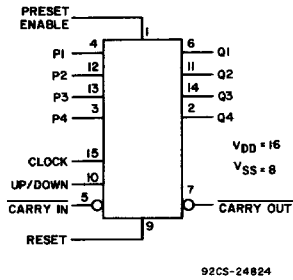
Functional Diagrams

| | | | |
|---|--|--|--|
| <p style="text-align: center;">8-Input NOR/OR Gate</p> <p style="text-align: center;">CD4078B (File No. 810)</p> | <p style="text-align: center;">Quad 2-Input AND Gate</p> <p style="text-align: center;">CD4081B (File No. 806)</p> | <p style="text-align: center;">Dual 4-Input AND Gate</p> <p style="text-align: center;">CD4082B (File No. 806)</p> | <p style="text-align: center;">Dual 2-Wide, 2-Input AND-OR-INVERT (AOI) Gate</p> <p style="text-align: center;">CD4085B (File No. 811)</p> |
| <p style="text-align: center;">Expandable 4-Wide, 2-Input AND-OR-INVERT (AOI) Gate</p> <p style="text-align: center;">CD4086B (File No. 812)</p> | <p style="text-align: center;">Binary Rate Multiplier</p> <p style="text-align: center;">CD4089B (File No. 1003)</p> | | |
| <p style="text-align: center;">Quad 2-Input NAND Schmitt Trigger</p> <p style="text-align: center;">CD4093B (File No. 836)</p> | <p style="text-align: center;">8-Stage Shift-and-Store Bus Register</p> <p style="text-align: center;">CD4094B (File No. 869)</p> | <p style="text-align: center;">Gated J-K Master-Slave Flip-Flop, Non-Inverting Inputs</p> <p style="text-align: center;">CD4095B (File No. 879)</p> | <p style="text-align: center;">Gated J-K Master-Slave Flip-Flop, Inverting and Non-Inverting Inputs</p> <p style="text-align: center;">CD4096B (File No. 879)</p> |

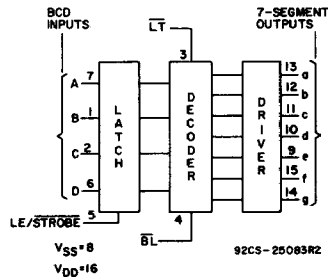
Functional Diagrams



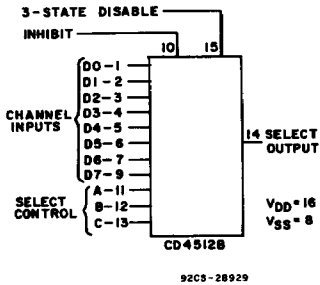
Functional Diagrams



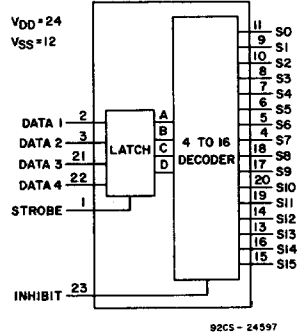
BCD Presettable Up/Down Counter
CD4510B (File No. 899)



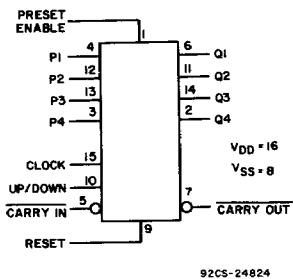
BCD-to-7-Segment Latch Decoder Driver
CD4511B (File No. 901)



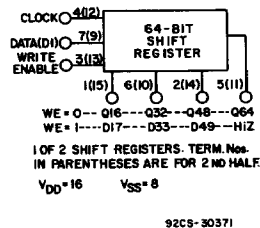
8-Channel Data Selector
CD4512B (File No. 1032)



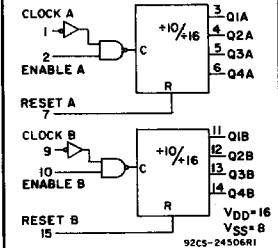
4-Bit Latch/4-to-16 Line Decoder
CD4514B (File No. 814) CD4515B (File No. 814)
Output "High" on Select Output "Low" on Select



Binary Presettable Up/Down Counter
CD4516B (File No. 899)

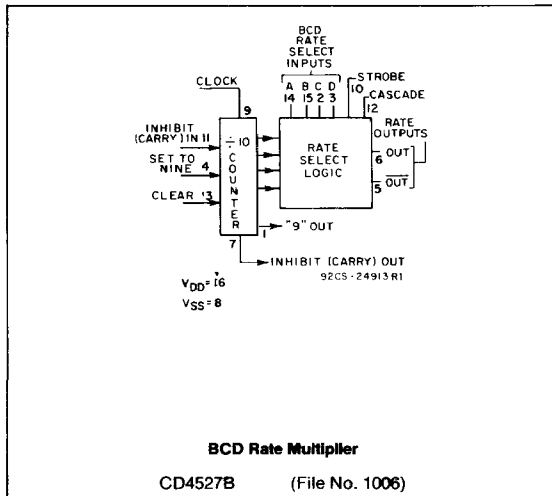


Dual 64-Bit Shift Register
CD4517B (File No. 1148)



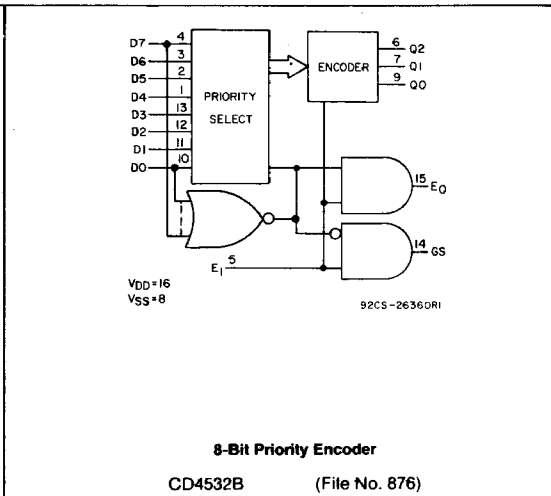
Dual Up Counter
CD4518B (File No. 808) BCD
CD4520B (File No. 808) Binary

Functional Diagrams



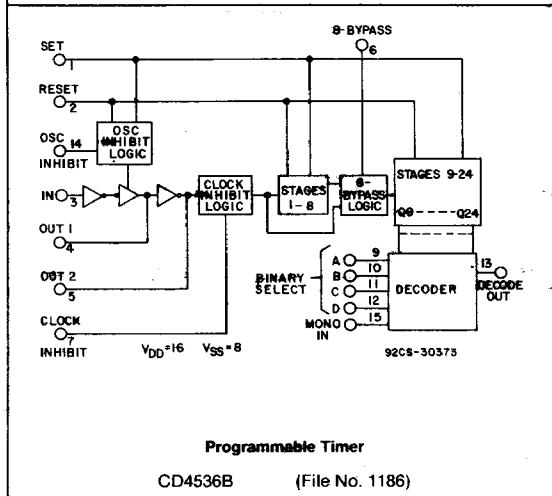
BCD Rate Multiplier

CD4527B (File No. 1006)



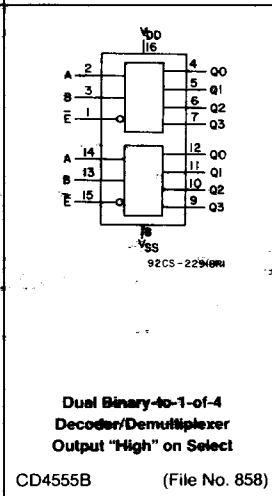
8-Bit Priority Encoder

CD4532B (File No. 876)



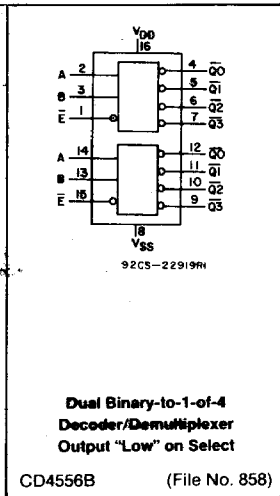
Programmable Timer

CD4536B (File No. 1186)



Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "High" on Select

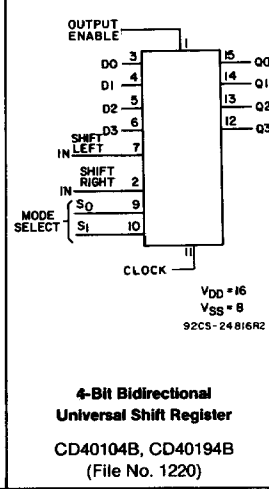
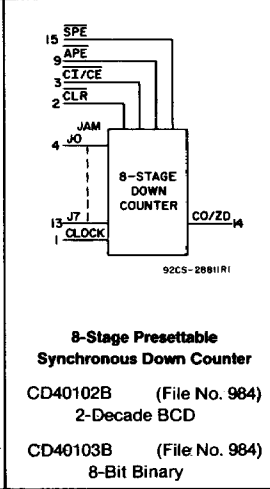
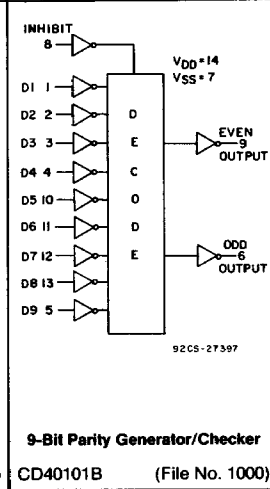
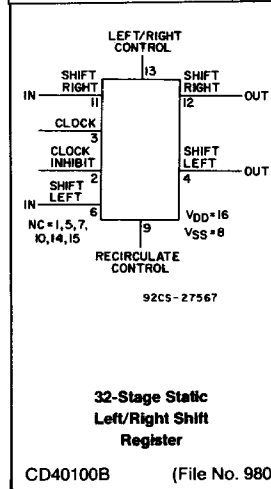
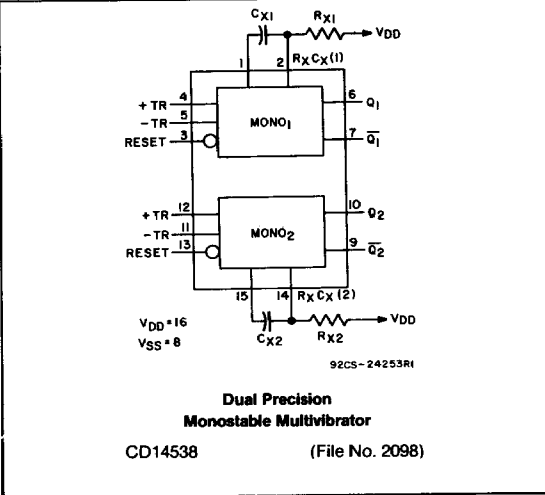
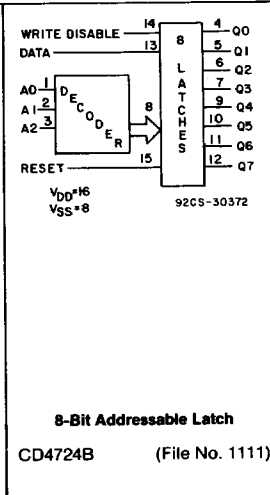
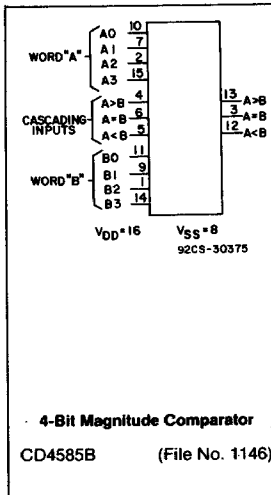
CD4555B (File No. 858)



Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "Low" on Select

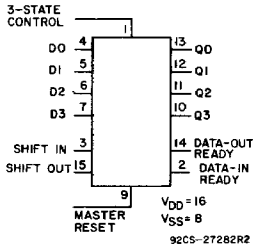
CD4556B (File No. 858)

Functional Diagrams

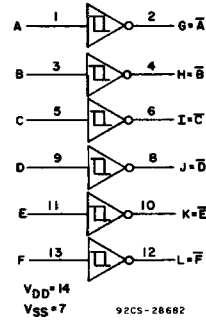


File No. = commercial data sheet

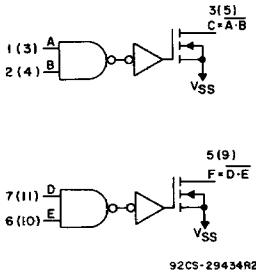
Functional Diagrams



FIFO Register
4-Bits Wide by 16-Bits Long
CD40105B (File No. 1044)

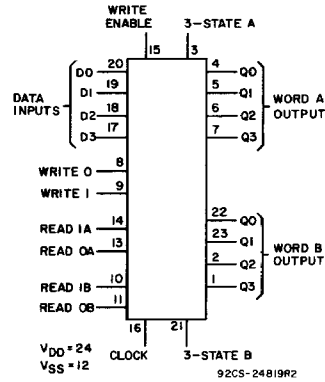


Hex Schmitt Trigger
CD40106B (File No. 1017)

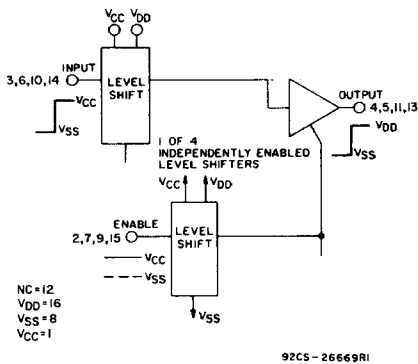


Dual 2-Input NAND Buffer/Driver
CD40107B (File No. 1015)

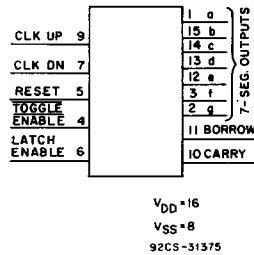
NOTE:
NUMBERS IN PARENTHESES
FOR CD40107BF, OTHERS
FOR CD40107BE.



4-by-4 Multiport Register
CD40108B (File No. 1011)

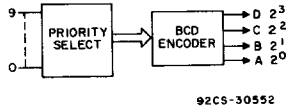


Quad Low-to-High Voltage Level Shifter
CD40109B (File No. 1018)



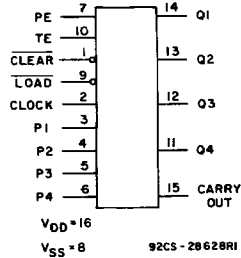
**Decade Up-Down Counter/
Decoder/Latch/Driver**
CD40110B (File No. 1125)

Functional Diagrams



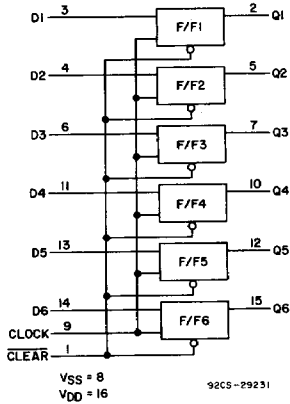
**10-Line-to-4-Line
BCD Priority Encoder**

CD40147B (File No. 1117)



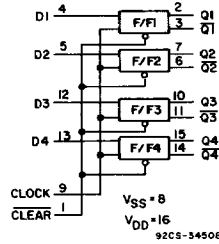
Synchronous 4-Bit Counter

CD40160B (File No. 1047)
Decade with Asynchronous Clear
CD40161B (File No. 1047)
Binary with Asynchronous Clear
CD40162B (File No. 1047)
Decade with Synchronous Clear
CD40163B (File No. 1047)
Binary with Synchronous Clear



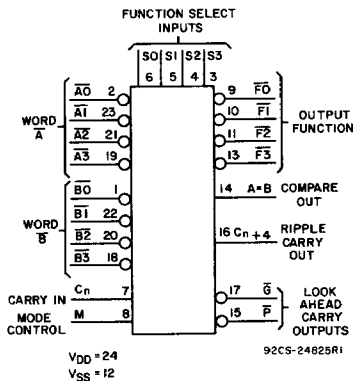
Hex "D" Type Flip-Flop

CD40174B (File No. 1031)



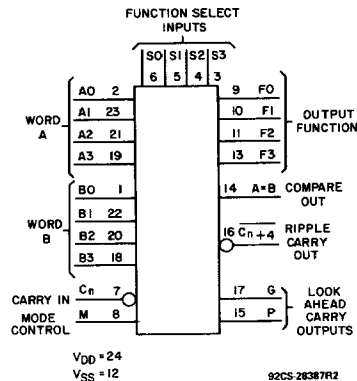
Quad 'D' Type Flip-Flop

CD40175B (File No. 1326)



Active-Low Data

CD40181B



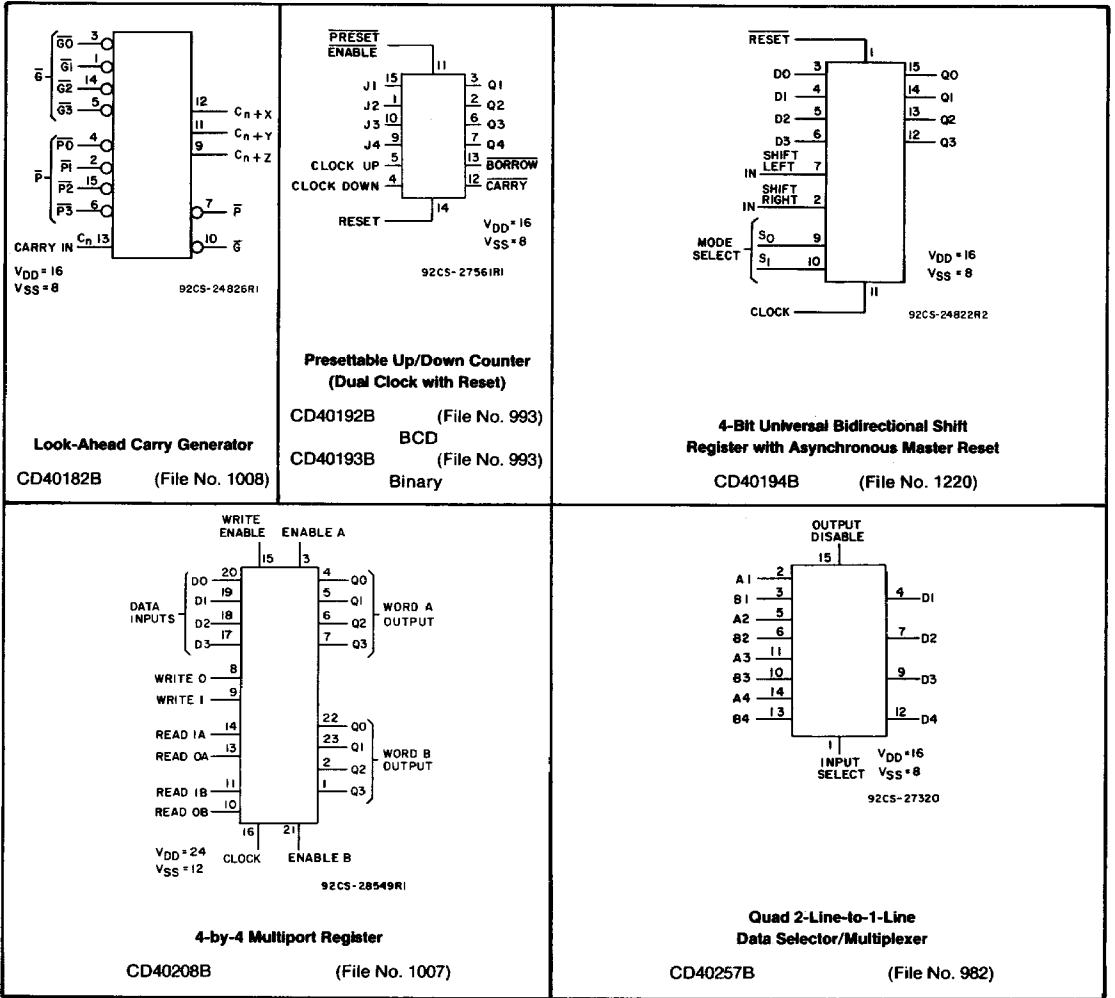
Active-High Data

(File No. 989)

4-Bit Arithmetic Logic Unit

High Reliability CD400B-Series CMOS ICs

Functional Diagrams



File No. = commercial data sheet

High Reliability CD4000B-Series CMOS ICs

Static Burn-In Test Circuit Connections

For Type A devices, use $V_{DD} = 12.5V$. For Type B and UB devices, use $V_{DD} = 18V$.

NOTE: Each pin except V_{DD} and V_{SS} must have resistors of 2-47 kilohms. In most cases, V_{SS} is at pin 7 (of 14-pin IC), pin 8 (of 16-pin) or pin 12 (of 24-pin), while V_{DD} is at the highest-numbered pin; exceptions are noted by an asterisk (*).

| TYPE | STATIC BURN-IN I | | | STATIC BURN-IN II | | |
|---------|-----------------------|---------------------|---------------|-----------------------|--------|------------------------|
| | OPEN | GROUND | V_{DD} | OPEN | GROUND | V_{DD} |
| CD4000 | 1,2,6,9,10 | 3-5,7,8,11-13 | 14 | 1,2,6,9,10 | 7 | 3-5,8,11-14 |
| CD4001 | 3,4,10,11 | 1,2,5-9,12,13 | 14 | 3,4,10,11 | 7 | 1,2,5,6,8,9,12-14 |
| CD4002 | 1,6,8,13 | 2-5,7,9-12 | 14 | 1,6,8,13 | 7 | 2-5,9-12,14 |
| CD4006 | 2,8-13 | 1,3-7 | 14 | 2,8-13 | 7 | 1,3-6,14 |
| CD4007 | 1,5,8,12,13 | 3,4,6,7,9,10 | 2,11,14 | 1,5,8,12,13 | 4,7,9 | 2,3,6,10,11,14 |
| CD4008 | 10-14 | 1-9,15 | 16 | 10-14 | 8 | 1-7,9,15,16 |
| CD4009* | 2,4,6,10,12,13,15 | 3,5,7-9,11,14 | 1*,16* | 2,4,6,10,12,13,15 | 8 | 1*,3,5,7,9,11,14,16* |
| CD4010* | 2,4,6,10,12,13,15 | 3,5,7-9,11,14 | 1*,16* | 2,4,6,10,12,13,15 | 8 | 1*,3,5,7,9,11,14,16* |
| CD4011 | 3,4,10,11 | 1,2,5-9,12,13 | 14 | 3,4,10,11 | 7 | 1,2,5,6,8,9,12-14 |
| CD4012 | 1,6,8,13 | 2-5,7,9-12 | 14 | 1,6,8,13 | 7 | 2-5,9-12,14 |
| CD4013 | 1,2,12,13 | 3-11 | 14 | 1,2,12,13 | 7 | 3-6,8-11,14 |
| CD4014 | 2,3,12 | 1,4-11,13-15 | 16 | 2,3,12 | 8 | 1,4-7,9-11,13-16 |
| CD4015 | 2-5,10-13 | 1,6-9,14,15 | 16 | 2-5,10-13 | 8 | 1,6,7,9,14-16 |
| CD4016 | 2,3,9,10 | 1,4-8,11-13 | 14 | 2,3,9,10 | 7 | 1,4-6,8,11-14 |
| CD4017 | 1-7,9-12 | 8,13,15 | 14,16 | 1-7,9-12 | 8,14 | 13,15,16 |
| CD4018 | 4-6,11,13 | 1-3,7-9,12,14,15 | 16 | 4-6,11,13 | 8 | 1-3,7,9,10,12,14-16 |
| CD4019 | 10-13 | 1-9,14,15 | 16 | 10-13 | 8 | 1-7,9,14-16 |
| CD4020 | 1-7,9,12-15 | 8,10,11 | 16 | 1-7,9,12-15 | 8 | 10,11,16 |
| CD4021 | 2,3,12 | 1,4-11,13-15 | 16 | 2,3,12 | 8 | 1,4-7,9-11,13-16 |
| CD4022 | 1-7,9-12 | 8,13,15 | 14,16 | 1-7,9-12 | 8,14 | 13,15,16 |
| CD4023 | 6,9,10 | 1-5,7,8,11-13 | 14 | 6,9,10 | 7 | 1-5,8,11-14 |
| CD4024 | 3-6,8-13 | 1,2,7 | 14 | 3-6,8-13 | 7 | 1,2,14 |
| CD4025 | 6,9,10 | 1-5,7,8,11-13 | 14 | 6,9,10 | 7 | 1-5,8,11-14 |
| CD4026 | 4-7,9-14 | 1-3,8,15 | 16 | 4-7,9-14 | 8 | 1-3,15,16 |
| CD4027 | 1,2,14,15 | 3-13 | 16 | 1,2,14,15 | 8 | 3-7,9-13,16 |
| CD4028 | 1-7,9,14,15 | 8,10-13 | 16 | 1-7,9,14,15 | 8 | 10-13,16 |
| CD4029 | 2,6,7,11,14 | 1,3-5,8-10,12,13,15 | 16 | 2,6,7,11,14 | 8 | 1,3-5,9,10,12,13,15,16 |
| CD4030 | 3,4,10,11 | 1,2,5-9,12,13 | 14 | 3,4,10,11 | 7 | 1,2,5,6,8,9,12-14 |
| CD4031 | 3-7,9,11-14 | 1,2,8,10,15 | 16 | 3-7,9,11-14 | 8 | 1,2,10,15,16 |
| CD4033 | 4-7,9-13 | 1-3,8,14,15 | 16 | 4-7,9-13 | 8 | 1-3,14-16 |
| CD4034 | 1-8 | 12,15-23 | 9-11,13,14,24 | 1-8 | 12 | 9-11,13-24 |
| CD4035 | 1,13-15 | 2-12 | 16 | 1,13-15 | 8 | 2-7,9-12,16 |
| CD4040 | 1-7,9,12-15 | 8,10,11 | 16 | 1-7,9,12-15 | 8 | 10,11,16 |
| CD4041 | 1,2,4,5,8,9,11,12 | 3,6,7,10,13 | 14 | 1,2,4,5,8,9,11,12 | 7 | 3,6,10,13,14 |
| CD4042 | 1-3,9-12,15 | 4-8,13,14 | 16 | 1-3,9-12,15 | 8 | 4-7,13,14,16 |
| CD4043 | 1,2,9,10,13 | 3-8,11,12,14,15 | 16 | 1,2,9,10,13 | 8 | 3-7,11,12,14-16 |
| CD4044 | 1,2,9,10,13 | 3-8,11,12,14,15 | 16 | 1,2,9,10,13 | 8 | 3-7,11,12,14-16 |
| CD4046 | 1,2,4,6,7,10,11,13,15 | 3,5,8,9,14 | 12,16 | 1,2,4,6,7,10,11,13,15 | 8 | 3,5,9,12,14,16 |
| CD4047 | 1,2,10,11,13 | 3-9,12 | 14 | 1,2,10,11,13 | 7 | 3-6,8,9,12,14 |

Non-standard pin arrangement, or multiple supply pins; connect pins marked () without using resistor.

High Reliability CD400B-Series CMOS ICs

Static Burn-In Test Circuit Connections

| TYPE | STATIC BURN-IN I | | | STATIC BURN-IN II | | |
|---------|----------------------|---------------------------|-------------------------|----------------------|--------|---------------------------------------|
| | OPEN | GROUND | V _{DD} | OPEN | GROUND | V _{DD} |
| CD4048 | 1 | 2-15 | 16 | 1 | 8 | 2-7,9-16 |
| CD4049* | 2,4,6,10,12,13,15 | 3,5,7-9,11,14 | 1*,16* | 2,4,6,10,12,13,15 | 8 | 1*,3,5,7,9,11,14,16* |
| CD4050* | 2,4,6,10,12,13,15 | 3,5,7-9,11,14 | 1*,16* | 2,4,6,10,12,13,15 | 8 | 1*,3,5,7,9,11,14,16* |
| CD4051* | 3 | 1,2,4-6,7*,8*,9-15 | 16 | 3 | 7*,8* | 1,2,4-6,9-16 |
| CD4052* | 3,13 | 1,2,4-6,7*,8*,9-12,14,15 | 16 | 3,13 | 7*,8* | 1,2,4-6,9-12,14-16 |
| CD4053* | 4,14,15 | 1-3,5,6,7*,8*,9-13 | 16 | 4,14,15 | 7*,8* | 1-3,5,6,9-13,16 |
| CD4060 | 1-7,9,10,13-15 | 8,11,12 | 16 | 1-7,9,10,13-15 | 8 | 11,12,16 |
| CD4063 | 5-7 | 1,2,4,8-15 | 3,16 | 5-7 | 3,8 | 1,2,4,9-16 |
| CD4066 | 2,3,9,10 | 1,4-8,11-13 | 14 | 2,3,9,10 | 7 | 1,4-6,8,11-14 |
| CD4067 | 1 | 2-23 | 24 | 1 | 12 | 2-11,13-23 |
| CD4068 | 1,6,8,13 | 2-5,7,9-12 | 14 | 1,6,8,13 | 7 | 2-5,9-12,14 |
| CD4069 | 2,4,6,8,10,12 | 1,3,5,7,9,11,13 | 14 | 2,4,6,8,10,12 | 7 | 1,3,5,9,11,13,14 |
| CD4070 | 3,4,10,11 | 1,2,5-9,12,13 | 14 | 3,4,10,11 | 7 | 1,2,5,6,8,9,12-14 |
| CD4071 | 3,4,10,11 | 1,2,5-9,12,13 | 14 | 3,4,10,11 | 7 | 1,2,5,6,8,9,12-14 |
| CD4072 | 1,6,8,13 | 2-5,7,9-12 | 14 | 1,6,8,13 | 7 | 2-5,9-12,14 |
| CD4073 | 6,9,10 | 1-5,7,8,11-13 | 14 | 6,9,10 | 7 | 1-5,8,11-14 |
| CD4075 | 6,9,10 | 1-5,7,8,11-13 | 14 | 6,9,10 | 7 | 1-5,8,11-14 |
| CD4076 | 3-6 | 1,2,7-15 | 16 | 3-6 | 8 | 1,2,7,9-16 |
| CD4077 | 3,4,10,11 | 1,2,5-9,12,13 | 14 | 3,4,10,11 | 7 | 1,2,5,6,8,9,12-14 |
| CD4078 | 1,6,8,13 | 2-5,7,9-12 | 14 | 1,6,8,13 | 7 | 2-5,9-12,14 |
| CD4081 | 3,4,10,11 | 1,2,5-9,12,13 | 14 | 3,4,10,11 | 7 | 1,2,5,6,8,9,12-14 |
| CD4082 | 1,6,8,13 | 2-5,7,9-12 | 14 | 1,6,8,13 | 7 | 2-5,9-12,14 |
| CD4085 | 3,4 | 1,2,5-13 | 14 | 3,4 | 7 | 1,2,5,6,8-14 |
| CD4086 | 3,4 | 1,2,5-13 | 14 | 3,4 | 7 | 1,2,5,6,8-14 |
| CD4089 | 1,5-7 | 2-4,8-15 | 16 | 1,5-7 | 8 | 2-4,9-16 |
| CD4093 | 3,4,10,11 | 1,2,5-9,12,13 | 14 | 3,4,10,11 | 7 | 1,2,5,6,8,9,12-14 |
| CD4094 | 4-7,9-14 | 1-3,8,15 | 16 | 4-7,9-14 | 8 | 1-3,15,16 |
| CD4095 | 1,6,8 | 2-5,7,9-13 | 14 | 1,6,8 | 7 | 2-5,9-14 |
| CD4096 | 1,6,8 | 2-5,7,9-13 | 14 | 1,6,8 | 7 | 2-5,9-14 |
| CD4097 | 1,17 | 2-16,18-23 | 24 | 1,17 | 12 | 2-11,13-24 |
| CD4098 | 2,6,7,9,10,14 | 1,3-5,8,11-13,15 | 16 | 2,6,7,9,10,14 | 1,8,15 | 3-5,11-13,16 |
| CD4099 | 1,9-15 | 2-8 | 16 | 1,9-15 | 8 | 2-7,16 |
| CD4502 | 2,5,7,9,11,14 | 1,3,4,6,8,10,12,13,15 | 16 | 2,5,7,9,11,14 | 8 | 1,3,4,6,10,12,13,15,16 |
| CD4503 | 3,5,7,9,11,13 | 1,2,4,6,8,10,12,14,15 | 16 | 3,5,7,9,11,13 | 8 | 1,2,4,6,10,12,14-16 |
| CD4504 | 2,4,6,10,12,15 | 3,5,7-9,11,14 | 16 (1*,13) ¹ | 2,4,6,10,12,15 | 8 | 16 (1*,3,5,7,9,11,13,14) ¹ |
| CD4508 | 5,7,9,11,17,19,21,23 | 1-4,6,8,10,12-16,18,20,22 | 24 | 5,7,9,11,17,19,21,23 | 12 | 1-4,6,8,10,13-16,18,20,22,24 |
| CD4510 | 2,6,7,11,14 | 1,3-5,8-10,12,13,15 | 16 | 2,6,7,11,14 | 8 | 1,3-5,9,10,12,13,15,16 |
| CD4511 | 9-15 | 1-8 | 16 | 9-15 | 8 | 1-7,16 |
| CD4512 | 14 | 1-13,15 | 16 | 14 | 8 | 1-7,9-13,15,16 |

Non-standard pin arrangement, or multiple supply pins; connect pins marked () without using resistor.

¹Pin voltage is V_{DD}/2 for pins inside parentheses.

High Reliability CD400B-Series CMOS ICs

Static Burn-In Test Circuit Connections

| TYPE | STATIC BURN-IN I | | | STATIC BURN-IN II | | |
|----------|---------------------|----------------------|--------------------|---------------------|--------|--|
| | OPEN | GROUND | V _{DD} | OPEN | GROUND | V _{DD} |
| CD4514 | 4-11,13-20 | 1-3,12,21-23 | 24 | 4-11,13-20 | 12 | 1-3,21-24 |
| CD4515 | 4-11,13-20 | 1-3,12,21-23 | 24 | 4-11,13-20 | 12 | 1-3,21-24 |
| CD4516 | 2,6,7,11,14 | 1,3-5,8-10,12,13,15 | 16 | 2,6,7,11,14 | 8 | 1,3-5,9,10,12,13,15,16 |
| CD4517 | 1,2,5,6,10,11,14,15 | 3,4,7-9,12,13 | 16 | 1,2,5,6,10,11,14,15 | 8 | 3,4,7,9,12,13,16 |
| CD4518 | 3-6,11-14 | 1,2,7-10,15 | 16 | 3-6,11-14 | 8 | 1,2,7,9,10,15,16 |
| CD4520 | 3-6,11-14 | 1,2,7-10,15 | 16 | 3-6,11-14 | 8 | 1,2,4,9,10,15,16 |
| CD4527 | 1,5-7 | 2-4,8-15 | 16 | 1,5-7 | 8 | 2-4,9-16 |
| CD4532 | 6,7,9,14,15 | 1-5,8,10-13 | 16 | 6,7,9,14,15 | 8 | 1-5,10-13,16 |
| CD4536 | 4,5,13 | 1-3,6-12,14,15 | 16 | 4,5,13 | 8 | 1-3,6,7,9-12,14-16 |
| CD4555 | 4-7,9-12 | 1-3,8,13-15 | 16 | 4-7,9-12 | 8 | 1-3,13-16 |
| CD4556 | 4-7,9-12 | 1-3,8,13-15 | 16 | 4-7,9-12 | 8 | 1-3,13-16 |
| CD4585 | 3,12,13 | 1,2,4-11,14,15 | 16 | 3,12,13 | 8 | 1,2,4-7,9-11,14-16 |
| CD4724 | 4-7,9-12 | 1-3,8,13-15 | 16 | 4-7,9-12 | 8 | 1,3,13-16 |
| CD14538 | 2,6,7,9,10,14 | 1,3-5,8,11-13,15 | 16 | 2,6,7,9,10,14 | 1,8,15 | 3-5,11-13,16 |
| CD40100 | 1,4,5,7,10,12,14,15 | 2,3,6,8,9,11,13 | 16 | 1,4,5,7,10,12,14,15 | 8 | 2,3,6,9,11,13,16 |
| CD40101 | 6,9 | 1-5,7,8,10-13 | 14 | 6,9 | 7 | 1-5,8,10-14 |
| CD40102 | 14 | 1-13,15 | 16 | 14 | 8 | 1-7,9-13,15,16 |
| CD40103 | 14 | 1-13,15 | 16 | 14 | 8 | 1-7,9-13,15,16 |
| CD40104 | 12-15 | 1-11 | 16 | 12-15 | 8 | 1-7,9-11,16 |
| CD40105 | 2,10-14 | 1,3-9,15 | 16 | 2,10-14 | 8 | 1,3-7,9,15,16 |
| CD40106 | 2,4,6,8,10,12 | 1,3,5,7,9,11,13 | 14 | 2,4,6,8,10,12 | 7 | 1,3,5,9,11,13,14 |
| CD40107 | 1,2,5,6,8,9,12,13 | 3,4,7,10,11 | 14 | 1,2,5,6,8,9,12,13 | 7 | 3,4,10,11,14 |
| CD40108 | 1,2,4-7,22,23 | 3,8-21 | 24 | 1,2,4-7,22,23 | 12 | 3,8-11,13-21,24 |
| CD40109* | 4,5,11-13 | 2,3,6-10,14,15 | 1 [•] ,16 | 4,5,11-13 | 8 | (1 [•] ,2,3,6,7,9,10,14,15) ¹ 16 |
| CD40110 | 1-3,10-15 | 4-9 | 16 | 1-3,10-15 | 8 | 4-7,9,16 |
| CD40147 | 6,7,9,14 | 1-5,8,10-13,15 | 16 | 6,7,9,14 | 8 | 1-5,10-13,15,16 |
| CD40160 | 11-15 | 1-10 | 16 | 11-15 | 8 | 1-7,9,10,16 |
| CD40161 | 11-15 | 1-10 | 16 | 11-15 | 8 | 1-7,9,10,16 |
| CD40162 | 11-15 | 1-10 | 16 | 11-15 | 8 | 1-7,9,10,16 |
| CD40163 | 11-15 | 1-10 | 16 | 11-15 | 8 | 1-7,9,10,16 |
| CD40174 | 2,5,7,10,12,15 | 1,3,4,6,8,9,11,13,14 | 16 | 2,5,7,10,12,15 | 8 | 1,3,4,6,9,11,13,14,16 |

*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using resistor.

¹Pin voltage is V_{DD}/2 for pins inside parentheses.

²V_{DD} = 11.5 volts; V_{CC} = 6.5 volts; use 300 Ω resistors at pins 10,13-21.

High Reliability CD4000B-Series CMOS ICs

Static Burn-In Test Circuit Connections

| TYPE | STATIC BURN-IN I | | | STATIC BURN-IN II | | |
|---------|---------------------|-----------------------|-----------------|---------------------|--------|------------------------|
| | OPEN | GROUND | V _{DD} | OPEN | GROUND | V _{DD} |
| CD40175 | 2,3,6,7,10,11,14,15 | 1,4,5,8,9,12,13 | 16 | 2,3,6,7,10,11,14,15 | 8 | 1,4,5,9,12,13,16 |
| CD40181 | 9-11,13-17 | 1-8,12,18-23 | 24 | 9-11,13-17 | 12 | 1-8,18-24 |
| CD40182 | 7,9-12 | 1-6,8,13-15 | 16 | 7,9-12 | 8 | 1-6,13-16 |
| CD40192 | 2,3,6,7,12,13 | 1,4,5,8-11,14,15 | 16 | 2,3,6,7,12,13 | 8 | 1,4,5,9-11,14-16 |
| CD40193 | 2,3,6,7,12,13 | 1,4,5,8-11,14,15 | 16 | 2,3,6,7,12,13 | 8 | 1,4,5,9-11,14-16 |
| CD40194 | 12-15 | 1-11 | 16 | 12-15 | 8 | 1-7,9-11,16 |
| CD40208 | 1,2,4-7,22,23 | 3,8-21 | 24 | 1,2,4-7,22,23 | 12 | 3,8-11,13-21,24 |
| CD40257 | 4,7,9,12 | 1-3,5,6,8,10,11,13-15 | 16 | 4,7,9,12 | 8,15 | 1-3,5,6,10,11,13,14,16 |

Dynamic Burn-In Test Circuit Connections

| TYPE | OPEN | GROUND | 1/2 V _{DD} | V _{DD} | OSCILLATOR | |
|---------|-----------|---------------|---------------------|-----------------|-------------------|-------------|
| | | | | | 50 kHz | 25 kHz |
| CD4000 | 1,2 | 7 | 6,9,10 | 14 | 3-5,8,11-13 | — |
| CD4001 | — | 7 | 3,4,10,11 | 14 | 1,2,5,6,8,9,12,13 | — |
| CD4002 | 6,8 | 7 | 1,13 | 14 | 2-5,9-12 | — |
| CD4006 | 2 | 7 | 8-13 | 14 | 3 | 1,4-6 |
| CD4007 | — | 4,7,9 | 1,5,8,12,13 | 2,11,14 | 3,6,10 | — |
| CD4008 | — | 8 | 10-14 | 16 | 2,4,6,15 | 1,3,5,7,9 |
| CD4009* | 13 | 8 | 2,4,6,10,12,15 | 1*,16* | 3,5,7,9,11,14 | — |
| CD4010* | 13 | 8 | 2,4,6,10,12,15 | 1*,16* | 3,5,7,9,11,14 | — |
| CD4011 | — | 7 | 3,4,10,11 | 14 | 1,2,5,6,8,9,12,13 | — |
| CD4012 | 6,8 | 7 | 1,13 | 14 | 2-5,9-12 | — |
| CD4013 | — | 4,6-8,10 | 1,2,12,13 | 14 | 3,11 | 5,9 |
| CD4014 | — | 1,4-9,13-15 | 2,3,12 | 16 | 10 | 11 |
| CD4015 | — | 6,8,14 | 2-5,10-13 | 16 | 1,9 | 7,15 |
| CD4016 | — | 7 | 2,3,9,10 | 14 | 5,6,12,13 | 1,4,8,11 |
| CD4017 | — | 8,13,15 | 1-7,9-12 | 16 | 14 | — |
| CD4018 | — | 2,8,9,15 | 4-6,11,13 | 1,3,12,16 | 7,14 | 10 |
| CD4019 | — | 8 | 10-13 | 16 | — | 1-7,9,14,15 |
| CD4020 | — | 8,11 | 1-7,9,12-15 | 16 | 10 | — |
| CD4021 | — | 1,4-9,13-15 | 2,3,12 | 16 | 10 | 11 |
| CD4022 | — | 8,13,15 | 1-7,9-12 | 16 | 14 | — |
| CD4023 | — | 7 | 6,9,10 | 14 | 1-5,8,11-13 | — |
| CD4024 | 8,10,13 | 2,7 | 3-6,9,11,12 | 14 | 1 | — |
| CD4025 | — | 7 | 6,9,10 | 14 | 1-5,8,11-13 | — |
| CD4026 | — | 2,8,15 | 4-7,9-14 | 3,16 | 1 | — |
| CD4027 | — | 4,7-9,12 | 1,2,14,15 | 5,6,10,11,16 | 3,13 | — |
| CD4028 | — | 8 | 1-7,9,14,15 | 16 | 10,12,13 | 11 |
| CD4029 | — | 1,3-5,8,12,13 | 2,6,7,11,14 | 9,10,16 | 15 | — |
| CD4030 | — | 7 | 3,4,10,11 | 14 | 2,6,9,13 | 1,5,8,12 |
| CD4031 | 3-5,11-14 | 8,15 | 6,7,9 | 1,16 | 2 | 10 |

Non-standard pin arrangement, or multiple supply pins; connect pins marked () without using a resistor.

High Reliability CD400B-Series CMOS ICs

Dynamic Burn-In Test Circuit Connections

| TYPE | OPEN | GROUND | 1/2 V _{DD} | V _{DD} | OSCILLATOR | |
|---------|---------------------|-------------------|---------------------|-----------------|-------------------|----------------------------|
| | | | | | 50 kHz | 25 kHz |
| CD4033 | — | 2,3,8,14,15 | 4-7,9-13 | 16 | 1 | — |
| CD4034 | — | 1-8,11-14 | 16-23 | 9,24 | 15 | 10 |
| CD4035 | 1,3,4 | 2,5,7-12 | 13-15 | 16 | 6 | — |
| CD4040 | — | 8,11 | 1-7,9,12-15 | 16 | 10 | — |
| CD4041 | — | 7 | 1,2,4,5,8,9,11,12 | 14 | 3,6,10,13 | — |
| CD4042 | — | 8 | 1-3,9-12,15 | 6,16 | 5 | 4,7,13,14 |
| CD4043 | 13 | 8 | 1,2,9,12 | 5,16 | 4,6,12,14 | 3,7,11,15 |
| CD4044 | 2 | 8 | 1,9,10,13 | 5,16 | 4,6,12,14 | 3,7,11,15 |
| CD4046 | 1,4,6,7,10,11,13,15 | 8,9 | 2 | 3,5,12,16 | 14 | — |
| CD4047 | — | 7,9,12 | 1,2,10,11,13 | 4,5,14 | 6,8 | 3 |
| CD4048 | — | 8,15 | 1 | 2,16 | 9-14 | 3-7 |
| CD4049* | 13 | 8 | 2,4,6,10,12,15 | 1*,16 | 3,5,7,9,11,14 | — |
| CD4050* | 13 | 8 | 2,4,6,10,12,15 | 1*,16 | 3,5,7,9,11,14 | — |
| CD4051* | — | 4-6,7*,8*,9,12,14 | 3 | 1,2,13,15,16 | 11 | 10 |
| CD4052* | — | 4-6,7*,8*,12,15 | 3,13 | 1,2,11,14,16 | 10 | 9 |
| CD4053* | — | 1,5,6,7*,8*,12 | 4,14,15 | 2,3,13,16 | 9-11 | — |
| CD4054 | — | 7*,8 | 3-6 | 1,10,12,14 | 2 | 9,11,13,15 |
| CD4055 | — | 7*,8 | 1,9-15 | 16 | 6 | 2-5 |
| CD4056 | — | 7*,8 | 9-15 | 1,16 | 6 | 2-5 |
| CD4060 | — | 8,12 | 1-7,9,10,13-15 | 16 | 11 | — |
| CD4063 | — | 1,2,4,8,10,11,13 | 5-7 | 3,16 | 12,15 | 9,14 |
| CD4066 | — | 7 | 2,3,9,10 | 14 | 5,6,12,13 | 1,4,8,11 |
| CD4067 | — | 12,15 | 1 | 24 | 2-9,16-23 | (10,11,13,14) ¹ |
| CD4068 | 6,8 | 7 | 1,13 | 14 | 2-5,9-12 | — |
| CD4069 | — | 7 | 2,4,6,8,10,12 | 14 | 1,3,5,9,11,13 | — |
| CD4070 | — | 7 | 3,4,10,11 | 14 | 1,5,8,12 | 2,6,9,13 |
| CD4071 | — | 7 | 3,4,10,11 | 14 | 1,2,5,6,8,9,12,13 | — |
| CD4072 | 6,8 | 7 | 1,13 | 14 | 2-5,9-12 | — |
| CD4073 | — | 7 | 6,9,10 | 14 | — | 1-5,8,11-13 |
| CD4075 | — | 7 | 6,9,10 | 14 | — | 1-5,8,11-13 |
| CD4076 | — | 1,2,8-10,15 | 3-6 | 16 | 7 | 11-14 |
| CD4077 | — | 7 | 3,4,10,11 | 14 | 1,5,8,12 | 2,6,9,13 |
| CD4078 | 6,8 | 7 | 1,13 | 14 | 2-5,9-12 | — |
| CD4081 | — | 7 | 3,4,10,11 | 14 | 1,2,5,6,8,9,12,13 | — |
| CD4082 | 6,8 | 7 | 1,13 | 14 | 2-5,9-12 | — |
| CD4085 | — | 7 | 3,4 | 14 | 1,2,5,6,8,9,12,13 | 10,11 |
| CD4086 | 4 | 7 | 3 | 14 | 1,2,5,6,8,9,11-13 | 10 |
| CD4089 | — | 2,4,8,10,12-15 | 1,5-7 | 3,16 | 9 | 11 |
| CD4093 | — | 7 | 3,4,10,11 | 14 | 1,2,5,6,8,9,12,13 | — |
| CD4094 | — | 8 | 4-7,9-14 | 1,15,16 | 3 | 2 |
| CD4095 | 1 | 2,7,13 | 6,8 | 3-5,9-11,14 | — | 12 |
| CD4096 | 1 | 2,5,7,9,13 | 6,8 | 3,4,10,11,14 | 12 | — |
| CD4097 | — | 12,13 | 1,17 | 24 | 2-9,15,16,18-23 | (10,11,14) ² |
| CD4098 | — | 1,4,8,12,15 | 6,7,9,10 | 2,14,16 | 5,11 | 3,13 |

Non-standard pin arrangement, or multiple supply pins; connect pins marked () without using a resistor.

¹Pin 10 is @ 14 kHz; pin 11 is @ 7 kHz; pin 13 is @ 1.7 kHz; pin 14 is @ 3.5 kHz.

²Pin 10 is @ 14 kHz; pin 11 is @ 7 kHz; pin 14 is @ 3.5 kHz.

High Reliability CD400B-Series CMOS ICs

Dynamic Burn-In Test Circuit Connections

| TYPE | OPEN | GROUND | 1/2 V _{DD} | V _{DD} | OSCILLATOR | |
|----------|----------------|-----------------|----------------------|-----------------|------------------------------|-----------------------------|
| | | | | | 50 kHz | 25 kHz |
| CD4099 | — | 5-8 | 1,9-15 | 16 | 2,4 | 3 |
| CD4502 | — | 8 | 2,5,7,9,11,14 | 16 | 4 | 1,3,6,10,12,13,15 |
| CD4503 | — | 1,8,15 | 3,5,7,9,11,13 | 16 | 2,4,6,10,12,14 | — |
| CD4504 | — | 8 | 1*,2,4,6,10,12,15 | 16 | (3,5,7,9,11,14) ³ | 13 ³ |
| CD4508 | — | 1,3,12,13,15 | 5,7,9,11,17,19,21,23 | 2,14,24 | 4,6,8,10,16,18,20,22 | — |
| CD4510 | — | 1,3,4,8,9,12,13 | 2,6,7,11,14 | 10,16 | 15 | 5 |
| CD4511 | 9-15 | 5,8 | — | 3,4,16 | 1,2,7 | 6 |
| CD4512 | — | 8,10,15 | 14 | 16 | 1-7,9,11,12 | 13 |
| CD4514 | — | 2,3,12 | 4-11,13-20 | 21,22,24 | 1 | 23 |
| CD4515 | — | 2,3,12 | 4-11,13-20 | 21,22,24 | 1 | 23 |
| CD4516 | — | 1,3,4,8,9,12,13 | 2,6,7,11,14 | 10,16 | 15 | 5 |
| CD4517 | — | 3,8,13 | 1,2,5,6,10,11,14,15 | 16 | 4,12 | 7,9 |
| CD4518 | — | 7,8,15 | 3-6,11-14 | 2,10,16 | 1,9 | — |
| CD4520 | — | 7,8,15 | 3-6,11-14 | 2,10,16 | 1,9 | — |
| CD4527 | — | 2,4,8,10,12-15 | 1,5-7 | 3,16 | 9 | 11 |
| CD4532 | — | 8 | 6,7,9,14,15 | 5,16 | 1-4,10-13 | — |
| CD4536 | — | 1,2,6-8,14,15 | 4,5,13 | 9-12,16 | 3 | — |
| CD4541 | 4,11 | 5-7 | 1,2,8 | 9,10,12-14 | 3 | — |
| CD4543 | — | 6-8 | 9-15 | 1,4,16 | 2,3,5 | — |
| CD4555 | — | 1,8,15 | 4-7,9-12 | 16 | 2,14 | 3,13 |
| CD4556 | — | 1,8,15 | 4-7,9-12 | 16 | 2,14 | 3,13 |
| CD4585 | — | 5-9,11,14,15 | 3,12,13 | 1,4,16 | 2 | 10 |
| CD4724 | — | 1-3,8 | 4-7,9-12 | 16 | 14,15 | 13 |
| CD14538 | — | 1,4,8,12,15 | 6,7,9,10 | 2,14,16 | 5,11 | 3,13 |
| CD22100 | — | 8 | 10,11,14,15 | 7,16 | 1,3,9,12,13 | (2,4-6) ⁴ |
| CD22101 | — | 12 | 4,5,8,9,16,17,20,21 | 24 | 3,6,7,10,15,18,19,22 | (1,2,11,14,23) ⁵ |
| CD40100 | 1,5,7,10,14,15 | 2,8,13 | 4,12 | 9,16 | 3 | 6,11 |
| CD40101 | — | 4,7 | 6,9 | 12,14 | 2,3,5,8,10 | 1,11,13 |
| CD40102 | — | 3,8,15 | 14 | 2,16 | 1,4,6,11,13 | 5,7,9,10,12 |
| CD40103 | — | 3,8,15 | 14 | 2,16 | 1,4,6,11,13 | 5,7,9,10,12 |
| CD40104 | — | 7,8,10 | 12-15 | 1,3-6,9,16 | 11 | 2 |
| CD40105 | — | 1,8,9 | 2,10-14 | 16 | 3,15 | 4-7 |
| CD40106 | — | 7 | 2,4,6,8,10,12 | 14 | 1,3,5,9,11,13 | — |
| CD40107 | 1,2,6,8,12,13 | 7 | 5,9 | 14 | — | 3,4,10,11 |
| CD40108 | — | 12 | 1,2,4-7,22,23 | 3,15,16,21,24 | 8,11,14,19,20 | 9,10,13,17,18 |
| CD40109* | 12 | 8 | 1*,4,5,11,13 | 16 | (3,6,10,14) ⁵ | (2,7,9,15) ³ |
| CD40110 | — | 4-8 | 1-3,10-15 | 16 | 9 | — |
| CD40116* | — | — | — | — | — | — |
| CD40117 | — | 7 | 3-6,8-11 | 14 | 12,13 | 1,2 |
| CD40147 | — | 8 | 6,7,9,14 | 16 | 1,3,11,13 | 2,4,5,10,12,15 |
| CD40160 | — | 8 | 11-15 | 1,7,9,10,16 | 2-6 | — |
| CD40161 | — | 8 | 11-15 | 1,7,9,10,16 | 2-6 | — |
| CD40162 | — | 8 | 11-15 | 1,7,9,10,16 | 2-6 | — |
| CD40163 | — | 8 | 11-15 | 1,7,9,10,16 | 2-6 | — |
| CD40174 | — | 8 | 2,5,7,10,12,15 | 1,16 | 9 | 3,4,6,11,13,14 |

*Pin Voltage is V_{DD}/2.

³Pin 5 is @ 14 kHz; Pin 6 is @ 7 kHz; Pin 2 is @ 3.5 kHz.

⁴Pin 2 is @ 14 kHz; Pin 1 is @ 7 kHz; Pins 14, 23 are @ 3.5 kHz.

⁵Non-standard pin arrangement, or multiple supply pins; connect pins marked (*) without using a resistor.

Dynamic Burn-In Test Circuit Connections

| TYPE | OPEN | GROUND | 1/2 V _{DD} | V _{DD} | OSCILLATOR | |
|---------|------|----------|------------------------|-----------------|-------------------------|---------------|
| | | | | | 50 kHz | 25 kHz |
| CD40175 | — | 8 | 2,3,6,7,10,11 14,15 | 1,16 | 9 | 4,5,12,13 |
| CD40181 | — | 4-6,8,12 | 9-11,13-17 | 3,24 | 1,2,18-23 | 7 |
| CD40182 | — | 8 | 7,9-12 | 16 | 1-6,14,15 | 13 |
| CD40192 | — | 8,14 | 2,3,6,7,12,13 | 1,5,9-11,15,16 | 4 | — |
| CD40193 | — | 8,14 | 2,3,6,7,12,13 | 1,5,9-11,15,16 | 4 | — |
| CD40194 | — | 7,8,10 | 12-15 | 1,3-6,9,16 | 11 | 2 |
| CD40208 | — | 12 | 1,2,4-7,22,23 | 3,15,16,21,24 | 8,10,14,19,20 | 9,11,13,17,18 |
| CD40257 | — | 8,15 | 4,7,9,12 | 16 | 2,3,5,6,10,11, 13,14 | 1 |

Guide to Burn-In Delta Limits for Level /MS
CD400B-Series CMOS ICs

Delta Parameters

For the /MS level devices, certain parameters are data-logged and deltas are calculated from pre to post burn-in. These parameters are shown below.

| Critical Parameters | Symbols | Test Conditions | | | Delta (Δ) Limits |
|--|-----------------|--------------------|---------------------|---------------------|---------------------------|
| | | V _O (V) | V _{IN} (V) | V _{DD} (V) | |
| Quiescent Device Current Gates MSI-1 Types MSI-2 Types | I _{DD} | — | 0,20 | 20 | ± 0.1 μ A |
| | I _{DD} | — | 0,20 | 20 | ± 0.2 μ A |
| | I _{DD} | — | 0,20 | 20 | ± 1.0 μ A |
| Output Low (Sink) Current | I _{OL} | 0.4 | 0,5 | 5 | ± 20% of initial value |
| Output High (Source) Current | I _{OH} | 4.6 | 0,5 | 5 | ± 20% of initial value |
| Types with R _{ON} limits instead of I _{OL} and I _{OH} | R _{ON} | — | — | 10V | ± 20% of initial value |

High Reliability CD4000B-Series CMOS ICs

Leadless Chip Carrier Pinouts

The following table and diagrams show JEDEC standard pinout conversions from 14, 16, 22 and 24 pin leaded FP/DIL packages to 20 and 28 terminal leadless chip

carriers. Harris CD4000B-series products offered in leadless chip carriers are shown below.

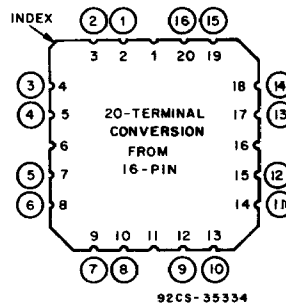
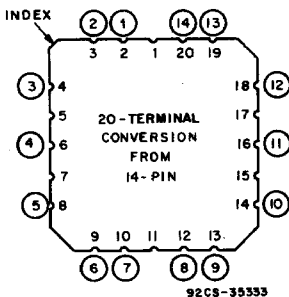
Pinout Conversion From Leaded Package to Leadless-Chip Carrier

| FP/DIL Pin | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |
|------------|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|
| Leadless | 2 | 3 | 4 | 6 | 8 | 9 | 10 | 12 | 13 | 14 | 16 | 18 | 19 | 20 | | | | | | | | | | | |
| Chip | 2 | 3 | 4 | 5 | 7 | 8 | 9 | 10 | 12 | 13 | 14 | 15 | 17 | 18 | 19 | 20 | | | | | | | | | |
| Carrier | 2 | 3 | 4 | 5 | 6 | 8 | 10 | 11 | 12 | 13 | 14 | 16 | 17 | 18 | 19 | 20 | 22 | 24 | 25 | 26 | 27 | 28 | | | |
| Terminal | 2 | 3 | 4 | 5 | 6 | 7 | 9 | 10 | 11 | 12 | 13 | 14 | 16 | 17 | 18 | 19 | 20 | 21 | 23 | 24 | 25 | 26 | 27 | 28 | |

CD4000B-Series Conversion Diagrams

Top Views Shown

20-Terminal Leadless-Chip Carriers



28-Terminal Leadless-Chip Carriers

