Signetics

Military Logic Products

54LS173
Flip-Flop

Quad D-Type Flip-Flop with 3-State Outputs

Product Specification

FEATURES

- **Edge-triggered D-type register**
- **Gated input enable for hold "do nothing" mode**
- **3-State output buffers**
- **Gated output enable control**
- **Pin compatible with the 8T10 and DM8551**

DESCRIPTION

The 54LS173 is a 4-bit parallel load register with clock enable control, 3-State buffered outputs and master reset. When the two Clock Enable ($\overline{E}_1$ and $\overline{E}_2$) inputs are Low, the data on the D inputs is loaded into the register synchronously with the Low-to-High Clock (CP) transition. When one or both $\overline{E}$ inputs are High one setup time before the Low-to-High clock transition, the register will retain the previous data. Data inputs and Clock Enable inputs are fully edge triggered and must be stable only one setup time before the Low-to-High clock transition.

The Master Reset (MR) is an active High asynchronous input. When the MR is High, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable ($\overline{OE}_1$ and $\overline{OE}_2$) inputs are Low, the data in the register is presented at the Q outputs. When one or both $\overline{OE}$ inputs is High, the outputs are forced to a High impedance "off" state. The 3-State output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

ORDERING INFORMATION

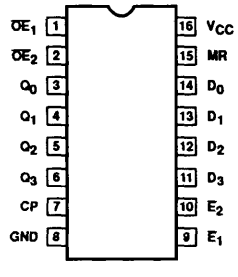
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS173/BEA
16-Pin Ceramic FlatPack	54LS173/BFA
16-Pin Ceramic LLCC	54LS173/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
All	Outputs	30LSUL

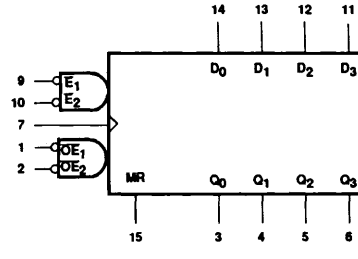
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



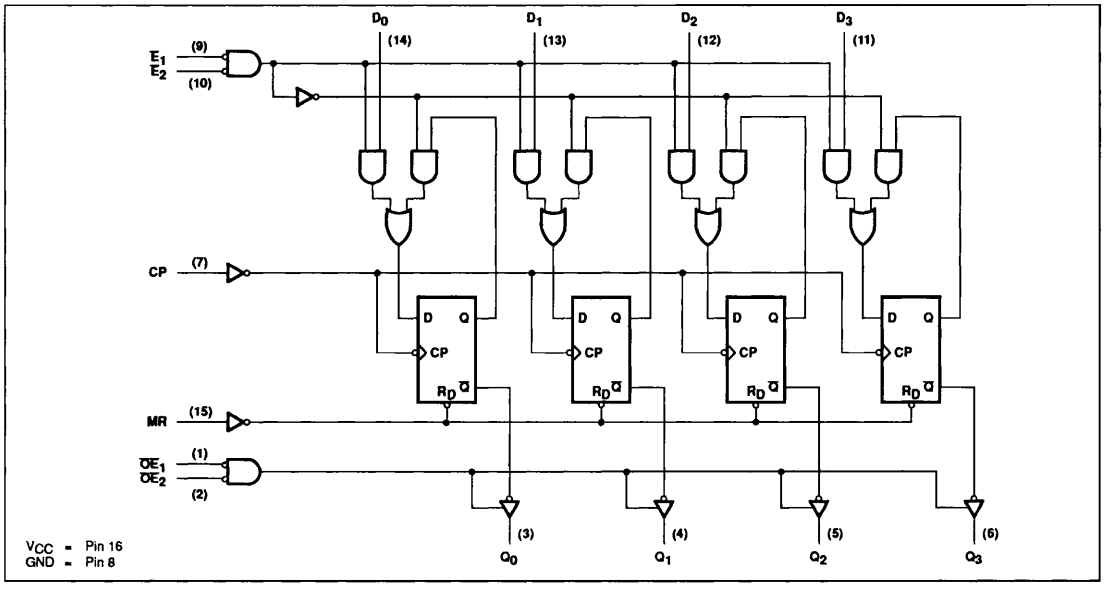
For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (no change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS
	Q_n (Register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0, Q_1, Q_2, Q_3
Read	L	L	L	L
	H	L	L	H
Disabled	X	H	X	(Z)
	X	X	H	(Z)

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the Low-to-High clock transition
X = Don't care
(Z) = High impedance "off" state
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.6	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.30	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-1.5	V
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			20	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.4V			-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		20	30	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		25 30	ns ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		35	ns
t_{PZH}	Output enable to High level	Waveform 2		23	ns
t_{PZL}	Output enable to Low level	Waveform 3		27	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		17	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		17	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		33	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		19	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W(CP)	Clock pulse width	Waveform 1	20		ns
t_W(MR)	MR pulse width	Waveform 4	20		ns
t_s(D)	Setup time, data to clock	Waveform 5	17		ns
t_h(D)	Hold time, data to clock	Waveform 5	0		ns
t_s(E)	Setup time, enable to clock	Waveform 5	35		ns
t_h(E)	Hold time, enable to clock	Waveform 5	0		ns
t_{rec}(MR)	Recovery time, Master Reset to clock	Waveform 4	17		ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

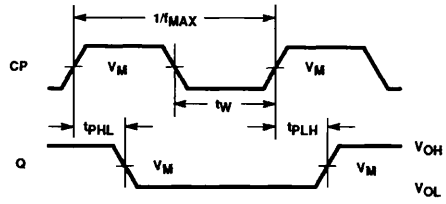
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		32 39	ns ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		45	ns
t_{PZH}	Output enable to High level	Waveform 2		30	ns
t_{PZL}	Output enable to Low level	Waveform 3		35	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		22	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		22	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		43	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		24	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C[6]

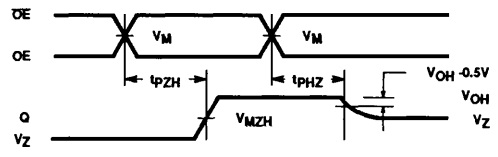
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W(CP)	Clock pulse width	Waveform 1	22		ns
t_W(MR)	MR pulse width	Waveform 4	20		ns
t_s(D)	Setup time, data to clock	Waveform 5	24		ns
t_h(D)	Hold time, data to clock	Waveform 5	5		ns
t_s(E)	Setup time, enable to clock	Waveform 5	35		ns
t_h(E)	Hold time, enable to clock	Waveform 5	0		ns
t_{rec}(MR)	Recovery time, Master Reset to clock	Waveform 4	17		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with MR grounded following momentary connection $\geq$ 4.0V, $\overline{OE}_2$, E_1, $\overline{E}_2$ and all Data inputs grounded, CP and $\overline{OE}_1 \geq$ 4.0V, and all outputs open.
5. Guaranteed by the 50pF limit, but not tested.
6. These parameters are guaranteed, but not tested.

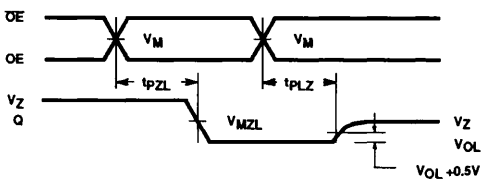
AC WAVEFORMS



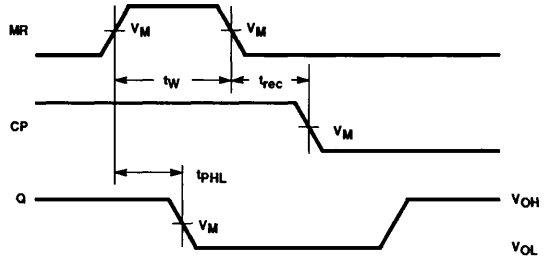
Waveform 1. Clock to Output Delays and Clock Pulse Width



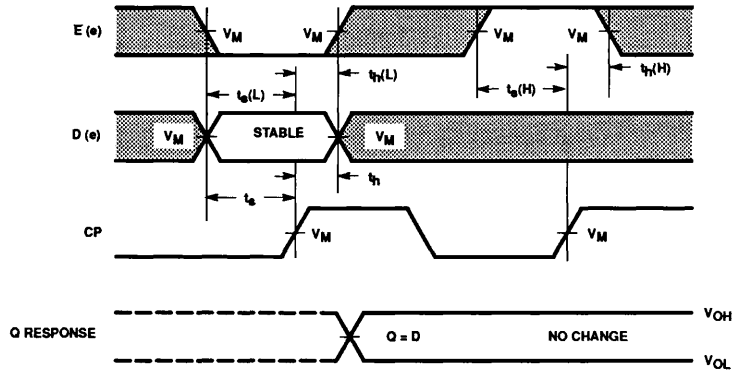
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level



Waveform 4. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

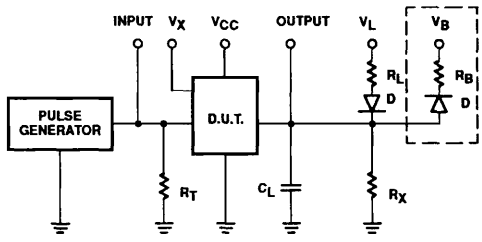


Waveform 5. Setup (t_s) and Hold (t_h) Times for Data (D) and Enable (E) Inputs

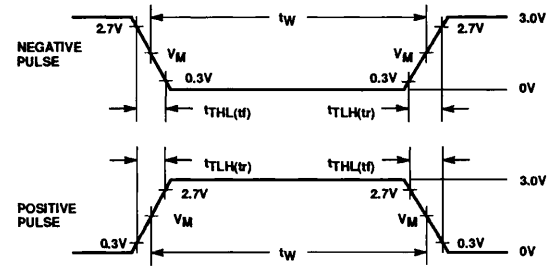
NOTE: The shaded areas indicate when the input is permitted to change for predictable output performances.

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.