TYPES SN54LS216, SN54LS217, SN54LS218, SN54LS316, SN54LS317, SN54LS318,
SN74LS216, SN74LS217, SN74LS218, SN74LS316, SN74LS317, SN74LS318

256-BIT RANDOM-ACCESS READ/WRITE MEMORIES

- Choice of 32 x 8 or 64 x 4 Organization
- Choice of 3-State or Open-Collector Outputs
- PNP Inputs and 12/24mA Outputs
- Full On-Chip Decoding and Fast Chip-Enable Simplify System Design

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

description

These monolithic TTL memories feature Schottky clamping for high performance and a fast chip-select access time to enhance decoding at the system level. A three-state-output version and an open-collector-output version are offered for all three basic configurations. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.

write cycle

Information to be stored in the memory is written into the selected address (A) location when the chip-select ($\overline{S}$) and the read-write (R/$\overline{W}$) inputs are low. While the read-write input is low, the memory outputs are off (three-state = Hi-Z, open-collector = high). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

read cycle

Information stored in the memory (see function table for input/output phase relationships) is available at the outputs when the read-write input is high and the chip-select input is low. When the chip-select input is high, the outputs are off.

FUNCTION TABLE

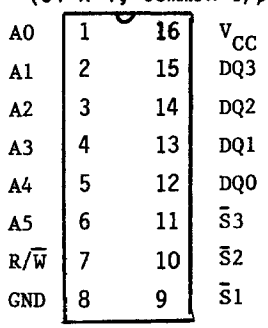
FUNCTION	INPUTS		OUTPUTS					
	CHIP SELECT	READ-WRITE	'LS216	'LS217	'LS218	'LS316	'LS317	'LS318
Write	L	L	Z	Z	Z	Off	Off	Off
Read	L	H	Data Entered	Data Entered	Data Entered	Data Entered	Data Entered	Data Entered
Inhibit	H	X	Z	Z	Z	Off	Off	Off

H = high level, L = low level, X = irrelevant, Z = high impedance

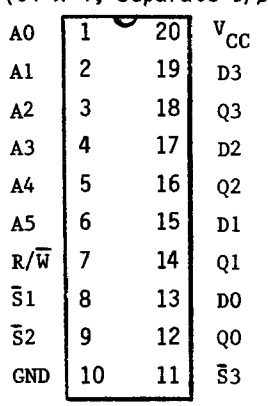
Please note the configuration of the 'LS217 and 'LS317 features separate input-output (DQ) pins for added convenience.

DEVICE TYPE	ORGANIZATION	COMMON I/Ø	OUTPUT TYPE
'LS216	64 words x 4 bits	YES	3-State
'LS217	64 words x 4 bits	NO	3-State
'LS218	32 words x 8 bits	YES	3-State
'LS316	64 words x 4 bits	YES	Open-Collector
'LS317	64 words x 4 bits	NO	Open-Collector
'LS318	32 words x 8 bits	YES	Open-Collector

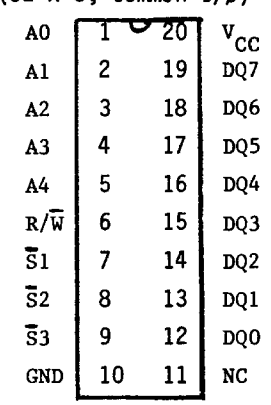
'LS216 3-State
'LS316 O. C.
(64 x 4, Common I/Ø)



'LS217 3-State
'LS317 O. C.
(64 x 4, Separate I/Ø)



'LS218 3-State
'LS318 O. C.
(32 x 8, Common I/Ø)



NC — No internal connection