Multistandard Encoder

1. Introduction

The MSE 3000 is a multistandard encoder implemented in CMOS technology. It delivers an analog composite video signal or an S–VHS signal (chroma and luma separated) which can be fed directly into a video input (e.g. SCART) of a connected device. The video mode of this signal can be PAL, NTSC or SECAM. The input signals are delivered from a signal source in components. The signal source can be one of the video processors of the DIGIT 2000 system (e.g. VPU, SPU, DMA) or other digital systems (for example computers). The main features of the MSE 3000 are:

- encoding of component signals (Y, U, V) to composite video or S–VHS signals in PAL/NTSC/SECAM standard
- analog output signals 1.25 V_{pp} at 75 Ohm
- large frequency range (13 to 26 MHz)
- very flexible due to adjustments via IM bus.
- usable in the DIGIT 2000 4:1:1 system and in 4:2:2 systems (D2–MAC or synthetic signals)

2. Functional Description

In the following, the functions of the MSE 3000 will be described. The descriptions refer to the block diagram, figure 2–1.

2.1. Chroma Input/Output

There are 8 chroma input bits. The lower 4 bits are used for the 4:1:1 input signal. This is the signal delivered from the VPU, SPU or VSP of the DIGIT 2000 system. The multiplex sequence starts with R–Y (low nibble). The following samples are R–Y (high nibble), B–Y (low nibble) and B–Y (high nibble). The synchronization pulses for the color demultiplexer (during vertical flyback) shows the start of this sequence. A synchronization with the horizontal pulses is only possible in the 4:2:2 mode. The delay between 4:1:1 input and 4:1:1 output is a multiple of 4 clock periods. There is one interpolation filter in this path. The transfer characteristics for different clock frequencies are shown in figure 2–2.

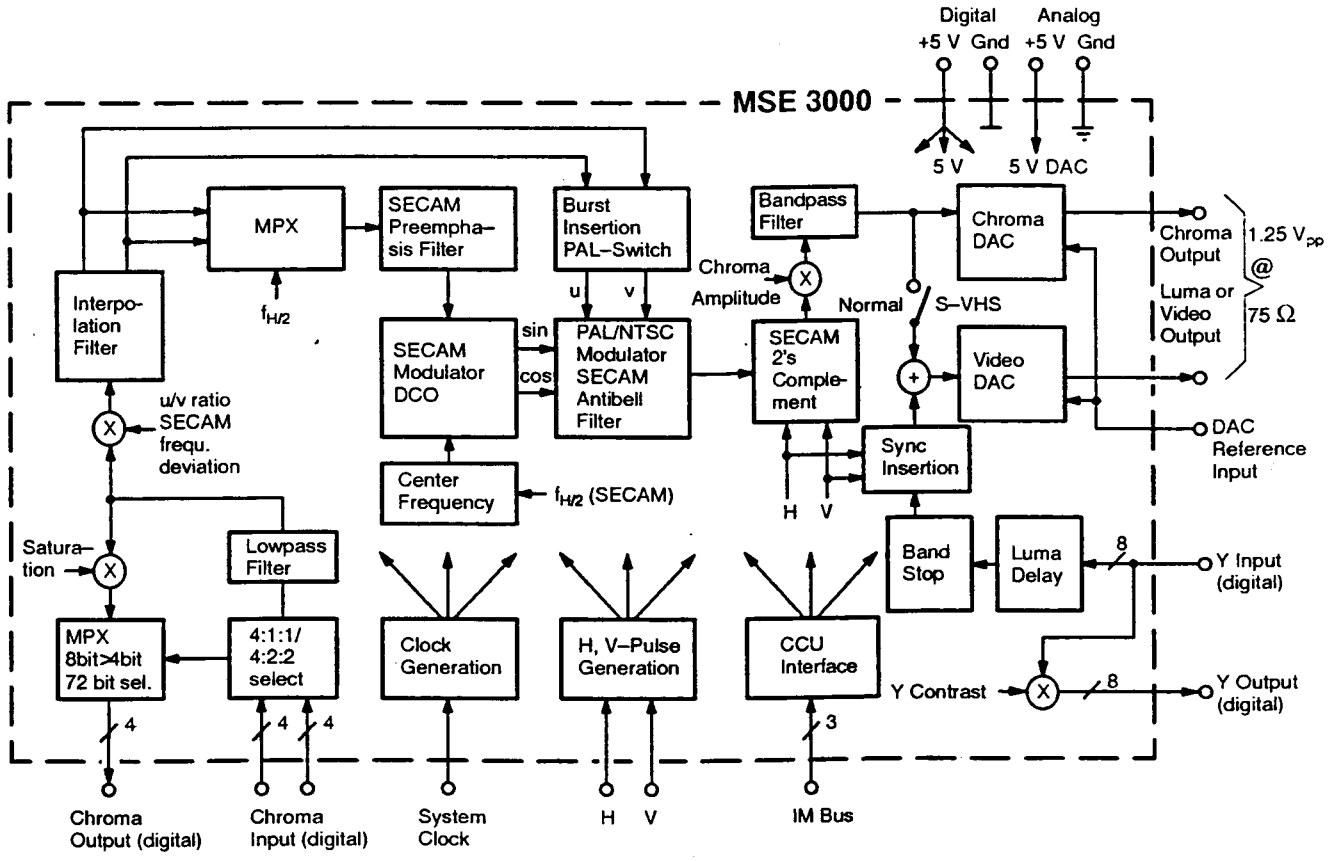


Fig. 2–1: Block diagram

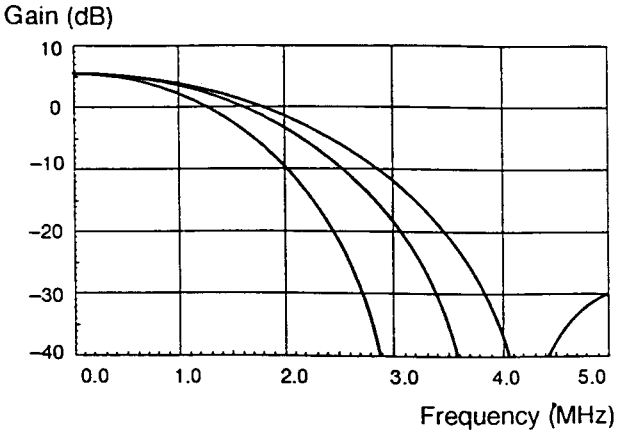


Fig. 2–2: Chroma 4:1:1 Input (fixed filters)
f_c = 14.32, 17.73, 20.25 MHz

For a 4:2:2 system all 8 bits are used for the input signal. In this case, R–Y and B–Y are multiplexed. One fixed and one adjustable lowpass filter can reduce the bandwidth. The synchronization of the demultiplexer can be done during vertical flyback (as in 4:1:1 mode) or with the horizontal pulse. If synchronization during vertical flyback is used, the 4:1:1 chroma output delivers a lowpass–filtered signal and the delay between 4:2:2 input and 4:1:1 output is a multiple of 2 clocks. The synchronization phase can be inverted by software. The transfer functions of the lowpass filters for different clock frequencies and different peaking adjustments are shown in figure 2–3.

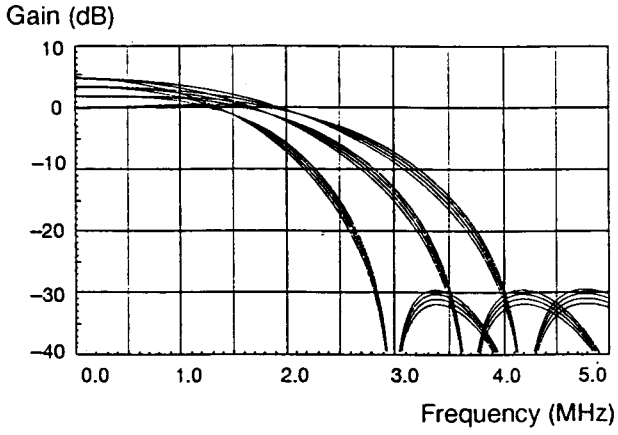


Fig. 2–3: Chroma 4:2:2 input
f_c = 14.32, 17.73, 20.25 MHz

2.2. PAL/NTSC Burst Insertion

During an internally generated color key pulse the color difference signals are replaced by the burst amplitude. The adjusted value will be inserted into the B–Y channel and inverted (PAL only) into the R–Y channel. Therefore the burst amplitude has to be negative. A positive value can be used for test purposes.

2.3. PAL/NTSC Modulator

The modulator for PAL and NTSC has inputs for R–Y, B–Y, sine and cosine of the color carrier. The B–Y signal is multiplied with the sine and the B–Y signal is multiplied with the cosine. The total gain of the modulator is 1 and can be adjusted with the C_GAIN value. The maximum resolution of the color carrier is eight bit.

2.4. SECAM Preemphasis

The SECAM preemphasis filter is a recursive filter with two coefficients. The gain of the color difference signals has to be adjusted in front of the interpolation filter. A typical amplitude and group delay transfer characteristic is shown in figure 2–4.

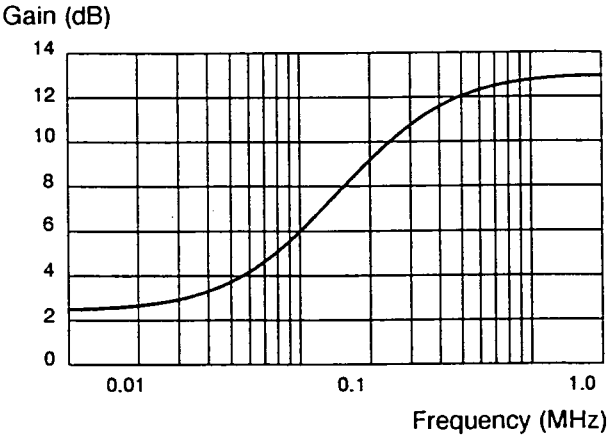
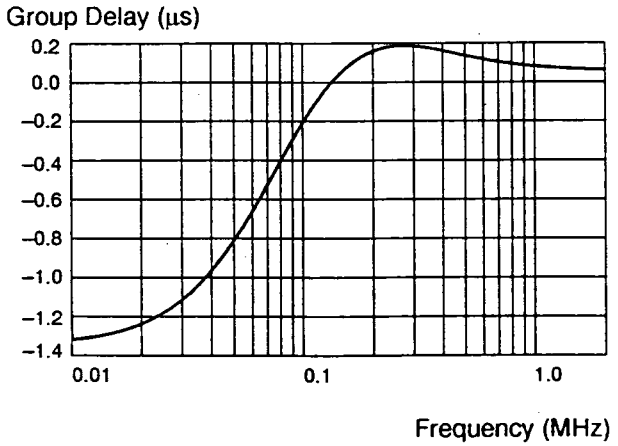


Fig. 2–4: Preemphasis filter



2.5. SECAM Modulator

The color carrier generator is an accumulator with a word length of 24 bit. The output sawtooth signal reads out a color lookup table with a sine and cosine function. The input of the accumulator gets the value for the center frequency plus the color difference signal in line multiplex.

The values for the center frequencies and the limits can be adjusted by software. In SECAM mode the generator starts each line with the same phase.

2.6. SECAM Antibell Filter

The SECAM antibell filter is a transversal filter with two coefficients. The correct center frequency can be adjusted in a clock frequency range of 13 to 26 MHz. The typical amplitude and group delay transfer characteristic is shown in figure 2–5.

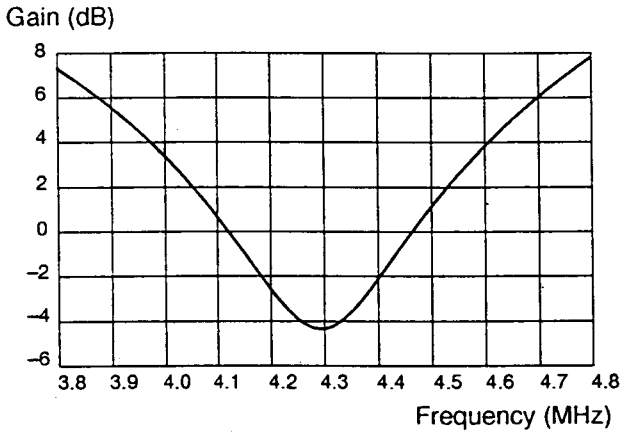
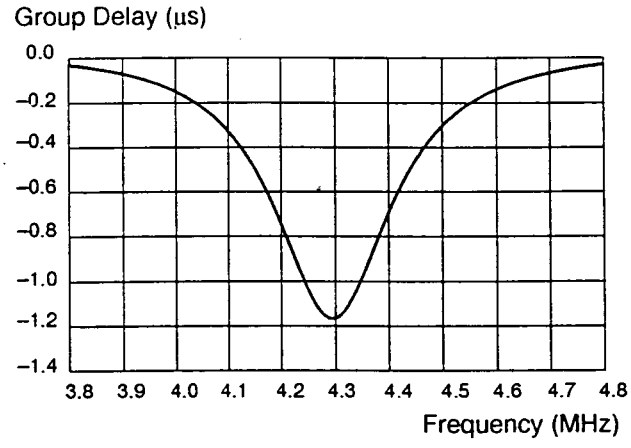


Fig. 2–5: Antibell filter



2.7. SECAM 2's Complement

This stage inverts the color subcarrier in the SECAM mode in the following sequence: 1 line non–inverted, 2 lines inverted. At each second field an additional inversion occurs. The phase of the color subcarrier at the output of the frequency modulator starts at each horizontal line with the same value.

2.8. Chroma Bandpass Filter

The chroma bandpass is a transversal filter structure. It consists of five parts. The first part can be switched to one or two variable zeroes or to neutral. The other four parts are zeroes, switchable to zero or fs/2 or neutral. A typical transfer characteristic with two zeroes each at zero and fs/2 and one zero at fs/4 and 3fs/4 is shown in figure 2–6.

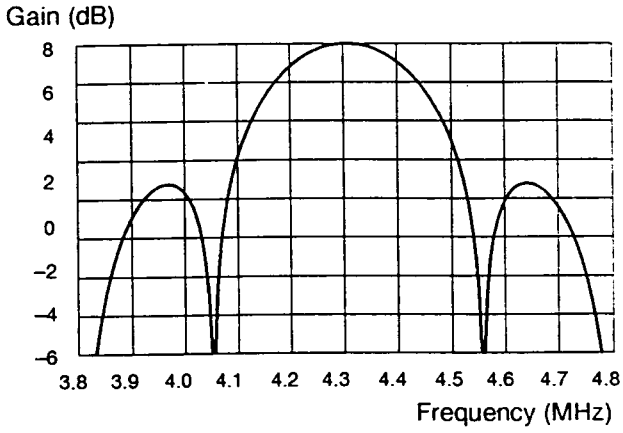


Fig. 2–6: Chroma bandpass filter

2.9. D/A Converters

There are two D/A–converters with 9–bit resolution. One of them produces the analog color subcarrier. The other one delivers either the analog luminance signal, sync included, or the composite video signal. The outputs are current outputs and need an external 75 Ω load resistor. With an additional load of 75 Ω, the output voltage is approx. 1.3 V_{pp}. A recommended lowpass filter is shown in the application, see Fig. 4–1.The output voltage can be varied by adjusting the reference current. The outputs are short–circuit protected.

2.10. Luma Input/Output

The luma delay compensates the processing delay in the chroma channel. It can be adjusted between 10 and 57 clocks. The bandstop filter (color carrier trap) produces an additional delay of approx. 15 clocks (depends on filter settings). The same delay is used for the composite sync signal which has an additional adjustable delay (see sync insertion).

2.11. Color Carrier Trap

The color carrier trap is a band stop filter in the luma channel. It consists of 4 parts. Two zeroes at fs/2 can separately be switched on or off. A single variable zero can be moved between 0 and fs/2. The fourth part is a peaking filter for a better transfer characteristic in the higher luma frequency. A typical transfer characteristic

is shown in figure 2–7. There are two zeroes at fs/2 and one zero at 4.43 MHz and peaking off and on.

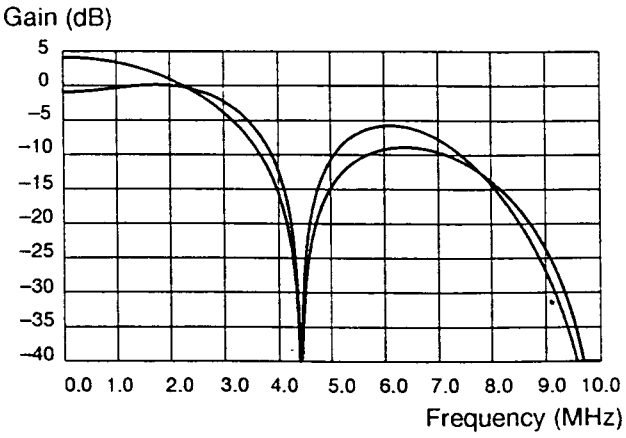


Fig. 2–7: Color carrier trap

2.12. Hsync/Vsync Generation and Insertion

The generation of the horizontal sync pulses starts with the low transition of the signal at pin 6. This pulse can have three different forms:

a) general horizontal sync pulse
b) skew data pulse train coming from the DPU in the DIGIT 2000 system
c) composite sync (e.g. from the D2–MAC decoder)

First, a trigger pulse is generated and starts a programmable down counter for the generation of horizontal sync. The output pulse of the counter is filtered to get a sync pulse with a rise and fall time of approx. 100 ns at 20 MHz clock frequency.

In case b) where skew data are used, a phase shifter shifts the phase of the horizontal sync pulse by a value between 0/31 and 31/32 of a clock period according to the skew data.

The delayed pulse from the counter triggers a 2H generator. This generator doubles the horizontal frequency. With this signal the vertical sync input (pin 33) is synchronized. The synchronized vertical pulse will be delayed by a programmable delay and triggers a pulse generator which produces a pulse with a duration of three horizontal lines.

The insertion of the sync pulses is made after the luminance gain adjustment, directly in front of the D/A–converter. Because the range of the converter is 9 bit, a value of 124 is added to the luma signal during the active line. During the sync pulse time, a value of zero is added. This produces a low impulse with the amplitude of approx. 25 % of the D/A converter range.

2.13. CCU Interface/IM Bus

The CCU interface has two main addresses: address 168 is used for the selection of the different modes, address 169 is used for parameters, testbits etc. with a subaddress of 6 bit (bit 0 to 5) and data of 8 bit (bit 8 to 15). Both main addresses can only be written, not read. The IM bus consists of three lines for the signals Ident, Clock and Data. Ident and Clock are unidirectional, Data is bidirectional. The MSE uses only one direction. This means that data can only be written to the MSE, not read. The timing is shown in Fig. 3–10.

In the non–operative state the signals of all three lines are on high level. To start a transaction, the CCU (Central Control Unit) sets the Ident to low level, indicating an address transmission. The Clock signal is set to low level as well, to switch the first bit on the Data line. Then eight address bits are transmitted, beginning wih the LSB. Data takeover in the MSE occurs at the positive edge of the clock signal.

At the end of the address byte the Ident signal goes high, initiating the address comparison in the the connected circuits. In the addressed circuit (e.g. MSE) the IM bus interface switches over to Data read or write, depending on the address. Also depending on the address, the CCU now transmits sixteen clock pulses, and accordingly two bytes of data are written to or read from the addressed circuit, beginning with the LSB.

The completion of the bus transaction is signalled by a short low pulse of the Ident signal. This initiates the storing of the transferred data.

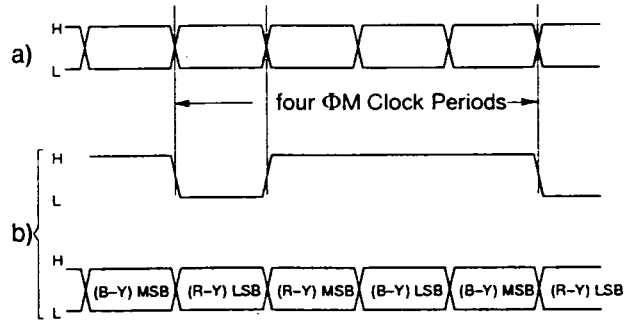


Fig. 2–8: Timing diagram of the multiplex data transfer of the chroma channel between the PVPU, SPU, DMA and MSE.

a) valid data out of the DMA 2281.

b) MUX data transfer of the chroma signals from DMA 2281 to MSE 3000, upper line: sync pulse from pin 30 DMA to pin 38 MSE during sync time in vertical blanking time.

3. Specifications

3.1. Outline Dimensions

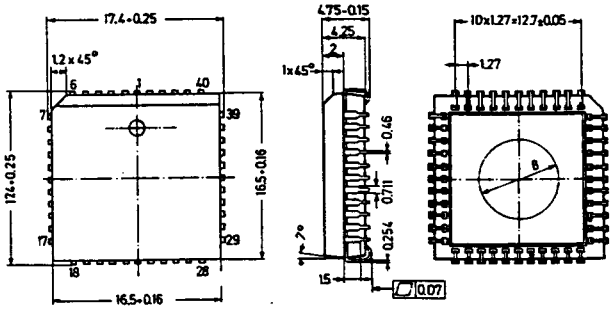


Fig. 3-1: MSE 3000 in 44-pin PLCC Package, Weight approx. 2.2 g, Dimensions in mm

3.2. Pin Connections

3.2.1. 44-Pin PLCC Package

1	C7 Chroma Input
2	Test Output (Ground in normal operation)
3	IM Bus Data
4	IM Bus Ident
5	IM Bus Clock
6	Horizontal Sync/ Composite Sync /Skew Data Input
7	L7 Luma Input
8	L6 Luma Input
9	L5 Luma Input
10	V_{SUP} (digital) +5V
11	ΦM Main Clock Input
12	Ground (digital)
13	L4 Luma Input
14	L3 Luma Input
15	L2 Luma Input
16	L1 Luma Input
17	L0 Luma Input
18	L7 Luma Output
19	L6 Luma Output
20	L5 Luma Output
21	L4 Luma Output
22	L3 Luma Output
23	L2 Luma Output
24	L1 Luma Output
25	L0 Luma Output
26	$\overline{\text{Reset}}$ Input
27	Reference Current D/A Converter
28	Internal Reference
29	Ground (analog)
30	Output Composite Video D/A Converter
31	V_{SUP} (analog) +5V
32	Output Chroma D/A Converter
33	Vertical Synchronization Input
34	C0 Chroma Output
35	C1 Chroma Output
36	C2 Chroma Output
37	C3 Chroma Output
38	C0 Chroma Input
39	C1 Chroma Input
40	C2 Chroma Input
41	C3 Chroma Input
42	C4 Chroma Input
43	C5 Chroma Input
44	C6 Chroma Input

3.3. Pin Descriptions

Pin 1 – C7 Chroma Input (Fig. 3–3)
See pin 38 to 44.

Pin 2 – Test Output
This pin is for test purposes only and has to be left vacant in normal operation.

Pin 3 to 5 – IM Bus (Fig. 3–5)
These are the connections of the MSE 3000 with the IM bus. All adjustments are done via this bus. The interface is for write only.

Pin 6 – Horizontal Synchronization (Fig. 3–5)

This input signal can exist in three forms:

- a) on a rectangular pulse, the high–low transition is used for starting the internal Hsync generation.
- b) if the skew data of the DPU in the DIGIT 2000 system are used, the internal Hsync generation starts after the first low–high transition after two low pulses (start of skew data). The skew data are necessary if the clock frequency is not an integer multiple of the horizontal frequency. They shift the generated Hsync pulse from 0/32 to 31/32 of a clock period.
- c) if the composite sync signal of the D2–MAC processors is used. In this case, the generation of internal Hsync pulses starts with the high–low transition of the incoming Hsync pulses. The end of timing generator has to be set to more than 32 µs and less than 64 µs because the Hsync input has to be disabled during h/2–pulses (equalizing pulses). The composite sync signal will be lowpass–filtered and added to the video signal. It is possible to switch between the different input signals via software.

Pin 7 to 9 – L7 to L5 Luma Input (Fig. 3–3)
These are the inputs for the digital luminance signal. It has to be in straight binary coded form (without sign).

Pin 10 – Digital Supply +5 V
This pin supplies all digital stages and has to be connected with the positive supply voltage.

Pin 11 – Clock Input (Fig. 3–4)
This is the input for the clock signal. The frequency can vary in the range of at least 13 to 26 MHz. In this range the SECAM filters can be set to the correct center frequencies.

Pin 12 – Digital Ground
This is the common ground connection of all digital stages and has to be connected with the ground of the power supply.

Pin 13 to 17 – L4 to L0 Luma Input (Fig. 3–3)
(see pin 7 to 9)

Pin 18 to 25 – L7 to L0 Luma Output (Fig. 3–2)
On this output you can get the digital luma signal in straight binary coded form. The amplitude can be adjusted with the coefficient for luma contrast.

Pin 26 – $\overline{\text{Reset}}$ (Fig. 3–6)
A low signal at this pin generates a reset. The low–high transition of this signal should come when the supply voltage is stable (power–on reset).

Pin 27 – Reference Current D/A Converter (Fig. 3–8)
This pin has to be connected to analog ground over a 500 Ohm resistor.

Pin 28 – Internal Reference (Fig. 3–8)
This pin should be connected to ground over a capacity of approx. 100 nF. The capacitor should be a type with low inductance and high resistance.

Pin 29 – Analog Ground
This is the ground pin for the D/A converters and has to be connected with the ground of the power supply.
Note: The layout of the PCB should take into consideration the need for a relatively noise–free ground.

Pin 30 – Output Composite Video D/A Converter (Fig. 3–7)
This output provides the composite video signal (in composite video mode) or the composite luma signal (in the S–VHS mode). The amplitude is 1.25 V_{pp} maximum at 75 Ohm. An additional 75 Ohm resistor has to be connected between output and analog ground because there is an internal current source only.

Pin 31 – Analog Supply +5 V
This is the supply voltage for the D/A converter and has to be connected with the positive supply voltage. Note: The layout of the PCB should take into consideration the need for a relatively noise–free supply.

Pin 32 – Output Chroma D/A Converter (Fig. 3–7)
This output provides the analog chroma signal. The amplitude is 1.25 V_{pp} maximum at 75 Ohm. An additional 75 Ohm resistor has to be connected between output and analog ground because there is an internal current source only.

Pin 33 – Vertical Synchronization (Fig. 3–5)
This input gets the signal for the vertical synchronization. From the high–low transition a Vsync pulse of 2.5 lines duration is generated after an adjustable delay. The length of the input pulse does not matter. This pulse is also necessary for internal control, if a composite sync is used at pin 6.

Pin 34 to 37 – C0 to C3 Chroma Output (Fig. 3–2)
These are the outputs for the digital chroma signal in 2's complement code. It has a halfbyte or nibble multiplex format (as in the DIGIT 2000 system). The amplitude for R–Y and B–Y can be adjusted separately with the coefficients for the color saturation.

Pin 38 to 44 – C0 to C6 Chroma Input (Fig. 3–3)
These are the inputs for the digital color difference signals. In the DIGIT 2000 system only 4 bits are transferred (4:1:1 mode, nibble–multiplex). Therefore you have to use pin 38 to 41. On 8 bit transfer (4:2:2, byte–multiplex) all 8 pins are used.

3.4. Pin Circuits

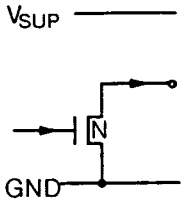


Fig. 3–2:
Output Pins 18 to 25, 34 to 37

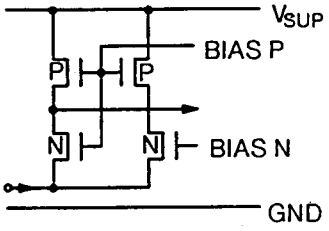


Fig. 3–3:
Input Pins 1, 7 to 9, 13 to 17, 38 to 44

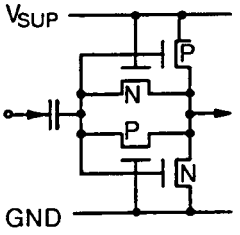


Fig. 3–4:
Input Pin 11

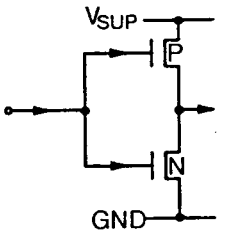


Fig. 3–5:
Input Pins 3 to 5, 6, 33

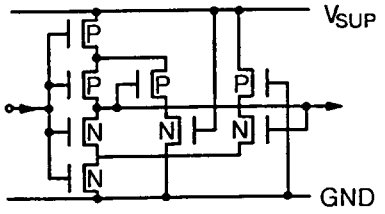


Fig. 3–6:
Input Pin 26

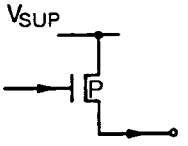


Fig. 3–7:
Output Pins 30, 32

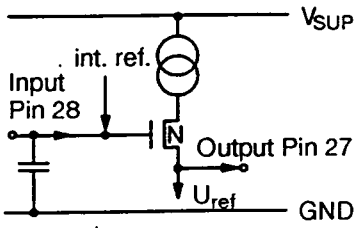


Fig. 3–8:
Input Pin 28 and Output Pin 27

3.5. Electrical Characteristics

3.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temp.	–	0	70	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP}	Supply Voltage	10, 31	–	6	V
V_I	Input Voltage, all Inputs		–0.3	V_{SUP}	V
V_{OLC}	Output Voltage Luma, Chroma, Test	2, 18–25, 34–37	–0.3	–	V
I_{OD}	Output Current Luma, Chroma, Test		–20	–	mA
V_{REF}	Output Voltage Internal Reference	27, 28	–	$\frac{V_{SUP}}{2}$	V
V_{AO}	Analog Output Voltage	30, 32	–	$\frac{V_{SUP}}{2}$	V
I_{OA}	Output Current Analog		–	40	mA

3.5.2. Recommended Operating Conditions at T = 0 to 65 °C, $f_{\Phi M}$ = 14.3 to 18.4 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUPD}	Digital Supply Voltage	10	4.75	5.0	5.25	V
V_{SUPA}	Analog Supply Voltage	31	4.75	5.0	5.25	V
$V_{\Phi MIDC}$	ΦM Clock Input D.C. Voltage	11	1.5	–	3.5	V
$V_{\Phi MIAC}$	ΦM Clock Input A.C. Voltage		0.8	–	2.5	V_{pp}
$f_{\Phi M}$	ΦM Clock Frequency		12	–	25	MHz
$\frac{t_{\Phi MIH}}{t_{\Phi MIL}}$	ΦM Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{\Phi MIHL}$	ΦM Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi M}}$	–
V_{REIL}	Reset Input Low Voltage	26	–	–	1.8	V
V_{REIH}	Reset Input High Voltage		2.6	–	–	V
t_{REIL}	Reset Input Low Time		1	–	–	µs
V_{LCIL}	Luma/Chroma Input Low Voltage	1, 7, 8, 9, 13, 14 to 17, 38 to 44	0.8	1.2	1.4	V
t_{LCIH}	Luma/Chroma Input Hold Time after Falling Edge of Master Clock		18	–	–	ns

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{LCIS}	Luma/Chroma Input Setup Time before Falling Edge of Master Clock	1, 7, 8, 9, 13, 14 to 17, 38 to 44	4	–	–	ns
V_{SIL}	Sync Input Low Voltage	6, 33	–	–	1.2	V
V_{SIH}	Sync Input High Voltage		1.8	–	–	V
I_{REF}	Reference Current for D/A Converters	27	4	–	5	mA
V_{IMIL}	IM Bus Input Low Voltage	3 to 5	–	–	1.2	V
V_{IMIH}	IM Bus Input High Voltage		1.8	–	–	V
$f_{\Phi IM}$	ΦIM IM Bus Clock Frequency		0.05	–	1000	kHz
t_{IM1}	IM Clock Input Delay Time after IM Bus Ident Input	5	0	–	–	–
t_{IM2}	IM Clock Input Low Pulse Time		500	–	–	ns
t_{IM3}	IM Clock Input High Pulse Time		500	–	–	ns
t_{IM4}	IM Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5}	IM Clock Input Hold Time after Ident Input High		500	–	–	ns
t_{IM6}	IM Clock Input Setup Time before Ident End–Pulse Input		1	–	–	µs
t_{IM7}	IM Bus Data Input Delay Time after IM Clock Input	3	0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before IM Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after IM Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End–Pulse Low Time	4	1	–	–	µs

3.5.3. Characteristics at T_A = 0 to 65 °C, V_{SUP} = 4.74 to 5.25 V, $f_{\Phi M}$ = 20.25 MHz

Symbol	Parameter	Pin. No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUPD}	Supply Current Digital	10	70	80	90	mA	
I_{SUPA}	Supply Current Analog	31	75	80	85	mA	
I_{LCIL}	Luma/Chroma Input Low Current	1, 7 to 9, 13, 14to 17, 38 to 44	1.3	2.5	4.1	mA	V_{LCIL} = 0.4 V
V_{LCOL}	Luma/Chroma Output Low Voltage	34 to 72, 2, 18 to 25	–	–	0.4	V	I_{LCOL} = 9.5 mA
I_{LCOH}	Luma/Chroma Output High Current		–	–	10	µA	
t_{LCOS}	Output Stable Time after Falling Edge of Master Clock		–	–	20	ns	
t_{LCOH}	Output Hold Time after Falling Edge of Master Clock		5	–	–	ns	
t_{LCOHL}	Luma/Chroma Output High to Low Transition Time		–	–	10	ns	C_L = 30 pF
V_{REFI}	Internal Reference Voltage	28	–	2.2	–	V	V_{SUPA} = 4.75 ... 5.25 V to be measured with $R_i \geq 1$ GΩ
V_{REF}	Reference Voltage	27	–	2.2	–	V	R_{REF} = 500 Ω
V_{AOUT}	Analog Output Voltage	30, 32	–	1.25	–	V_{pp}	R_L = 37.5 Ω
I_{ASH}	Analog Short Circuit Output Current		–	–	33	mA	R_L = 0

3.6. Waveforms and Frequency Responses

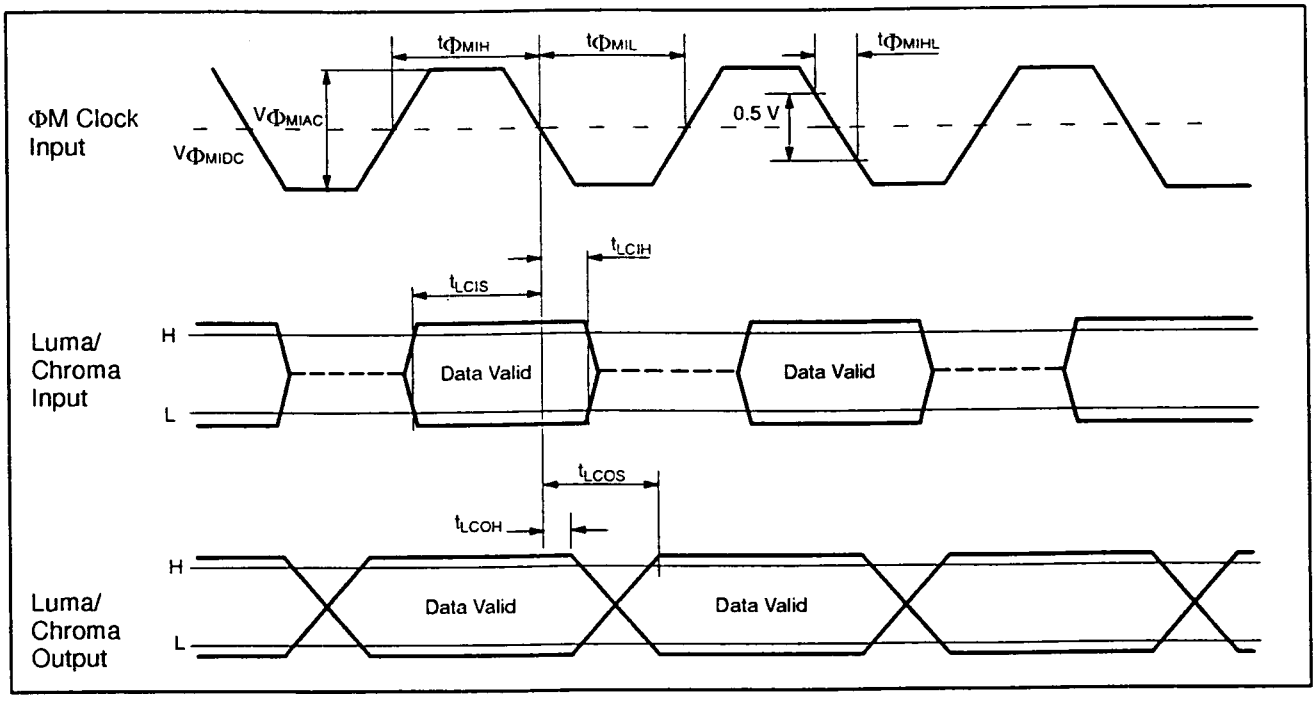


Fig. 3–9: Digital clock, luma and chroma waveforms

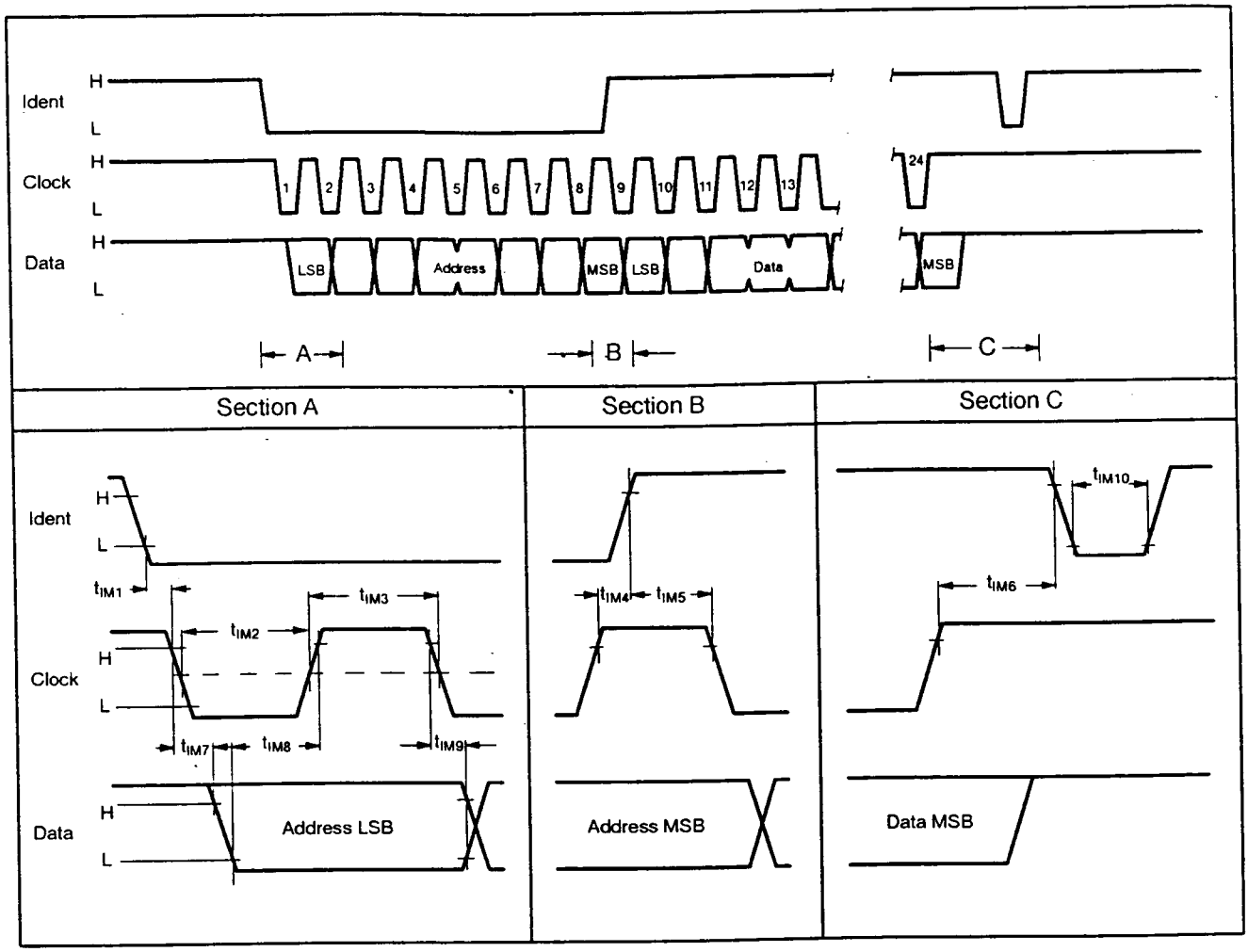


Fig. 3–10: IM bus waveforms

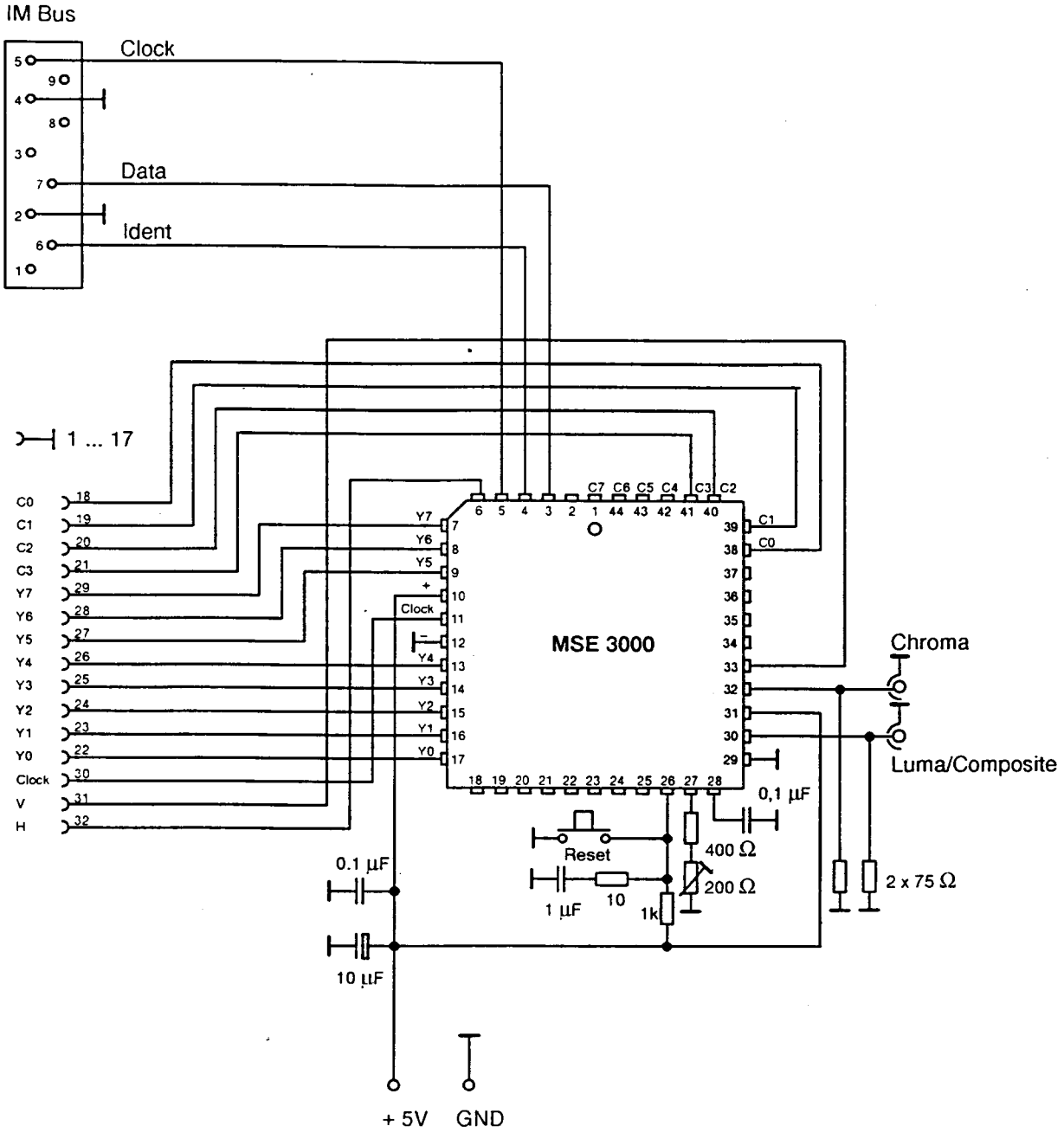


Fig. 3–11: Test circuit of MSE 3000

4. Programming

Table 4–1: Register addresses

IM Bus Address	IM Bus Data															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
168	SVHS	CSEXT	HSEXT	MUX411	LOS16	LOS32	NTSC	SECAM	HDMUX	OUTDIS						

SVHS 0 = Composite video and chroma output
1 = SVHS outputs

CSEXT 0 = Composite sync internally generated
1 = Composite sync externally generated

HSEXT 0 = Hsync from skew data of DPU
1 = Hsync from general horizontal pulse (low active)

MUX411 0 = Chroma input 8 bit (4:2:2)
Chroma input 4 bit (4:1:1)

LOS16 1 = Offset for luma input bit a

LOS32 1 = Offset for luma input bit b

NTSC 0 = Burst toggle on
1 = Burst toggle off

SECAM 0 = SECAM mode off (PAL or NTSC on)
1 = SECAM mode on

HDMUX 0 = Chroma demultiplexer synchronization during 72 bit in vertical blanking

1 = Chroma demultiplexer synchronization with horizontal pulse

OUTDIS 0 = Digital outputs enabled
1 = Digital outputs disabled (high impedance)

a	b	Offset
0	0	–32
0	1	–32
1	0	–16
1	1	0

Table 4–2: Data transfer to the MSE 3000

IM Bus Address	IM BUS DATA								
	MSE Data								MSE Sub–address
	15	14	13	12	11	10	9	8	0 ... 7
169	DCO Center Frequency for R–Y (Bit 16 ... 23)								0
	DCO Center Frequency for R–Y (Bit 8 ... 15)								1
	DCO Center Frequency for R–Y (Bit 0 ... 7)								2
	DCO Center Frequency for B–Y (Bit 16 ... 23)								3
	DCO Center Frequency for B–Y (Bit 8 ... 15)								4
	DCO Center Frequency for B–Y (Bit 0 ... 7)								5
	DCO Upper Frequency Limit for SECAM								6
	DCO Lower Frequency Limit for SECAM								7
	X	X	X	Chroma Gain Adjustment					8
	SECAM Antibell Filter Coefficient A								9
	SECAM Antibell Filter Coefficient B								10
	X	SECAM Preemphasis Filter Coefficient A							11
	X	X	SECAM Preemphasis Filter Coefficient B						12
	PAL/NTSC Color Burst Amplitude								13
	X	Chroma Demulti–plexer Phase	Chroma 4:2:2 Input Filter 1 = Peaking = 4/16 2 = Peaking = 3/16 4 = Peaking = 2/16 8 = Peaking = 1/16			0 = F2 on 1 = F2 off	0 = F1 on 1 = F1 off		14
	X	B–Y Saturation for Digital Outputs							15
	X	R–Y Saturation for Digital Outputs							16
	X	B–Y Gain							17
	X	R–Y Gain							18
	Luminance Blanking Start								19
	Luminance Blanking End								20

Table 4–2, continued

IM Bus Address	IM BUS DATA								
	MSE Data								MSE Sub–address
	15	14	13	12	11	10	9	8	0 ... 7
169	Horizontal Sync Start								21
	Horizontal Sync End								22
	Key Pulse Start								23
	Key Pulse End								24
	Timing Generator End								25
						Vertical Sync Delay			26
		Chroma Bandpass Filter Coefficient 1							27
		Chroma Bandpass Filter Coefficient 2							28
		Gain 5 0:Gain=1 1:Gain=0.5	Gain 4 0:Gain=1 1:Gain=0.5	Gain 3 0:Gain=1 1:Gain=0.5	Gain 2 0:Gain=1 1:Gain=0.5	Gain 1 0:Gain=1 1:Gain=0.5 2:Gain=0.25 3:Gain=0.125		Switch 1 0:1 Variable Zero 1:2 Variable Zeroes	29
	Sign 5	Switch 5	Sign 4	Switch 4	Sign 3	Switch 3	Sign 2	Switch 2	30
		Switch: 0: Filter on 1: Filter off			Sign: 0 = $1 + z^{-1}$ 1 = $1 - z^{-1}$				
		Luminance Contrast for Digital Outputs							31
	Switch 1 0 : Filter 1 off 1 : Filter 1 on	Color Carrier Trap Coefficient for Filter 1 (Variable Zero)							32
						Switch 4 0 = Peaking off 1 = Peaking on	Switch 3 0 : z^{-1} 1: 0.5 · $(1+z^{-1})$	Switch 2 0 = z^{-1} 1: 0.5 · $(1+z^{-1})$	33
			Luminance Gain						34
		Luminance Delay							35

Table 4–2, continued

IM Bus Address	IM Bus Data MSE Data								MSE Sub–address
	15	14	13	12	11	10	9	8	0 ... 7
169				Composite Sync Delay					36
	Test Register LSB								37
	Test Register MSB								38
	Chroma Blanking Start								39
									40
	Chroma Blanking End								41

4.1. Adjustment of the MSE 3000

For an easy adjustment of the MSE 3000, the CLIMB software can be used. The parameter names mentioned below refer to the CLIMB software.

4.1.1. Initialization (all modes)

Command name: INIT
This is a command in the CLIMB program. It initializes the MSE 3000 with the parameters set to the most recent values. Before this command, a hardware reset (power–on reset) should be done.

4.1.2. Clock Frequency (all modes)

Command name: SETCLOCK
With this command in the CLIMB program, all parameters will be loaded from the lookup table for the desired clock frequency (and the selected color mode). There are nine lookup tables for three clock frequencies (14.32 MHz, 17.73 MHz, 20.25 MHz) and three color modes.

4.1.3. Color Mode

Command name: SETMODE
With this command in the CLIMB program, all parameters will be loaded from the lookup table for the desired color mode (and the selected clock frequency). There are nine lookup tables for three color modes (NTSC, PAL, SECAM) and three clock frequencies.

4.1.4. Color Input (all modes)

Parameter names: CIN411, MUXVH, MUXPH
The color input can be selected as either 4:1:1 or 4:2:2. In the 4:1:1 mode, the synchronization of the color demultiplexer can be done with a sync signal during the vertical blanking interval (72 bit transfer in the DIGIT 2000 system). In the 4:2:2 mode, the synchronization of the color demultiplexer can also be done in the vertical mode or with the horizontal sync pulse. In this case, the sync phase can be switched between normal and inverted with the parameter MUXPH. The selection of vertical or horizontal mode can be done with the parameter MUXVH.

CIN411	0 → 4:2:2 color input 1 → 4:1:1 color input
MUXVH	0 → synchronization during vertical blanking 1 → synchronization with horizontal pulse (4:2:2 only)
MUXPH	0 → phase normal 1 → phase inverted

4.1.5. Output Selection (all modes)

Parameter name: SVHS
Pin 32 always delivers the chroma (color subcarrier) signal. On pin 30, you can select either luma or composite video signal.

SVHS	0 → composite video signal 1 → luminance signal

4.1.6. Chroma Lowpass 1 (4:1:1 and 4:2:2 Input)

Parameter names: none
This filter is not adjustable and consists of 3 parts. In 4:1:1 mode, the input signal for this filter is delivered from 4:1:1 chroma input to part 1 (Sample & Hold of 4:1:1 to 4:2:2 demultiplexer). The output of part 1 passes the signal to the input of part 2. The output of part 2 passes the signal to the chroma 4:1:1 output and to the input of part 3. Part 3 is an interpolation filter for the interpolation of the chroma signals to 4:4:4. The transfer functions are:

Part 1	$H(z) = 2 \cdot (1 + z^{-2})$ 4:1:1 only

Part 2	$H(z) = 0.125 \cdot (1 + 1.75 \cdot z^{-2} + z^{-4})$ 4:1:1 and 4:2:2

Part 3	$H(z) = 0.125 \cdot (1 + z^{-1})^3$ 4:1:1 and 4:2:2

4.1.7. Chroma Lowpass 2 (4:2:2 Input only)

Parameter names: CHRLP_F1, CHRLP_F2, CHRLP_P

This filter consists of 1 fixed part and 3 adjustable parts in series. Parts 1 to 3 are lowpass filters, part 4 is an adjustable peaking filter. In 4:2:2 mode, the output of this filter is fed to the input of part 2 of the chroma lowpass 2.

The transfer functions are:

Part 1		$H(z) = 0.5 \cdot (1 + z^{-4}) \cdot (1 + z^{-2})^2$
Part 2	F1 = 0	$H(z) = 0.5 \cdot (1 + z^{-4})$
	F1 = 1	$H(z) = z^{-4}$
Part 3	F2 = 0	$H(z) = 0.5 \cdot (1 + z^{-6})$
	F2 = 1	$H(z) = z^{-6}$
Part 4	P = 1	$H(z) = 4/16 \cdot (1 + z^{-12}) + Z^{-6}$
	P = 2	$H(z) = 3/16 \cdot (1 + z^{-12}) + Z^{-6}$
	P = 4	$H(z) = 2/16 \cdot (1 + z^{-12}) + Z^{-6}$
	P = 8	$H(z) = 1/16 \cdot (1 + z^{-12}) + Z^{-6}$

4.1.8. Chroma Preemphasis (SECAM only)

Parameter names: PREEM_A, _B
The preemphasis filter is used in SECAM mode only. It consists of a transversal path and a rec
ursive path. The input signals are –(R–Y) and +(B–Y) line sequential from the output of the chroma lowpass filter 1. The transfer function is:

$H(z) =$	$4 \cdot (1 - a \cdot z^{-4}) / (1 - b \cdot z^{-4})$	
where	A = 128 · a	range 0 ...127
	B = 64 · b	range 0 ... 63

4.1.9. Chroma Antibell (SECAM only)

Parameter names: BELL_A, _B
The antibell filter is used in the SECAM mode only. It is a transversal filter with the two coefficients A and B. The input signal is delivered from the SECAM frequency modulator and has an amplitude of ±127 steps. The transfer function is:

$H(z) =$	$8 \cdot (1 + a \cdot z^{-1} + b \cdot z^{-2})$	
where	A = 128 · a	range –128 ... +127
	B = 128 · b	range –128 ... +127

4.1.10. Chroma Bandpass (all modes)

Parameter names: CHRBP_C1, _C2, _S1, _S2, _S3, _S4, _S5, _G1, _G2, _G3, _G4, _G5
The Chroma Bandpass Filter consists of 5 parts:

Part 1:
One or two variable zeroes, adjustable with C1, C2, S1, G1. Switch S1 switches between one and two variable zeroes. The transfer functions are:

S1 = 0	$H(z) = 2^{-G1} \cdot (a + b \cdot z^{-1} + z^{-2})$	
where	C1 = 16 · a	range –63... +63
	C2 = 16 · b	range –63... +63
	G1 range 0...3	

S1 = 1	$H(z) = 2^{-(1+G1)} \cdot (1 + a \cdot z^{-1} + z^{-2}) \cdot (1 + b \cdot z^{-1} + z^{-2})$	
where	C1 = 16 · (a + b)	range –63... +63
	C2 = 16 · a · b +32	range –63... +63
	G1 range 0...3	

Part 2...5:
These are four identical filters, zeroes at f=0 or f= fs/2. Part 2 uses parameter S2 and G2. Part 3 uses S3 and G3. Part 4 uses S4 and G4. Part 5 uses S5 and G5. The transfer functions are:

Sn = 0	$H(z)= 2^{-Gn} \cdot (1 + z^{-1})$
Sn = 1	$H(z)= 2^{1-Gn}$
Sn = 2	$H(z)= 2^{-Gn} \cdot (1 - z^{-1})$
where	n = 2...5 Sn = 0...2 Gn = 0, 1

4.1.11. Color Carrier Frequency (all modes)

Parameter names: U_CCF_HB, _MB, _LB, V_CCF_HB, _MB, _LB

The adjustment of the color carrier frequency (or center frequency in SECAM mode) is controlled by 6 registers, of 8 bits each. The first three registers are for the B–Y center frequency (low, middle and high byte). The last three registers are for the R–Y center frequency. In PAL or NTSC mode, both register sets get the same information. The formula for the calculation of the value is:

$$Value = 2^{24} \cdot f_{subcarrier} / f_{clock}$$

Example:

f_c = 20.25 MHz, f_{sc} = 4.43361875 MHz
Value = 3673273.06
The rounded value is hexadecimal 380CB9
_HB = 38, _MB = 0C, _LB = B9

4.1.12. Limiter for Frequency Modulator (all modes)

Parameter names: UPLIM, LOLIM
In PAL and NTSC mode, The lower limit should be set to zero, the upper limit should be set to maximum. The correct adjustment is necessary in SECAM mode. The formula for the calculation of the value is:

$$Value = 2^{9} \cdot f_{limit} / f_{clock}$$

Example:

f_c = 20.25 MHz, f_{lim} = 4.75625 MHz
Value = 120.26; the rounded value is hexadecimal 78

4.1.13. Color Burst (NTSC/PAL only)

Parameter name: BURST
This is the value of the burst amplitude. The adjustment is relative to a maximum chroma amplitude of 1. This value's sign has to be negative. The positive sign can be used for test purposes. The formula for the calculation is:

Value =	–128 · Burst amplitude (NTSC)
range	–128...+127
Value =	–91 · Burst amplitude (PAL)
range	–128...+127

4.1.14. Luminance Offset (all modes)

Parameter name: Y_OFFSET
A negative luminance offset can be adjusted if the luminance input signal has an offset (e.g. in the DIGIT 2000 system).

Y_OFFSET	0 → Offset = –32
	1 → Offset = –32
	2 → Offset = –16
	3 → Offset = 0

4.1.15. Luminance Delay (all modes)

Parameter name: Y_DELAY
The delay of the luminance signal can be adjusted in steps of one clock period. The range is 0...47 clock periods. The adjustment is not completely binary. The weighting of bits is (from LSB to MSB): 1, 2, 4, 8, 16, 16.

Y_DELAY	Value = Delay · f_{clock}	0...31
	Value = Delay · f_{clock} + 16	32...47

4.1.16. Color Carrier Trap (all modes)

Parameter names: TRAP_C, _S1, _S2, _S3, _S4
This filter is in the luminance channel for the attenuation of the luminance signals in the area of the color carrier. It consists of 4 parts in series. Part 1 is an adjustable zero. Part 2 and part 3 are zeroes at fs/2 and part 4 is a peaking filter. The transfer functions are:

Part 1:		
S1 = 0	H(z) = 1	
S1 = 1	$H(z) = 1 + c \cdot z^{-1} + z^{-2}$	
	where C = 32 · c	range –64...+63

Part 2	
S2 = 0	$H(z) = 1$
S2 = 1	$H(z) = 0.5 \cdot (1 + z^{-1})$
Part 3	
S3 = 0	$H(z) = 1$
S3 = 1	$H(z) = 0.5 \cdot (1 + z^{-1})$
Part 4	
S4 = 0	$H(z) = z^{-2}$
S4 = 1	$H(z) = (1-0.25 \cdot z^{-2}) \cdot (-0.25 + z^{-2})$

4.1.17. Y/C Gain, Contrast and Saturation (all modes)

Parameter names: Y_GAIN, U_GAIN, V_GAIN, C_GAIN, Y_CONTR, U_SAT, V_SAT

Parameter names: Y_GAIN, U_GAIN, V_GAIN, C_GAIN, Y_CONTR, U_SAT, V_SAT

The luminance gain can be adjusted after the chroma trap. The gain for the color difference signals can be adjusted (separately for R–Y and B–Y) in front of the 4:4:4 interpolation filter. The gain for the color subcarrier can be adjusted in front of the chroma bandpass filter. The adjustments for luminance contrast and color saturation (separately for R–Y and B–Y) are operative for the digital luma and chroma outputs only. The formulae for the calculation of these values are:

Y_GAIN	Value = 64 · gain	range 0...63
U_GAIN	Value = 128 · gain	range 0...127
V_GAIN	Value = 128 · gain	range 0...127
C_GAIN	Value = 32 · gain	range 0...31
Y_CONTR	Value = 128 · contrast	range 0...127
U_SAT	Value = 128 · saturation	range 0...127
V_SAT	Value = 128 · saturation	range 0...127

4.1.18. Horizontal Sync Input (all modes)

Parameter name: HSYNC
The horizontal sync input can be switched between three input signals: horizontal sync, skew data (from DPU) or composite sync (from DMA).

HSYNC	0 →skew data
	1 →horizontal sync
	3 →composite sync

4.1.19. Blanking, Sync and Key Pulses (all modes)

Parameter names:

Y_BLANK_S, _E, C_BLANK_S, _E, HSYNC_S, _E, KEY_S, _E, TIMGEN_E, VSYNC_D, CSYNC_D

All these pulses are started with the low transition of the hsync input. The end of the timing generator (TIMGEN) stops the pulse generation. It must therefore have the highest value of all. While the timing generator is running, the hsync input is disabled. All pulses, except timing generator, vertical sync and composite sync, are adjustable within a step width of two clock periods, and have a range of 2 to 510 clock periods. The timing generator has a range of 4 to 1020 clock periods. The delay of the vertical sync pulse is adjustable in H/2 steps.

Y_BLANK	Value = $t_{delay} \cdot f_{clock} / 2$	range 1...255
C_BLANK	Value = $t_{delay} \cdot f_{clock} / 2$	range 1...255
HSYNC	Value = $t_{delay} \cdot f_{clock} / 2$	range 1...255
KEY	Value = $t_{delay} \cdot f_{clock} / 2$	range 1...255
TIMGEN	Value = $t_{delay} \cdot f_{clock} / 4$	range 1...255
CSYNC	Value = $t_{delay} \cdot f_{clock} / 2$	range 0...5 *
VSYNC	Value = $n_{H/2}$	range 0...7

* the delay is added to the luma delay and the weighting of the bits is not binary weighting: bit 0 =1, bit 1 = 1, bit 2 = 1, bit 3 = 2

4.1.20. Output Disable (all modes)

Parameter name: OUTDIS

This bit in the mode register can be used to disable all digital outputs. This is necessary if these outputs are directly connected to the outputs of another circuit (wired AND). If the bit is set, all outputs (open drain) have high impedance.

OUTDIS	0 → Outputs active
	1 → Outputs disabled (high Z)

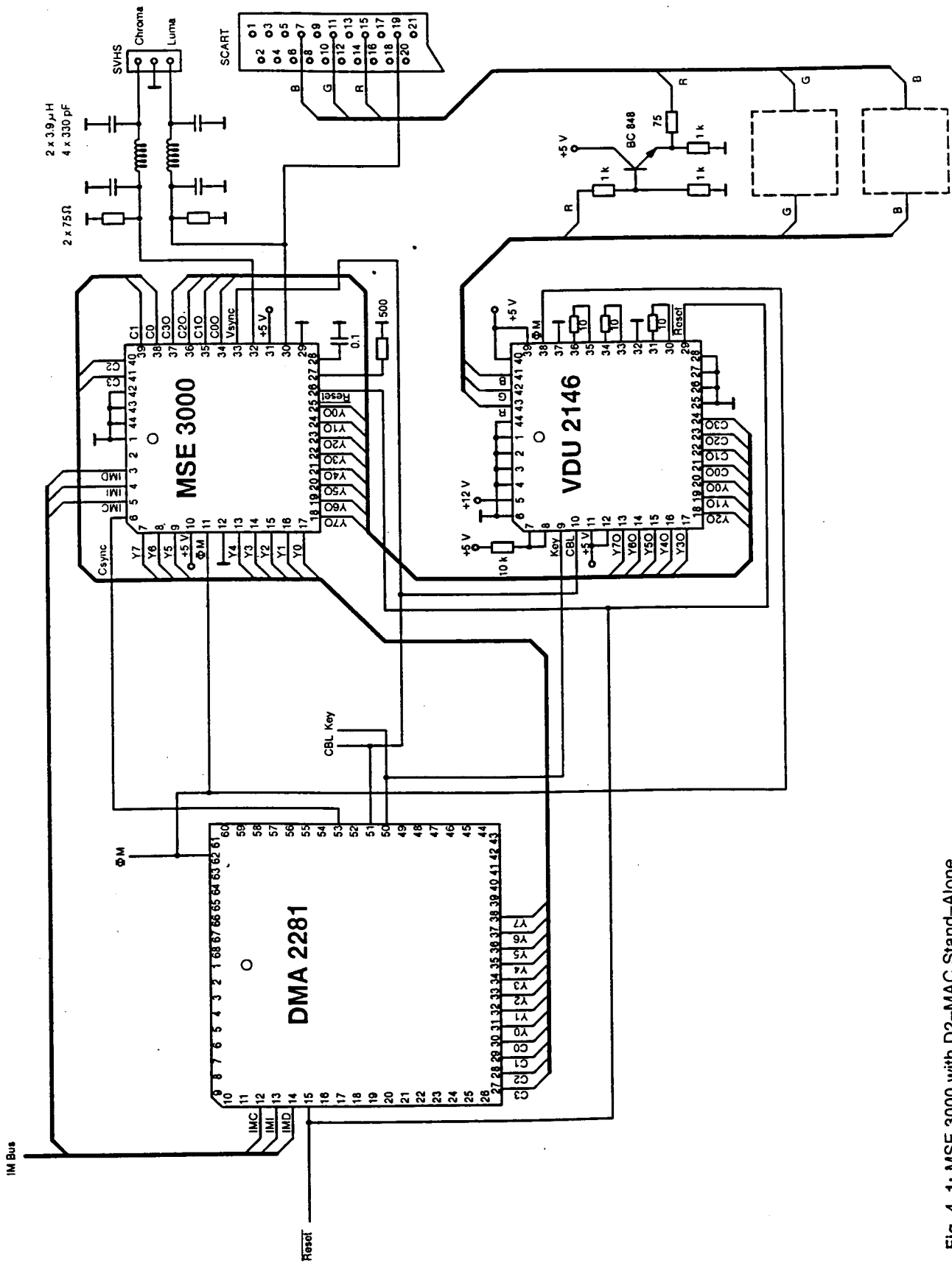


Fig. 4-1: MSE 3000 with D2-MAC Stand-Alone

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