# SONET/SDH/ATM QUAD OC-3 CLOCK RECOVERING TRANSCEIVER



## FEATURES

- **A complete single-chip 4 Channel Transmitter & Receiver**
- **Complies with Bellcore, ITU/CCITT and ANSI specifications**
- **Compatible with VLSI VNS67200 SUNI and IgT WAC-413-A ATM Quad-UNI Processor**
- **Supports clock recovery for 51.84 Mbit/s or 155.52 Mbit/s NRZ or NRZI data stream**
- **Supports clock generation for 51.84 Mbit/s OC/STS-1 or 155.52 Mbit/s OC/STS-3 SONET/SDH and ATM applications**
- **Operates from a single 12.96MHz or 19.44MHz crystal or oscillator**
- **100K ECL compatible I/O**
- **Single +5 volt power supply**
- **Typical power dissipation of only 3.8 watts**
- **Available in 128-pin thermally enhanced QFP package**

## DESCRIPTION

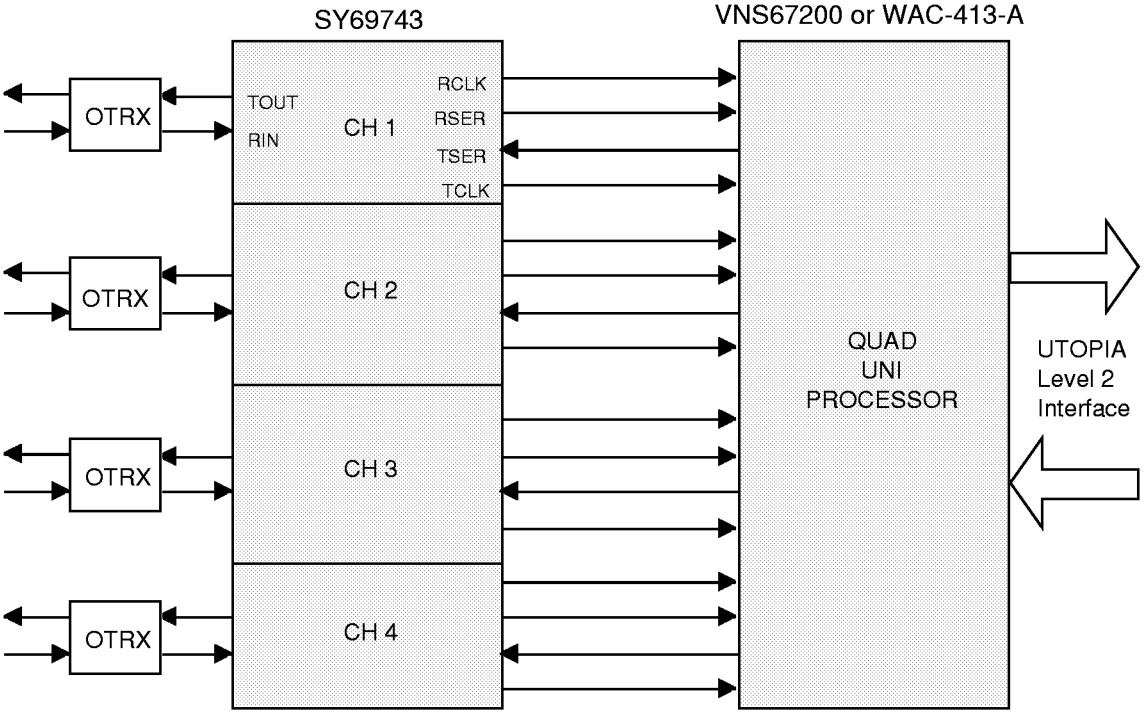
Synergy's SY69743 is the world's first integrated four-channel transmitter and receiver designed to provide clock recovery and generation for either 51.84Mbit/s OC/STS-1 or 155.52Mbit/s OC/STS-3 SONET/SDH and ATM applications.

On-chip clock generation is performed by a low-jitter phase-locked loop (PLL) allowing use of either a 12.96 or 19.44MHz crystal or oscillator as a reference. Clock recovery is performed by synchronizing the on-chip VCO directly to the input data stream.

Compliance with the bit-error rate requirements of the Bellcore ITU/CCITT and ANSI standards is ensured by Synergy's advanced PLL-technology and Positive-ECL (PECL) I/O.

Synergy's circuit design transceivers coupled with ASSET™ bipolar technology result in ultra-fast performance with low noise and lower power dissipation than similar competing products.

## BLOCK DIAGRAM

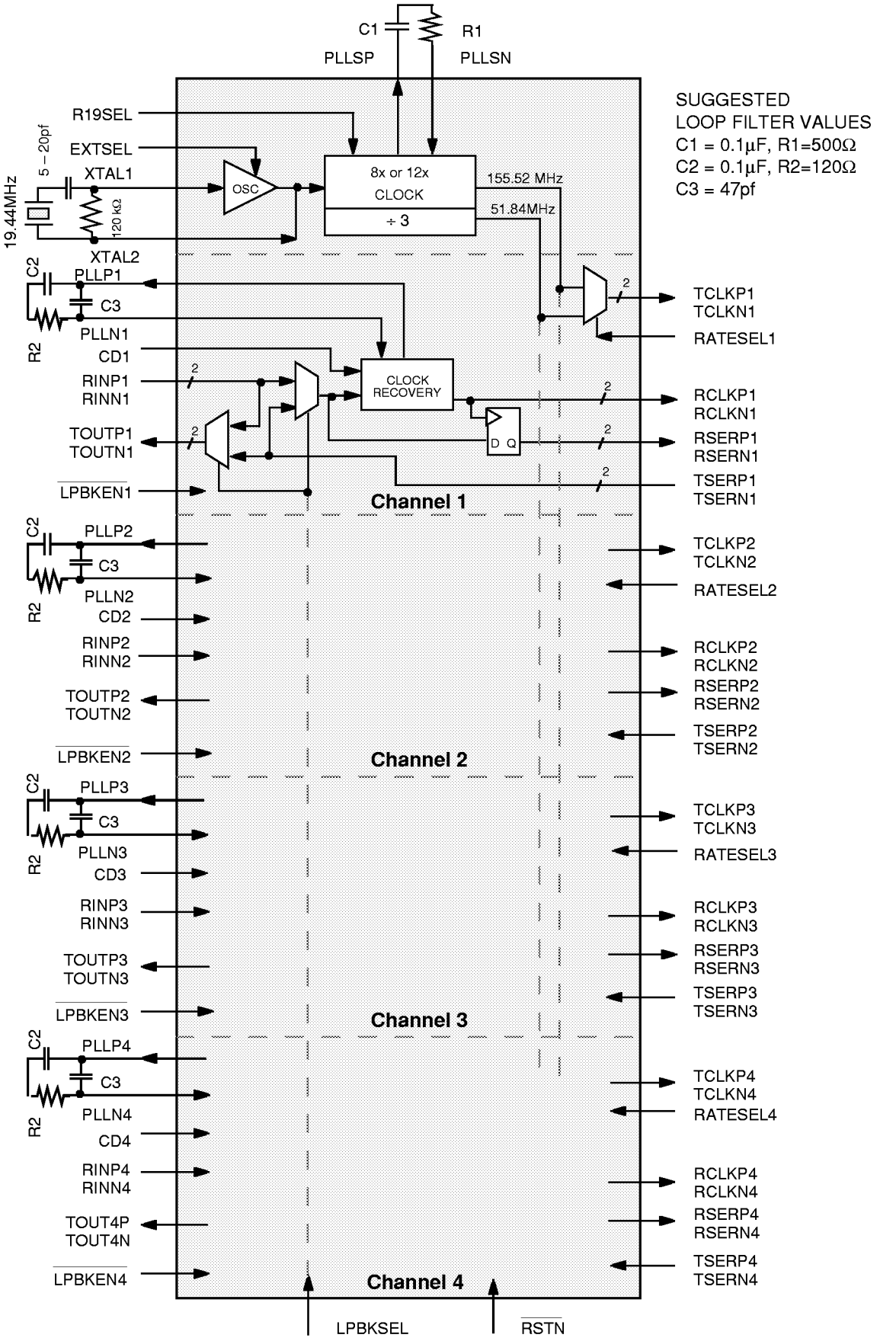




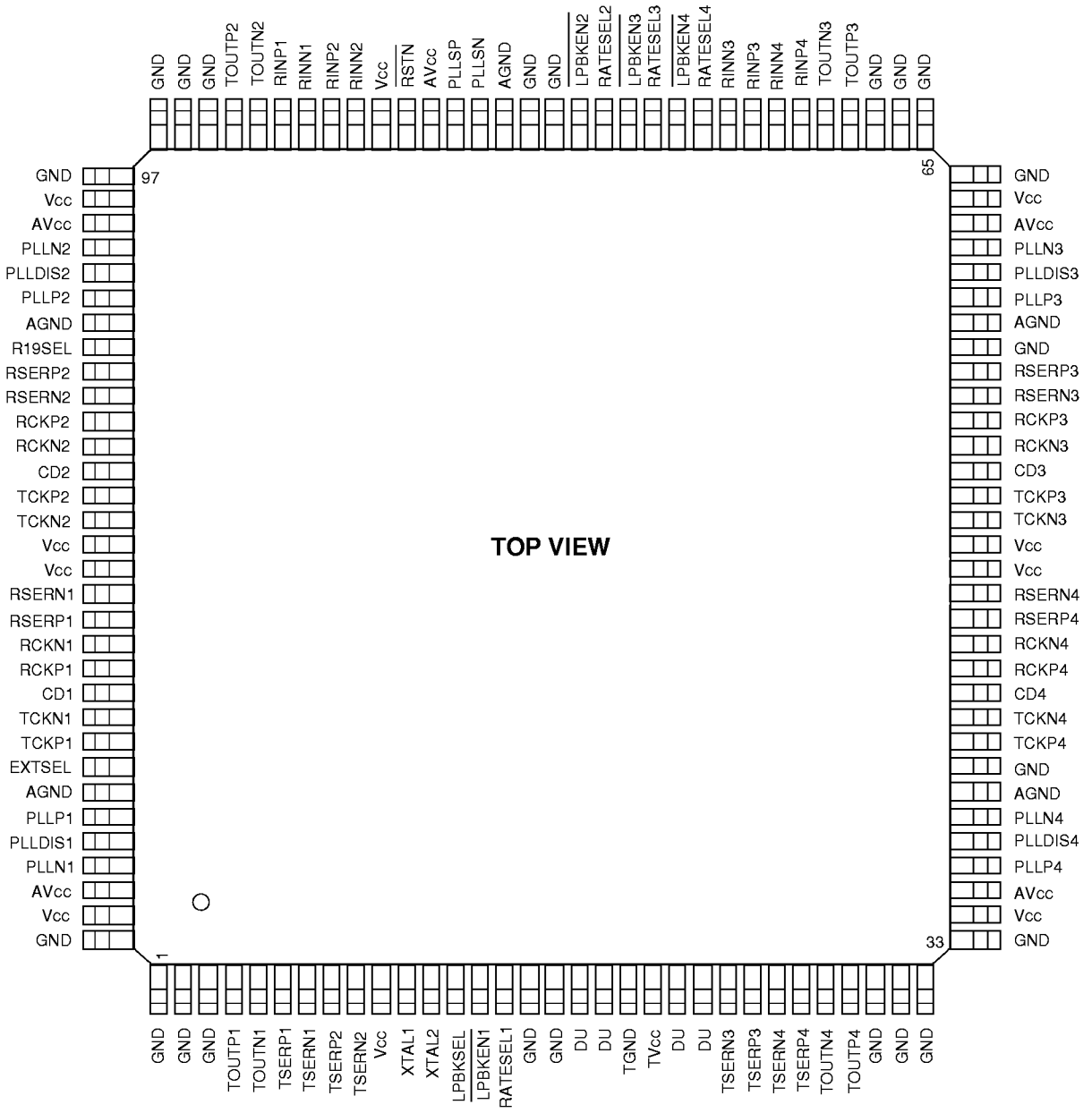



Rev.: K Amendment: /1
Issue Date: May, 1998

## FUNCTIONAL BLOCK DIAGRAM



## PINOUT




## PIN DESCRIPTIONS

### INPUTS

**RINP1/RINN1, ..., RINP4/RINN4 - Receive Input. Differential PECL.**

Differential serial inputs with built-in line receiver for each of the four receive channels. Clock is recovered from the transitions on these inputs.

**TSERP1/TSERN1, ..., TSERP4/TSERN4 - Transmit Serial Data. Differential PECL.**

Differential serial inputs with built-in line receiver for each of the four transmitter channels. The serial data to be transmitted is presented on these line receiver pins.

**LPBKSEL - Loopback Select. TTL.**

This input selects the loop path of either the receive data stream or the transmit data stream for the respective channel. It is used in conjunction with the LPBKEN (Loopback Enable) pins. When HIGH, the receive data stream is looped back out through the respective TOUTP/ TOUTN (Transmit Output) pins. When LOW, the data presented on the TSERP/TSERN (Transmit Serial Data) pins is looped back through the clock recovery circuit and is presented on the RSERP/RSERN (Recovered Serial Data) pins along with the recovered clock on the RCLKP/ RCLKN (Recovered Clock) pins.

## PIN DESCRIPTIONS (continued)

**$\overline{\text{LPBKEN1}}$, ..., $\overline{\text{LPBKEN4}}$ - Loopback Enable. TTL.- ACTIVE LOW**

These active LOW inputs enable the loopback mode for the respective channels. The loopback path is selected by the state of the LPBKSEL (Loopback Select) pin. When HIGH, the device is in normal receive/transmit mode.

**CD1, ..., CD4 - Carrier Detect. PECL.- ACTIVE HIGH**

These inputs control the recovery function of the receive PLL for each channel and can be driven by the carrier detect output from optical modules. When HIGH, the data on RINP,RINN (Receive Input) pins is recovered normally. When LOW, the internal transition detect circuitry and the clock recovery is disabled. When LOW, the Clock Recovery PLL no longer aligns to the RINP/RINN, but instead aligns with the internal equivalent of TCLKP/TCLKN. The RSERP (Recovered Serial Data) will remain LOW regardless of the signal level on the RINP/RINN (Receive Input) pins.

**RATESEL1, ..., RATESEL4 - Rate Select. TTL.**

These pins select the bit clock rate for the respective channel. When HIGH, a bit rate of 155.52MHz is selected and when LOW, a bit rate of 51.84MHz is selected.

**RSTN - Master Reset. TTL. - ACTIVE LOW**

This input should be used to initialize all internal circuitry upon power-up. Upon power-up this pin must held LOW for 1 millisecond to properly initialize the device.

**R19SEL - Frequency Select. TTL.**

This input selects between a 12.96MHz or a 19.44MHz input frequency. TTL LOW selects 12.96MHz; TTL HIGH selects 19.44MHz.

**EXTSEL - Oscillator Select. TTL.**

This input selects between using an external single-ended oscillator, or a crystal for the source of the 12.96MHz or 19.44MHz input frequency. TTL low selects crystal, TTL high selects a TTL oscillator source or PECL (differential) source.

**OUTPUTS**

**TOUTP1/TOUTN1, ..., TOUTP4,TOUTN4 - Transmit Output. Differential PECL.**

These pins are normally connected to the optical transmitter module of the respective channel. These represent the buffered version of the Transmit Serial Data.

**TCLKP1/TCLKN1,..., TCLKP4,TCLKN4 - Transmit Clock. Differential PECL.**

These pins provide the reference bit rate clock for the transmit processing device. The frequency of the output depends on the state of the RATESEL (Rate Select) pin.

**RCLKP1/RCLKN1, ..., RCLKP4/RCLKN4 - Recovered Clock. Differential PECL.**

These outputs represent the recovered clock from the RINP/RINN (Receive Input ) for the respective channel. It is used to sample the RSERP/RSERN (Recovered Serial Data).

**RSERP1/RSERN1, ..., RSERP4/RSERN4 - Recovered Serial Data. Differential PECL**

These outputs represent the recovered data from the input data stream. The recovered data is aligned with the Recovered Clock.

**OTHER**

**XTAL1, XTAL2.**

Positive and negative reference crystal inputs. A 12.96 MHz or 19.44MHz crystal or differential PECL oscillator with the associated capacitors connected to these pins provides the necessary 51.84MHz or 155.52MHz TCLKP/ TCLKN (Transmit clock) depending on the state of the RATESEL (Rate Select) pin for each channel. R19SEL selects the input frequency – 12.96MHz or 19.44MHz – and EXTSEL selects between crystal or oscillator input. If an oscillator is used, it should be connected to XTAL1 and XTAL2 should be connected to analog ground.

**PLLP1/PLLN1, ..., PLLP4/PLLN4 - Clock Recovery PLL Loop Filter.**

External loop filter connections for the clock recovery PLLs of the respective channels. A 0.1µf capacitor and a 120Ω resistor in series are recommended between these pins.

**PLLSP/PLLSN - Clock Synthesis PLL Loop Filter.**

External loop filter connections for the clock synthesis PLL. A 0.1µf capacitor and a 500Ω resistor in series are recommended between these pins.

**PLLDIS1, ..., PLLDIS4 - PLL Disable.**

Reserved for test purposes, for normal operation tie to low.

| | |
|---|---|
| **Vcc** | ECL +5V |
| **AVcc** | Analog +5V |
| **GND** | ECL Ground |
| **AGND** | Analog Ground |
| **TVcc** | TTL +5V |
| **TGND** | TTL Ground |
| **DU** | Do Not Use |

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{CC}$, $TV_{CC}$, $AV_{CC}$ | Power Supply (GND, TGND, AGND = 0V) | | 0 to +7 | V |
| $V_I$ | Input Voltage (GND, TGND, AGND = 0V) | | 0 to $V_{CC}$ | V |
| $I_{OUT}$ | Output Current | Continuous | 50 | mA |
| | | Surge | 100 | |
| $T_j$ | Junction Temperature Range | | 0 to +125 | °C |
| $T_{store}$ | Storage Temperature Range | | -65 to +150 | °C |

**NOTE:**

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

## PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = $TV_{CC}$ = $AV_{CC}$ = 4.75V to 5.25V; GND, TGND, AGND = 0V, $T_j$ = 0°C to +125°C (1)

| Symbol | Parameter | $T_j$ = 0° to +125°C | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ –1.075 | $V_{CC}$ –.955 | $V_{CC}$ –.830 | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ –1.860 | $V_{CC}$ –1.705 | $V_{CC}$ –1.570 | V |
| $V_{IH}$ | Input HIGH Voltage(2) | $V_{CC}$ –1.165 | — | $V_{CC}$ –.880 | V |
| $V_{IL}$ | Input LOW Voltage(2) | $V_{CC}$ –1.810 | — | $V_{CC}$ –1.475 | V |
| $I_{IL}$ | Input LOW Current | 0.5 | — | — | µA |

**NOTES:**

1. Equilibrium temperature
2. Forcing one input at a time. Apply $V_{IH}$ (max) or $V_{IL}$ (min) to all other inputs.

## TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = $TV_{CC}$ = $AV_{CC}$ = 4.75V to 5.25V; GND, TGND, AGND = 0V, $T_j$ = 0°C to +125°C

| Symbol | Parameter | Min. | Max. | Unit | Condition |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.4 | — | V | $I_{OH}$ = –2mA |
| $V_{OL}$ | Output LOW Voltage | — | 0.5 | V | $I_{OL}$ = 8mA |
| $I_{OS}$ | Output Short Circuit Current | –150 | –60 | mA | $V_{OUT}$ = Vcc |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | — | V | — |
| $V_{IL}$ | Input LOW Voltage | — | 0.8 | V | — |

## DC ELECTRICAL CHARACTERISTICS(1),(2),(3)

$V_{CC}$ = +5V ±5%; $V_{EE}$ = GND = 0V, $T_j$ = 0°C to +125°C

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{EE}$ | Internal Operating Current | — | 644 | — | mA | |
| $I_{OUT}$ | Termination Output Current | — | 11 | — | mA | 50Ω to Vcc -2, 50% duty cycle |

**NOTES:**

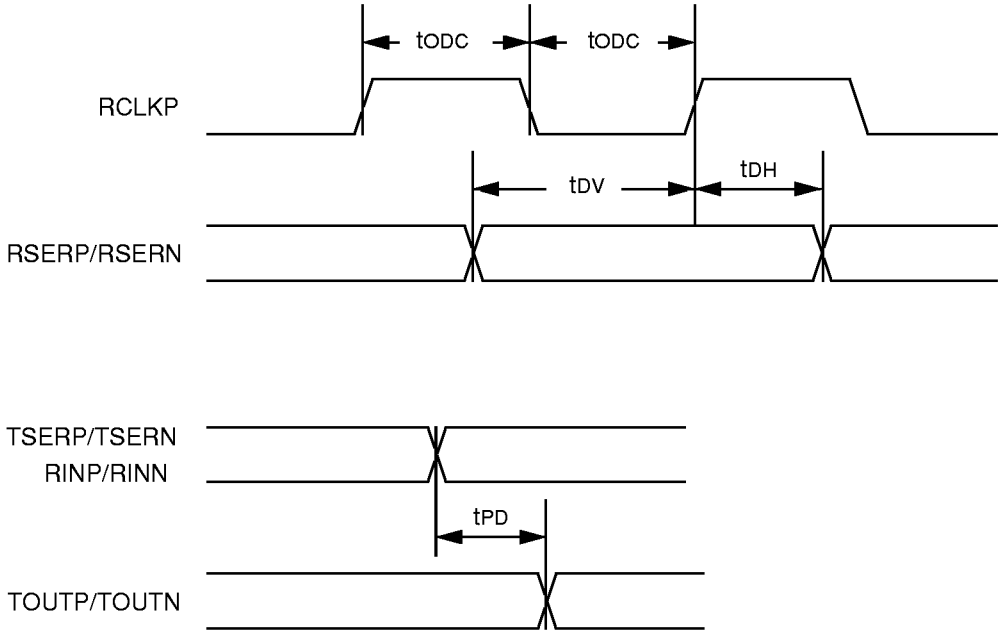
1. To calculate total power supply current into the $V_{CC}$ pins: $I_{CC}$ = (n * $I_{OUT}$); where n = number of ECL output pins used (ie, terminated).
2. To calculate total device power dissipation; $P_D$ = [$I_{EE}$ * ($V_{CC}$ - $V_{EE}$)] + [n * $I_{OUT}$ * 1.33](3).
3. Average ECL output voltage is calculated as $V_{OAVG}$ = ($V_{OH\,(max)}$ + $V_{OH(min)}$ + $V_{OL(max)}$ + $V_{OL(min)}$) /4 = 1.33V.

## AC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = $TV_{CC}$ = $AV_{CC}$ = 4.75V to 5.25V; GND, TGND, AGND = 0V, $T_j$ = 0°C to +125°C

| Parameter | Min. | Typ. | Max. | Units | Condition |
|---|---|---|---|---|---|
| VCO Center Frequency | — | 155.52 ±2% | — | MHz | Nominal |
| Acquisition Lock Time | — | — | 15 | µsec | |
| TTL Output Rise/Fall Time | — | — | 3 | ns | 10% t0 90% of amplitude, 30pF load |
| PECL Output Rise/Fall Time | — | — | 500 | ps | 10% to 90%, 50Ω load, 5pF cap |
| tDV - Data Valid | 3 | — | — | ns | 30pF load |
| tDH - Data Hold | 1 | — | — | ns | 30pF load |
| tODC - Output Clock Duty Cycle (TCLKP/N, RCLKP/N) | 45 | — | 55 | % OF UI | |
| TPD - Prop Delay (TSER to TOUT, RIN, TOUT) | 10.00 | — | — | ns | |

## TIMING WAVEFORMS




## PRODUCT ORDERING CODE

| Ordering Code | Package Type | Operating Range |
|---|---|---|
| SY69743QC | Q128-1 | Commercial |

# 128 LEAD METAL QUAD FLATPACK (Q128-1)