HARRIS Semiconductor

HC55171

5 REN Ringing SLIC for ISDN Modem/TA and WLL

July 1998

Features

- 5 REN Thru SLIC Ringing Capability to $75V_{PEAK}$
- Trapezoid, Square and Sinusoid Ringing Capability
- Bellcore Compliant Ringing Voltage Levels
- Lowest Component Count Trapezoidal Solution
- Single Additional +5V Supply
- Pin For Pin Compatible With HC5517
- DI Provides Latch-Up Immunity

Applications

- ISDN Internal/External Modems
- ISDN Terminal Adapters/Routers
- Wireless Local Loop Subscriber Terminals
- Cable Telephony Set-Top Boxes
- Digital Added Main Line
- Integrated LAN/PBX
- Related Literature
  - AN9606, Operation of the HC5517/171 Evaluation Board
  - AN9607, Impedance Matching Design Equations
  - AN9628, AC Voltage Gain
  - AN9608, Implementing Pulse Metering
  - AN9636, Implementing an Analog Port for ISDN Using the HC5517
  - AN549, The HC-5502X/4X Telephone Subscriber Line Interface Circuits (SLIC)

Description

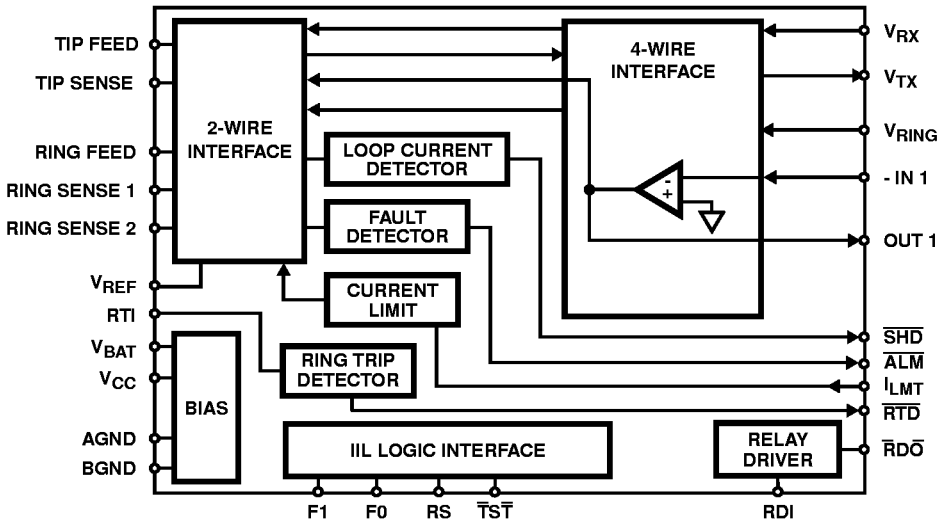
The HC55171 is backward compatible to the HC5517 with the added capability of driving 5 REN loads. The HC55171 is ideal for any modem or remote networking access application that requires plain old telephone service POTS, capability. The linear amplifier design allows a choice of Sinusoidal, Square wave or Trapezoidal ringing. The voltage feed architecture eliminates the need for a high current gain node achieving improved system noise immunity, an advantage in highly integrated systems.

The device is manufactured in a high voltage Dielectric Isolation (DI) process with an operating voltage range from -16V, for off-hook operation and -80V for ring signal injection. The DI process provides substrate latch up immunity, resulting in a robust system design.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HC55171IM	-40 to 85	28 Ld PLCC	N28.45
HC55171CM	0 to 75	28 Ld PLCC	N28.45
HC55171IB	-40 to 85	28 Ld SOIC	M28.3
HC55171CB	0 to 75	28 Ld SOIC	M28.3

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4323.4**

Absolute Maximum Ratings $T_A = 25^oC$

Maximum Supply Voltages
- V_{CC} . . . . . -0.5V to +7V
- V_{CC} - V_{BAT} 90V

Relay Drivers . . . . . -0.5V to +15V

Operating Conditions

Temperature Range
- HC55171IM, HC55171IB . . . . . -40^oC to 85^oC
- HC55171CM, HC55171CB . . . . . 0^oC to 75^oC

Relay Drivers . . . . . +5V to +12V

Positive Power Supply, V_{CC} . . . . . +5V ±5%

Negative Power Supply, V_{BAT} . . . . . -16V to -80V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PLCC	55
SOIC	70

Maximum Junction Temperature Plastic . . . . . 150^oC

Maximum Storage Temperature Range . . . . . -65^oC to 150^oC

Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC, PLCC - Lead Tips Only)

Die Characteristics

Transistor Count 224

Diode Count 28

Die Dimensions . . . . . 175 x 144

Substrate Potential . . . . . V_{BAT}

Process . . . . . Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, V_{BAT} = -24V, V_{CC} = +5V, AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RINGING TRANSMISSION PARAMETERS					
V_{RING} Input Impedance	(Note 2)	-	5.4	-	kΩ
4-Wire to 2-Wire Gain	V_{RING} to V_{T-R} (Note 2)	-	40	-	V/V
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 2)	-	108	-	kΩ
OUT1 Positive Output Voltage Swing	R_L = 10kΩ (Note 2)	+2.5	-	-	V
OUT1 Negative Output Voltage Swing	R_L = 10kΩ (Note 2)	-4.5	-	-	V
4-Wire Input Overload Level	300Hz to 3.4kHz R_L = 1200Ω, 600Ω Reference (Note 2)	-	+3.1	-	V_{PEAK}
2-Wire Return Loss	Matched for 600Ω, f = 300Hz (Note 2)	37	-	-	dB
	Matched for 600Ω, f = 1000Hz (Note 2)	40	-	-	dB
	Matched for 600Ω, f = 3400Hz (Note 2)	30	-	-	dB
2-Wire Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 300Hz to 3400Hz (Note 2)	58	63	-	dB
4-Wire Longitudinal Balance Off Hook	300Hz to 3400Hz (Note 2)	-	55	-	dB
Longitudinal Current Capability	I_{LINE} = 40mA, $T_A = 25^oC$ (Note 2)	-	40	-	mA_{RMS}
Insertion Loss, 2W-4W	0dBmO, 1kHz, Includes Tranhybrid Amp Gain = 3	-	±0.05	±0.2	dB
Insertion Loss, 4W-2W	0dBmO,1kHz	-	±0.05	±0.2	dB
Insertion Loss, 4W-4W	0dBmO, 1kHz, Includes Tranhybrid Amp Gain = 3	-	-	±0.25	dB
Frequency Response	300Hz to 3400Hz Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.06	dB

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, $V_{BAT} = -24V$, $V_{CC} = +5V$, AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Level Linearity	+3 to 0dBm, Referenced to -10dBm (Note 2)	-	-	±0.10	dB
	0 to -40dBm, Referenced to -10dBm (Note 2)	-	-	±0.12	dB
	-40 to -55dBm, Referenced to -10dBm (Note 2)	-	-	±0.30	dB
Absolute Delay, 2W-4W	300Hz to 3400Hz (Note 2)	-	-	1.0	µs
Absolute Delay, 4W-2W	300Hz to 3400Hz (Note 2)	-	-	1.0	µs
Absolute Delay, 4W-4W	300Hz to 3400Hz (Note 2)	-	0.95	-	µs
Transhybrid Loss	$V_{IN} = 1V_{P-P}$ at 1kH (Note 2)	36	40	-	dB
Total Harmonic Distortion 2-Wire/4-Wire, 4-Wire/2-Wire, 4-Wire/4-Wire	Reference Level 0dBm at 600Ω 300Hz to 3400Hz (Note 2)	-	-	-50	dB
Idle Channel Noise 2-Wire and 4-Wire	C-Message (Note 2)	-	3	-	dBrnC
	Psophometric (Note 2)	-	-87	-	dBmp
PSRR, V_{CC} to 2W	30Hz to 200Hz, $R_L = 600Ω$ (Note 2)	30	35	-	dB
PSRR, V_{CC} to 4W		45	47	-	dB
PSRR, VBAT to 2W		23	28	-	dB
PSRR, VBAT to 4W		33	38	-	dB
PSRR, V_{CC} to 2W	200Hz to 3.4kHz, $R_L = 600Ω$ (Note 2)	33	35	-	dB
PSRR, V_{CC} to 4W		44	46	-	dB
PSRR, VBAT to 2W		40	50	-	dB
PSRR, VBAT to 4W		50	60	-	dB
PSRR, V_{CC} to 2W	3.4kHz to 16kHz, $R_L = 600Ω$ (Note 2)	30	34	-	dB
PSRR, V_{CC} to 4W		35	40	-	dB
PSRR, VBAT to 2W		30	40	-	dB
PSRR, VBAT to 4W		40	50	-	dB
DC PARAMETERS					
Loop Current Programming Range	(Note 3)	20	-	60	mA
Loop Current Programming Accuracy		-10	-	+10	%
Loop Current During Power Denial	$R_L = 200Ω$, $V_{BAT} = -48V$	-	±4	-	mA
Fault Current, Tip to Ground	(Note 2)	-	90	-	mA
Fault Current, Ring to Ground		-	100	-	mA
Fault Current, Tip and Ring to Ground	(Note 2)	-	130	-	mA
Switch Hook Detection Threshold		9	12	15	mA
Ring Trip Comparator Voltage Threshold		-0.28	-0.24	-0.22	V
Thermal ALARM Output	Safe Operating Die Temperature Exceeded (Note 2)	-	160	-	^oC
Dial Pulse Distortion	(Note 2)	-	0.1	0.5	ms

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, V_{BAT} = -24V, V_{CC} = +5V, AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

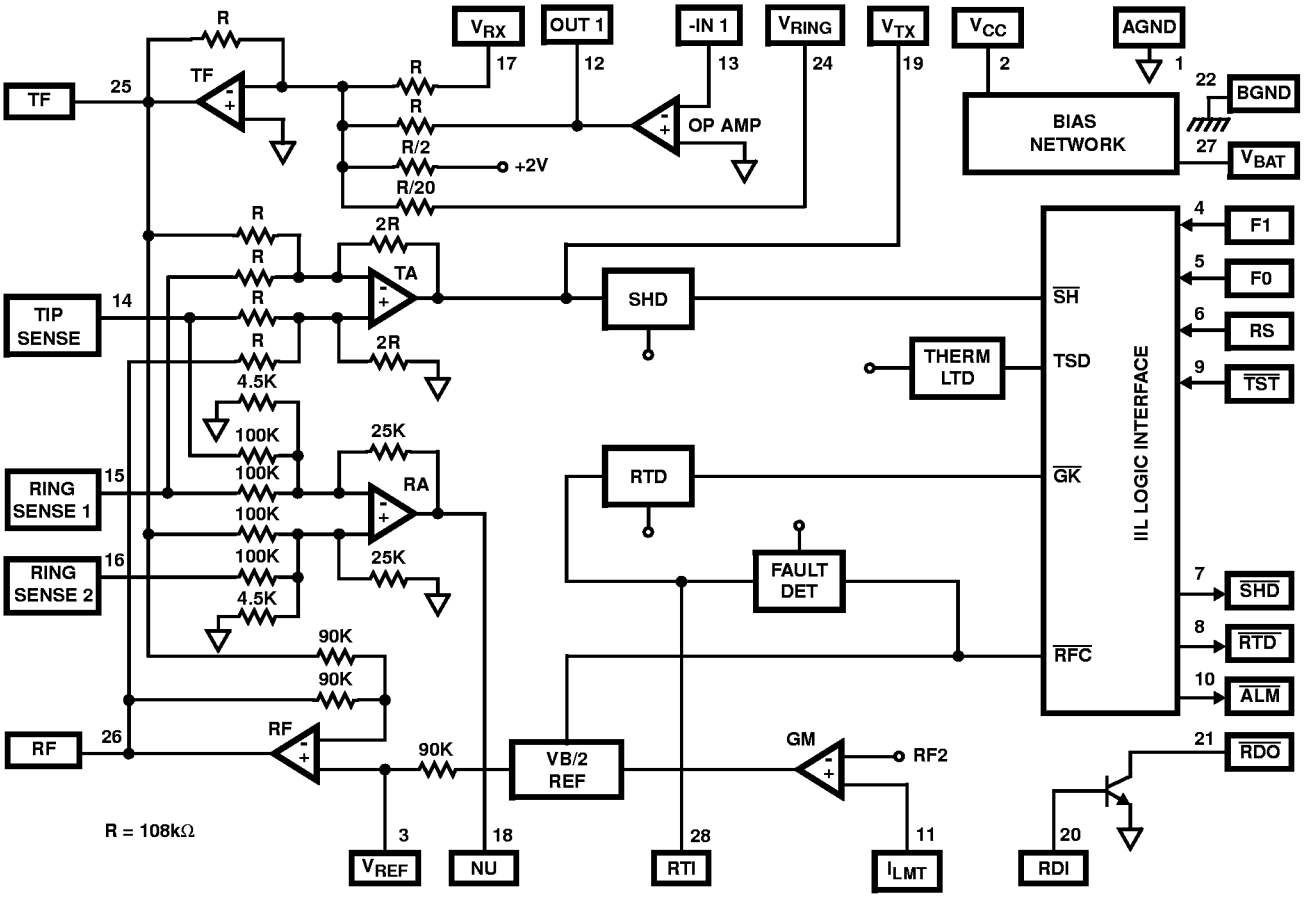
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNCOMMITTED RELAY DRIVER					
On Voltage, V_{OL}	I_{OL} ($\overline{RDO}$) = 30mA	-	0.2	0.5	V
Off Leakage Current		-	±10	±100	µA
TTL/CMOS LOGIC INPUTS (F0, F1, RS, $\overline{TST}$, RDI)					
Logic Low Input Voltage		0	-	0.8	V
Logic High Input Voltage		2.0	-	5.5	V
Input Current	I_{IH}, 0V ≤ V_{IN} ≤ 5V	-	-	-1	µA
Input Current	I_{IL}, 0V ≤ V_{IN} ≤ 5V	-	-	-100	µA
LOGIC OUTPUTS ($\overline{SHD}$, $\overline{RTD}$, $\overline{ALM}$)					
Logic Low Output Voltage	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic High Output Voltage	I_{LOAD} = 40µA	2.7	-	5.5	V
POWER DISSIPATION		-	-	-	
Power Dissipation On Hook	V_{CC} = +5V, V_{BAT} = -80V, R_{LOOP} = ∞	-	300	-	mW
	V_{CC} = +5V, V_{BAT} = -48V, R_{LOOP} = ∞	-	150	-	mW
Power Dissipation Off Hook	V_{CC} = +5V, V_{BAT} = -24V, R_{LOOP} = 600Ω, I_L = 25mA	-	280	-	mW
I_{CC}	V_{CC} = +5V, V_{BAT} = -80V, R_{LOOP} = ∞	-	3	6	mA
	V_{CC} = +5V, V_{BAT} = -48V, R_{LOOP} = ∞	-	2	5	mA
	V_{CC} = +5V, V_{BAT} = -24V, R_{LOOP} = ∞	-	1.9	5	mA
I_{BAT}	V_{CC} = +5V, V_{B-} = -80V, R_{LOOP} = ∞	-	3.6	7	mA
	V_{CC} = +5V, V_{B-} = -48V, R_{LOOP} = ∞	-	2.6	6	mA
	V_{CC} = +5V, V_{B-} = -24V, R_{LOOP} = ∞	-	2.3	4.5	mA

NOTES:

2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
3. This parameter directly affects device junction temperature. Refer to Power Dissipation discussion of data sheet for design information.

Functional Diagram

PLCC/SOIC



HC55171 DEVICE TRUTH TABLE

F1	F0	STATE
0	0	Loop power Denial Active
0	1	Power Down Latch RESET, Power on RESET
1	0	$\overline{RD}$ Active
1	1	Normal Loop feed

The truth table for the internal logic of the HC55171 is provided in the above table. This family of ringing SLICS can be configured to support traditional unbalanced ringing and thru SLIC balanced ringing. Refer to the HC5509A1R3060 for unbalanced ringing application information. The device operating states used by thru SLIC ringing applications are loop power denial and normal feed. During loop power denial, the tip and ring amplifiers are disabled (high impedance) and the DC voltage of each amplifier approaches ground. The SLIC will not provide current to the subscriber loop during this mode and will not detect loop closure. Voice transmission occurs during the normal loop feed mode. During normal loop feed the SLIC is completely operational and performs all transmission and supervisory functions.

Power Dissipation

Careful thermal design is required to guarantee that the maximum junction temperature of 150°C of the device is not exceeded. The junction temperature of the SLIC can be calculated using:

$$T_J = T_A + \theta_{JA}\left(I_{CC}\,V_{CC} + I_{BAT}\,V_{BAT} - \left((I_{LOOP})^2 \bullet R_{LOOP}\right)\right) \quad \text{(EQ. 1)}$$

Where T_A is maximum ambient temperature and θ_{JA} is junction to air thermal resistance (and is package dependent). The entire term in parentheses yields the SLIC power dissipation. The power dissipation of the subscriber loop does not contribute to device junction temperature and is subtracted from the power dissipation term. Operating at 85°C, the maximum PLCC SLIC power dissipation is 1.18W. Likewise, the maximum SOIC SLIC power dissipation is 0.92W.

Circuit Operation and Design Information

Introduction

The HC55171 is a high voltage Subscriber Line Interface Circuit (SLIC) specifically designed for through SLIC ringing applications. Through SLIC ringing applications are broadly defined as any application that requires ringing capability but does not have the standard wired central office interface. The most common implementation of the ringing SLIC is in the analog pots port. The analog pots port provides the ringing function as well as interface compatibility with answering and fax machines.

Subscriber Line Interface Basics

The basic SLIC provides DC loop current to power the handset, supports full duplex analog transmission between the handset and CODEC, matches the impedance of the SLIC to the impedance of the handset and performs loop supervision functions to detect when the handset is off hook. *The ringing SLIC adds through the SLIC ringing capability to this suite of features.* The analog interfaces of the SLIC are categorized as the 2-wire interface (high voltage DC, differential AC) and the 4-wire interface (low voltage DC, single ended AC).

DC Loop Current

The Tip and Ring terminals of the subscriber line circuit are biased at negative potentials with respect to ground. The Tip terminal DC potential is slightly negative with respect to ground, and the ring terminal DC potential is slightly positive with respect to the battery voltage (resulting in a large negative voltage). The HC55171 typical Tip DC voltage is -4V and the typical ring DC voltage is defined as V_{BAT} + 4V. For example, when the battery voltage is -24V the ring voltage is -20V.

To clearly comprehend the Tip and Ring interface it is helpful to understand that the handset and the SLIC constitute a DC and AC current loop as shown in Figure 1. The loop is often referred to as the subscriber loop.

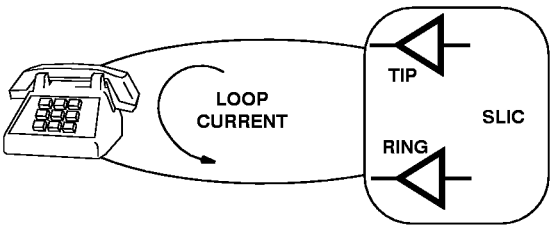


FIGURE 1. SUBSCRIBER LOOP

When the handset is on hook (idle) the phone is an open circuit load and the DC loop current is zero. The SLIC can still provide AC transmission in this condition, which supports caller id services. The DC resistance of the off hook handset is typically 400Ω. Since the Tip DC voltage is more positive than the ring DC voltage, DC loop current flows from Tip to Ring when the handset is off hook. The SLIC is designed with feedback to limit the maximum loop current when the handset is off hook.

Full Duplex Analog Transmission

Familiarity with the signal paths of the SLIC is critical in understanding the full duplex transmission capability of the device. The analog interfaces of the SLIC are categorized as 2-wire interfaces and 4-wire interfaces.

The 2-wire interface of the SLIC consists of the bidirectional Tip and Ring terminals of the device. A differential transmitter drives AC signals out of the Tip and Ring terminals to the handset. A differential receiver across Tip and Ring receives AC signals from the handset. The differential receiver is connected across sense resistors that are in the Tip and Ring signal paths. The differential transmitter and receiver concept is depicted in Figure 2.

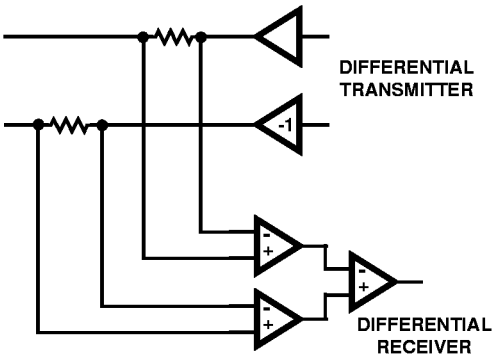


FIGURE 2. DIFFERENTIAL TRANSMIT/RECEIVE CONCEPT

Since the receiver is connected across the transmit signal path, one may deduce that in addition to receiving signals from the handset, the receiver will detect part of the transmit signal. Indeed this does occur and is the reason that all SLIC circuits require a hybrid balance or echo cancellation function.

The 4-wire interface of the SLIC consists of the receive (VRX) and transmit (OUT1) terminals. The 4-wire interfaces are single ended signal paths. The receiver is a dedicated input port and the transmitter is a dedicated output port. The 4-wire receive input of the SLIC drives the 2-wire differential transmitter and the 2-wire differential receiver drives the 4-wire transmit output.

The complete signal path for voice signals includes two digital data busses, a CODEC and a SLIC. There is a receive data bus and transmit data bus, each with an independent 3-wire serial interface. The CODEC contains a coder and decoder. The coder converts the SLIC analog transmit output to digital data for the transmit data bus. The receive digital data bus is converted to analog data and drives the SLIC receive input.

The CODECs use logarithmic compression schemes to extend the resolution of the 8-bit data to 14 bits. The accepted compression schemes are A-law (Harris CODEC - CD22357A) and μ-law (Harris CODEC - CD22354A). The complete signal path from the handset to the CODEC is shown in Figure 3.

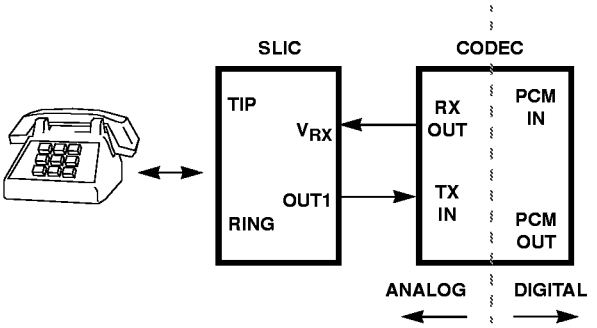


FIGURE 3. COMPLETE VOICE SIGNAL PATH

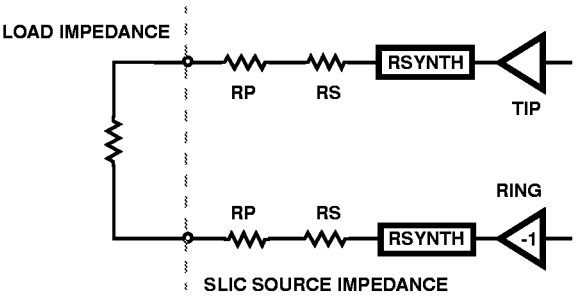


FIGURE 4. SLIC IMPEDANCE DIAGRAM

Impedance Matching

Impedance matching is used to match the AC source impedance of the SLIC to the AC source impedance of the load. When the impedance is matched, the voltage level at the receive input of the SLIC will be the same voltage level that is at the 2-wire differential output (i.e., Tip and Ring). Impedance matching applies only to the 2-wire interface, not the 4-wire interface.

Slic AC signal power levels are most commonly assigned the units dBmO. The term dBmO refers to milliwatts in a 600Ω load. The typical AC power level is 0dBmO which is 1mW referenced to a 600Ω load. The relationship between dBmO and V_{RMS} is provided in Equation 2.

$$dBmO = 10 \cdot \log\left(1000 \cdot \frac{(V_{RMS})^2}{600}\right) \quad \text{(EQ. 2)}$$

Substituting 0dBmO into the equation should result in 0.7746 V_{RMS}. For sinusoidal signals, multiply the RMS voltage by 1.414 to obtain the peak sinusoidal voltage.

The SLIC impedance matching is achieved by applying a feed back loop from the transmit output of the SLIC to the receive input of the SLIC. The transmit output voltage of the HC55171 is proportional to the loop current (DC + AC) flowing in the subscriber loop. The impedance matching feedback only uses the AC portion of the transmit output voltage. Applying a voltage gain to the feedback term and injecting it into the receive signal path, will cause the SLIC to “synthesize” a source impedance that is nonzero. Recall that the impedance matching sets the SLIC source impedance equal to the load impedance.

The SLIC application circuit requires external sense resistors in the Tip and Ring signal paths to achieve the differential receive function. The sense resistors contribute to the source impedance of the SLIC and are accounted for in the design equations. Specifically, if the load impedance is 600Ω and each sense resistor is 50Ω, the SLIC must synthesize an additional source impedance of 500Ω (i.e., 600Ω - 2(50Ω)).

In addition to the sense resistors, some applications may use a protection resistor in each of the Tip and Ring leads as part of a surge protection network. These resistors also contribute to the SLIC source impedance and can be easily accounted for in the design equations. If 50Ω protection resistors are added to the prior example, the SLIC would then have to synthesize 400Ω to match the load (i.e., 600Ω - 2(50Ω) - 2(50Ω)). A diagram showing the impedance terms is shown in Figure 4.

Loop Supervision

The SLIC must detect when the subscriber picks up the handset when the SLIC is not ringing the phone and when the SLIC is ringing the phone. The HC55171 uses a switch hook detector output to indicate loop closure when the SLIC is not ringing the phone. When the SLIC is ringing the phone, loop closure is indicated by the ring trip detector.

(Recall from earlier discussions that the subscriber loop is open when the handset is on hook and closed when off hook. The DC impedance of the handset when off hook is typically 400Ω.)

When the handset is off hook, DC loop current flows from Tip to Ring and the transmit output voltage increases to a negative value. In addition to interfacing to the CODEC and providing the feedback for impedance matching, the transmit output also drives the input to a voltage comparator. When the comparator threshold is exceeded, the $\overline{SHD}$ output goes to a logic low, indicating the handset is off hook. When the call is terminated and the handset is returned on hook, the transmit voltage decreases to zero, crossing the comparator threshold and setting $\overline{SHD}$ to a logic high.

Loop closure must also be detected when the SLIC is ringing the handset. The balanced ringing output of the SLIC coincides with a zero DC potential between Tip and Ring. Therefore the ring trip must be designed around an AC only waveform at the transmit output. When the SLIC is ringing and the handset is on hook, the echo of the ringing signal is at the transmit output. When the handset goes off hook, the amplitude of the ringing echo increases. The increase in amplitude is detected by an envelope detector. When the echo increases, the envelope detector output increases and exceeds the ring trip comparator threshold. Then $\overline{RTD}$ goes to a logic low, indicating the handset is off hook. When the system controller detects a logic low on $\overline{RTD}$, the ringing is turned off and the Tip and Ring terminals return to their typical negative DC potentials.

Design Equations and Operational Theory

The following discussion separates the SLICS's operation into its DC and AC path, then follows up with additional circuit design and application information.

DC Operation of Tip and Ring Amplifiers

SLIC in the Active Mode

The tip and ring amplifiers are voltage feedback op amps that are connected to generate a differential output (e.g., if tip sources 20mA then ring sinks 20mA). Figure 5 shows the connection of the tip and ring amplifiers. The tip DC voltage is set by an internal +2V reference, resulting in -4V at the output. The ring DC voltage is set by the tip DC output voltage and an internal $V_{BAT}/2$ reference, resulting in V_{BAT} +4V at the output. (See Equation 3, Equation 4 and Equation 5.)

$$V_{TIPFEED} = V_C = -2V\left(\frac{R}{R/2}\right) = -4V \quad \text{(EQ. 3)}$$

$$V_{RINGFEED} = V_D = \frac{V_{BAT}}{2}\left(1+\frac{R}{R}\right) - V_{TIPFEED}\left(\frac{R}{R}\right) \quad \text{(EQ. 4)}$$

$$V_{RINGFEED} = V_D = V_{BAT} + 4 \quad \text{(EQ. 5)}$$

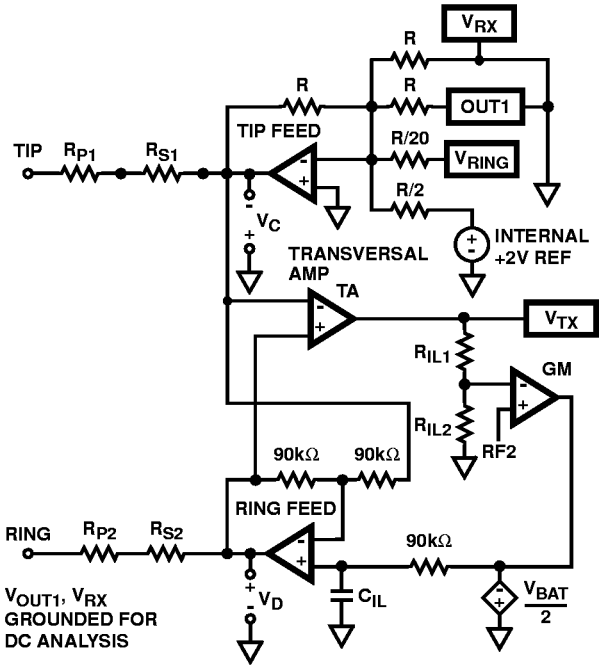


FIGURE 5. OPERATION OF THE TIP AND RING AMPLIFIERS

Transmit Output Voltage

The transmit output voltage in terms of loop current is expressed as 200x I_{LOOP}. The 200 term is actually formed by the sum of twice the sense resistors and is shown in the following equation.

$$200 \times I_{LOOP} = (2 \cdot R_{S1} + 2 \cdot R_{S2}) \times I_{LOOP} \quad \text{(EQ. 6)}$$

This is a relationship that is critical when modifying the sense resistor (R_{S1}, R_{S2}). The 200 term factors into the loop current limit and loop detector functions of the SLIC.

Current Limit

The tip feed to ring feed voltage (Equation 3 minus Equation 5) is equal to the battery voltage minus 8V. Thus, with a 48 (24) volt battery and a 600Ω loop resistance, including the feed resistors, the loop current would be 66.6mA (26.6mA). On short loops the line resistance often approaches zero and there is a need to control the maximum DC loop current.

Current limiting is achieved by a feedback network (Figure 5) that modifies the ring feed voltage (V_D) as a function of the loop current. The output of the Transversal Amplifier (TA) has a DC voltage that is directly proportional to the loop current. This voltage is scaled by R_{IL1} and R_{IL2}. The scaled voltage is the input to a transconductance amplifier (GM) that compares it to an internal reference level. When the scaled voltage exceeds the internal reference level, the transconductance amplifier sources current. This current charges C_{IL} in the positive direction causing the ring feed voltage (V_D) to approach the tip feed voltage (V_C). This effectively reduces the tip feed to ring feed voltage (V_{T-R}), and holds the maximum loop current constant.

The maximum loop current is programed by resistors R_{IL1} and R_{IL2} as shown in Equation 7 (Note: R_{IL1} is typically 100kΩ).

$$I_{LIMIT} = \frac{(0.6)(R_{IL1} + R_{IL2})}{(200 \times R_{IL2})} \quad \text{(EQ. 7)}$$

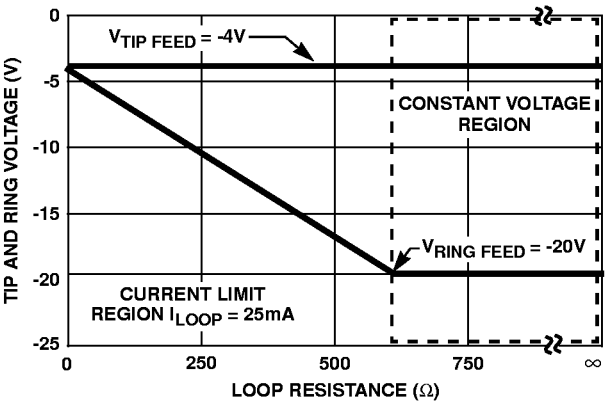


FIGURE 6. V_{T-R} vs R_L (V_{BAT} = -24V, I_{LIMIT} = 25mA)

Figure 6 illustrates the relationship between V_{T-R} and the loop resistance. The conditions are shown for a battery voltage of -24V and the loop current limit set to 25mA. For an open circuit loop the tip feed and ring feed are at -4V and -20V respectively. When the loop resistance decreases from infinity to about 640Ω the loop current (obeying Ohm's Law) increases from 0mA to the set loop current limit. As the loop resistance continues to decrease, the ring feed voltage approaches the tip feed voltage as a function of the programmed loop current limit (Equation 7).

AC Voltage Gain Design Equations

The HC55171 uses feedback to synthesize the impedance at the 2-wire tip and ring terminals. This feedback network defines the AC voltage gains for the SLIC.

The 4-wire to 2-wire voltage gain (V_{RX} to V_{TR}) is set by the feedback loop shown in Figure 7. The feedback loop senses the loop current through resistors R_{S1} and R_{S2}, sums their voltage drop and multiplies it by 2 to produce an output voltage at the V_{TX} pin equal to $+4R_S\Delta I_L$. The V_{TX} voltage is then fed into the -IN1 input of the SLIC's internal op amp. This signal is multiplied by the ratio R_{Z0}/R_{RF} and fed into the tip current summing node via the OUT1 pin. (Note: the internal $V_{BAT}/2$ reference (ring feed amplifier) and the internal +2V reference (tip feed amplifier) are grounded for the AC analysis.)

The current into the summing node of TF amp is equal to:

$$I_{OUT1} = -\frac{4R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right)}{R} \quad \text{(EQ. 8)}$$

Equation 9 is the node equation for the tip amplifier summing node. The current in the tip feedback resistor (I_R) is given in Equation 7.

$$-I_R - \frac{4R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right)}{R} + \frac{V_{RX}}{R} = 0 \quad \text{(EQ. 9)}$$

$$I_R = -\frac{4R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right)}{R} + \frac{V_{RX}}{R} \quad \text{(EQ. 10)}$$

The AC voltage at V_C is then equal to:

$$V_C = (I_R)(R) \quad \text{(EQ. 11)}$$

$$V_C = -4R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right) + V_{RX} \quad \text{(EQ. 12)}$$

and the AC voltage at V_D is:

$$V_D = 4R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right) - V_{RX} \quad \text{(EQ. 13)}$$

The values for R_{Z0} and R_{RF} are selected to match the impedance requirements on tip and ring, for more information refer to AN9607 "Impedance Matching Design Equations for the HC5509 Series of SLICs". The following loop current calculations will assume the proper R_{Z0} and R_{RF} values for matching a 600Ω load.

The loop current (ΔI_L) with respect to the feedback network, is calculated in Equations 14 through 17. Where R_{Z0} = 40kΩ, R_{RF} = 40kΩ, R_L = 600Ω, $R_{P1} = R_{P2} = R_{S1} = R_{S1}$ = 50Ω.

$$\Delta I_L = \frac{V_C - V_D}{R_L + R_{P1} + R_{P2} + R_{S1} + R_{S2}} \quad \text{(EQ. 14)}$$

Substituting the expressions for V_C and V_D

$$\Delta I_L = \frac{2 \times \left(-4R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right) + V_{RX}\right)}{R_L + R_{P1} + R_{P2} + R_{S1} + R_{S2}} \quad \text{(EQ. 15)}$$

Equation 15 simplifies to

$$\Delta I_L = \frac{2V_{RX} - 400\Delta I_L}{800} \quad \text{(EQ. 16)}$$

Solving for ΔI_L results in

$$\Delta I_L = \frac{V_{RX}}{600} \quad \text{(EQ. 17)}$$

Equation 17 is the loop current with respect to the feedback network. From this, the 4-wire to 2-wire and the 2-wire to 4-wire AC voltage gains are calculated. Equation 18 shows the 4-wire to 2-wire AC voltage gain is equal to 1.00.

$$A_{4W-2W} = \frac{V_{TR}}{V_{RX}} = \frac{\Delta I_L(R_L)}{V_{RX}} = \frac{\frac{V_{RX}}{600}(600)}{V_{RX}} = 1 \quad \text{(EQ. 18)}$$

Equation 19 shows the 2-wire to 4-wire AC voltage gain is equal to -0.333.

$$A_{2W-4W} = \frac{V_{OUT1}}{V_{TR}} = \frac{-4R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right)}{\Delta I_L(R_L)} = \frac{-200\frac{V_{RX}}{600}(1)}{\frac{V_{RX}}{600}(600)} = -\frac{1}{3} \quad \text{(EQ. 19)}$$

Impedance Matching

The feedback network, described above, is capable of synthesizing both resistive and complex loads. Matching the SLIC's 2-wire impedance to the load is important to maximize power transfer and maximize the 2-wire return loss. The 2-wire return loss is a measure of the similarity of the impedance of a transmission line (tip and ring) and the impedance at it's termination. It is a ratio, expressed in decibels, of the power of the outgoing signal to the power of the signal reflected back from an impedance discontinuity.

Requirements for Impedance Matching

Impedance matching of the HC55171 application circuit to the transmission line requires that the impedance be matched to points "A" and "B" in Figure 7. To do this, the sense and protection resistors R_{P1}, R_{P2}, R_{S1} and R_{S2} must be accounted for by the feedback network to make it appear as if the output of the tip and ring amplifiers are at points "A" and "B". The feedback network takes a voltage that is equal to the voltage drop across the sense resistors and feeds it into the summing node of the tip amplifier. The effect of this is to cause the tip feed voltage to become more negative by a value that is proportional to the voltage drop across the sense resistors R_{P1} and R_{S1}. At the same time the ring amplifier becomes more positive by the same amount to account for resistors R_{P2} and R_{S2}.

The net effect cancels out the voltage drop across the feed resistors. By nullifying the effects of the feed resistors the feedback circuitry becomes relatively easy to match the impedance at points “A” and “B”.

Impedance Matching Design Equations

Matching the impedance of the SLIC to the load is accomplished by writing a loop equation starting at V_D and going around the loop to V_C.

The loop equation to match the impedance of any load is as follows (note: $V_{RX} = 0$ for this analysis):

$$-4R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right) + 2R_S\Delta I_L - \Delta V_{IN} + R_L\Delta I_L + 2R_S\Delta I_L - 4R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right) = 0 \quad \text{(EQ. 20)}$$

$$\Delta V_{IN} = -8R_S\Delta I_L\left(\frac{R_{Z0}}{R_{RF}}\right) + 4R_S\Delta I_L + R_L\Delta I_L \quad \text{(EQ. 21)}$$

$$\Delta V_{IN} = \Delta I_L\left[-8R_S\left(\frac{R_{Z0}}{R_{RF}}\right) + 4R_S + R_L\right] \quad \text{(EQ. 22)}$$

Equation 22 can be separated into two terms, the feedback ($-8R_S(R_{Z0}/R_{RF})$) and the loop impedance ($+4R_S+R_L$).

$$\frac{\Delta V_{IN}}{\Delta I_L} = -8R_S\left(\frac{R_{Z0}}{R_{RF}}\right) + [4R_S + R_L] \quad \text{(EQ. 23)}$$

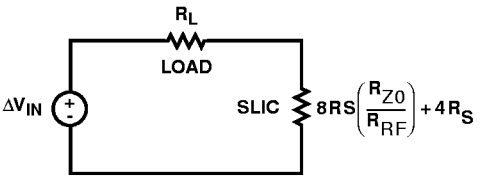


FIGURE 8. SCHEMATIC REPRESENTATION OF EQUATION 20

The result is shown in Equation 23. Figure 8 is a schematic representation of Equation 18. To match the impedance of the SLIC to the impedance of the load, set:

$$8R_S\left(\frac{R_{Z0}}{R_{RF}}\right) + 4R_S = R_L \quad \text{(EQ. 24)}$$

If R_{RF} is made to equal $8R_S$ then:

$$R_{Z0} + 4R_S = R_L \quad \text{(EQ. 25)}$$

Therefore to match the HC5517, with R_S equal to 50Ω, to a 600Ω load:

$$R_{RF} = 8R_S = 8(50\Omega) = 400\Omega \quad \text{(EQ. 26)}$$

and

$$R_{Z0} = R_L - 4R_S = 600\Omega - 200\Omega = 400\Omega \quad \text{(EQ. 27)}$$

To prevent loading of the V_{TX} output, the value of R_{Z0} and R_{RF} are typically scaled by a factor of 100:

$$KR_{Z0} = 40k\Omega \qquad KR_{RF} = 40k\Omega \quad \text{(EQ. 28)}$$

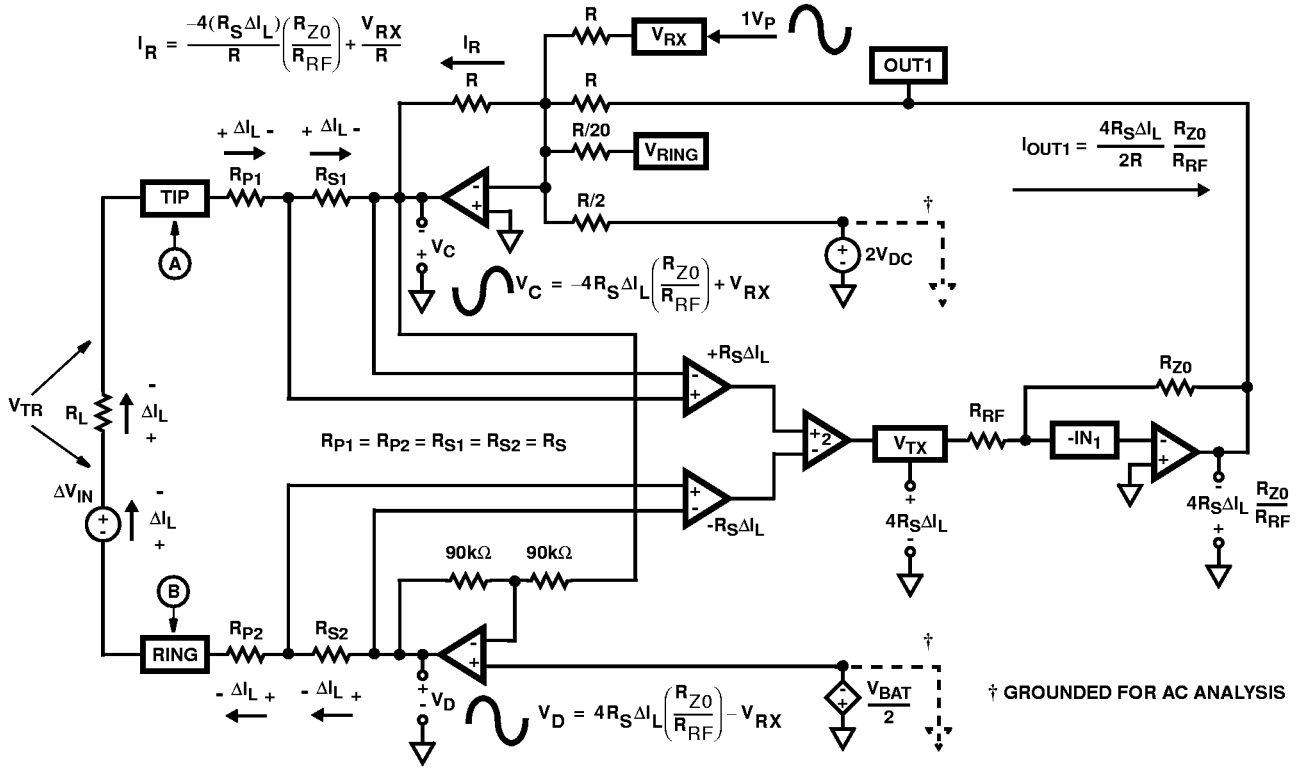


FIGURE 7. AC VOLTAGE GAIN AND IMPEDANCE MATCHING

Since the impedance matching is a function of the voltage gain, scaling of the resistors to achieve a standard value is recommended.

For complex impedances the above analysis is the same.

$$(KR_{RF} = 40k\Omega)\left(KR_{Z0} = 100(Resistive - 200) + \frac{Reactive}{100}\right) \quad \text{(EQ. 29)}$$

Refer to application note AN9607 ("Impedance Matching Design Equations for the HC5509 Series of SLICs") for the values of KR_{RF} and KR_{Z0} for many worldwide typical line impedances.

Through SLIC Ringing

The HC55171 uses linear amplification to produce the ringing signal. As a result the ringing SLIC can produce sinusoid, trapezoid or square wave ringing signals. Regardless of the wave shape, the ringing signal is balanced. The balanced waveform is another way of saying that the tip and ring DC potentials are the same during ringing. The following figure shows the Tip and Ring waveforms for sinusoid and trapezoid wave shapes as can be displayed using an oscilloscope.

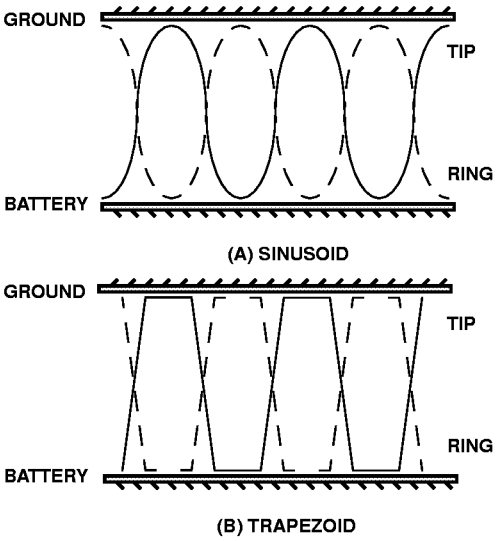


FIGURE 9. BALANCED RINGING WAVESHAPES

Pertinent Bellcore Ringing Specifications

Bellcore has defined bounds around the existing unbalanced ringing signal that is supplied by the central office. The HC55171 ringing SLIC meets the REN drive requirement, the crest factor limitations and the minimum RMS ringing voltage.

The foremost requirement is that the ringing source must be able to drive 5 REN. A REN is a ringer equivalence number modeled by a 6.93kΩ resistor in series with a 8µF capacitor (see Figure 10). The impedance of 1 REN at 20Hz is approximately 7kΩ. 5 REN is equivalent to five of the networks in parallel. Figure 10 provides the Bellcore REN models.

The crest factor of the ringing waveform is the ratio of the peak voltage to the RMS voltage. For reference, the crest factor of a sinusoid is 1.414 and of a square wave is 1.0. Bellcore defines the crest factor range from 1.2 to 1.6. A signal with a crest factor between 1.2 and 1.414 resembles the trapezoid of Figure 9. A signal with a crest factor between 1.414 and 1.6 resembles a "rounded triangular" wave shape and is an inefficient waveform for the ringing SLIC.

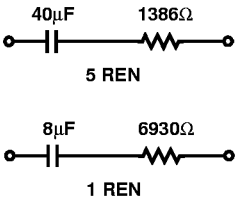


FIGURE 10. BELLCORE RINGER EQUIVALENCE MODELS

The third pertinent Bellcore requirement is the that RMS ringing voltage must be greater than $40V_{RMS}$ at the telephone instrument. The HC5517 is able to deliver $40V_{RMS}$ at the end of 500Ω loops. The 500Ω loop drive capability of the HC5517 is achieved with trapezoidal ringing.

Sinusoidal Ringing

The HC55171 uses the same sinusoidal application circuit as the HC5517. The only difference being the values of three components in the ring trip filter. The following table lists the components and the different values required by each device. All reference designators refer to the application circuit published in the HC5517 and HC55171 data sheet.

TABLE 1. RING TRIP COMPONENT DIFFERENCES

COMPONENT	HC5517	COMPONENT	HC55171
R_{15}	47kΩ	R_{RT3}	51.1kΩ
R_{17}	56.2kΩ	R_{RT1}	49.9kΩ
C_{10}	1.0µF	C_{RT}	0.47µF

The sinusoidal circuit published in the HC5517 can be used as an additional reference circuit for the HC55171. To generate a sinusoid ringing signal, two conditions must be met on the ringing (V_{RING}) input of the SLIC.

The first condition is that a positive DC voltage, which is directly related to the battery voltage, must be present at the ringing input. The DC voltage is used to force the Tip and Ring DC outputs to half the battery voltage. Having both the Tip and Ring amplifiers biased at the same DC voltage during ringing is one characteristic of balanced ringing. The centering voltage (V_C) can be calculated from the following equation.

$$V_C = \left(\left|\frac{V_{BAT}}{2}\right| - 4\right)/20 \quad \text{(EQ. 30)}$$

Substituting values of battery voltage, the centering voltage is +1.8V for a -80V battery and +1.3V for a -60V battery.

The second condition that must be met for sinusoidal ringing is a low level ringing signal must be applied to the ringing input of the SLIC. The AC signal that is present at V_{RING} will

be amplified by a gain of 20 through the Tip amplifier and a then inverted through the ring amplifier, resulting in a differential gain of 40. The maximum low level amplitude that can be injected for a given battery voltage can be determined from the following equation.

$$V_{RING(Max)} = (V_{BAT} - 8)/20 \quad \text{(EQ. 31)}$$

The maximum output swing may be increased by driving the V_{RING} negative by 200mV. Equation 31 can then by rewritten as:

$$V_{RING(Max)} = (V_{BAT} - 5)/20 \quad \text{(EQ. 32)}$$

Exceeding the maximum signal calculated from the above equation will cause the peaks of the sinusoid to clip at ground and battery. The compression will reduce the crest factor of the waveform, producing a trapezoidal waveform. This is just one method, though inefficient, for achieving trapezoidal ringing. The application circuit provided with the HC55171 has been specifically developed for trapezoidal ringing and may also be used with the HC5517.

Trapezoidal Ringing

The trapezoidal ringing waveform provides a larger RMS voltage to the handset. Larger RMS voltages to the handset provide more power for ringing and also increase the loop length supported by the ringing SLIC.

The HC55171 trapezoidal ringing application circuit will operate for loop lengths ranging from 0Ω to 500Ω. In addition, one set of component values will satisfy the entire ringing loop range of the SLIC. A single resistor sets the open circuit RMS ringing voltage, which will set the crest factor of the ringing waveform. The crest factor of the HC55171 ringing waveform is independent of the ringing load (REN) and the loop length. Another robust feature of the HC55171 ringing SLIC is the ring trip detector circuit. The suggested values for the ring trip detector circuit cover quite a large range of applications.

The assumptions used to design the trapezoidal ringing application circuit are listed below:

- Loop current limit set to 25mA.
- Impedance matching is set to 600Ω resistive.
- 2-wire surge protection is not required.
- System able to monitor $\overline{RTD}$ and $\overline{SHD}$.
- Logic ringing signal is used to drive RC trapezoid network.

Crest Factor Programming

As previously mentioned, a single resistor is required to set the crest factor of the trapezoidal waveform. The only design variable in determining the crest factor is the battery voltage. The battery voltage limits the peak signal swing and therefore directly determines the crest factor.

A set of tables will be provided to allow selection of the crest factor setting resistor. The tables will include crest factors below the Bellcore minimum of 1.2 since many ringing SLIC applications are not constrained by Bellcore requirements.

TABLE 2. CREST FACTOR PROGRAMMING RESISTOR FOR V_{BAT} = -80V

R_{TRAP}	CF	RMS	R_{TRAP}	CF	RMS
0Ω	1.10	65.0	825Ω	1.25	57.6
389Ω	1.15	62.6	964Ω	1.30	55.4
640Ω	1.20	60.0	1095Ω	1.35	53.3

The RMS voltage listed in the table is the open circuit RMS voltage generated by the SLIC.

TABLE 3. CREST FACTOR PROGRAMMING RESISTOR FOR V_{BAT} = -75V

R_{TRAP}	CF	RMS	R_{TRAP}	CF	RMS
0Ω	1.10	60.9	1010Ω	1.25	53.7
500Ω	1.15	58.3	1190Ω	1.30	51.6
791Ω	1.20	55.9	1334Ω	1.35	49.7

TABLE 4. CREST FACTOR PROGRAMMING RESISTOR FOR V_{BAT} = -65V

R_{TRAP}	CF	RMS	R_{TRAP}	CF	RMS
0Ω	1.10	52.5	1330Ω	1.25	45.9
660Ω	1.15	49.8	1600Ω	1.30	44.1
1040Ω	1.20	47.8	1800Ω	1.35	42.5

TABLE 5. CREST FACTOR PROGRAMMING RESISTOR FOR V_{BAT} = -60V

R_{TRAP}	CF	RMS	R_{TRAP}	CF	RMS
0Ω	1.10	48.2	1460Ω	1.25	42.0
740Ω	1.15	45.6	1760Ω	1.30	40.4
1129Ω	1.20	43.7	2030Ω	1.35	38.8

Ringing Voltage Limiting Factors

As the load impedance decreases (increasing REN), the feedback used for impedance synthesis slightly attenuates the ringing signal. Another factor that attenuates the ringing signal is the voltage divider formed by the sense resistors and the impedance of the ringing load. as the load impedance decreases, the 100Ω of sense resistors becomes a larger percentage of the load impedance.

If surge protection resistance must be used with the trapezoidal circuit, the loop length performance of the circuit will decrease. The decrease in ringing loop length is caused by the addition of protection resistors in series with the Tip and Ring outputs. The amount of protection resistance that is added will subtract directly from the loop length. For example if 30Ω protection resistors is used in each of the Tip and Ring leads, the ringing loop length will decrease by a total of 60Ω. Therefore, subtracting 60Ω from the graphs will provide the reduced loop length data.

Lab Measurements

The lab measurements of the trapezoidal ringing circuit were made with the crest factor programming resistor set to 0Ω and the battery voltage set to -80V. The Bellcore suggested REN model was used to simulate the various ringing loads. A resistor in series with the Tip terminal was used to emulate loop length.

A logic gate is used to drive the RC shaping network. When the crest factor programming resistor is set to 0Ω, the output impedance of the logic gate results in a 0.8V/ms slewing voltage on C_{TRAP}.

Each graph shows the RMS ringing voltage into a fixed REN load versus loop length. The ringing voltage was measured across the test load. Each test also verified proper operation of the ring trip detector. Proper ring trip detector operation is defined as a constant logic high while ringing and on hook and a constant logic low when off hook is detected. The component values in the application circuit provide a ring trip response in the 100ms to 150ms range.

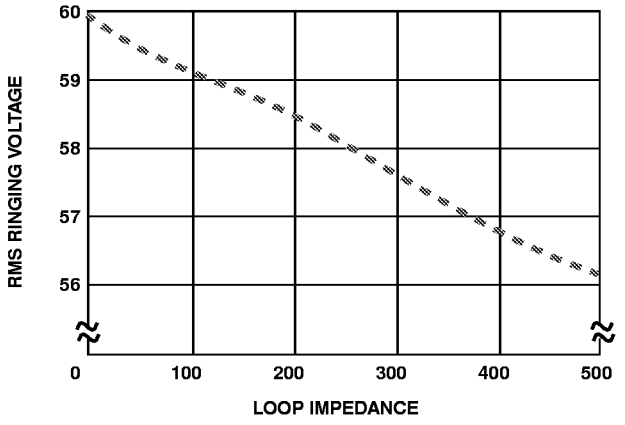


FIGURE 11. RMS RINGING VOLTAGE vs LOOP LENGTH REN = 1

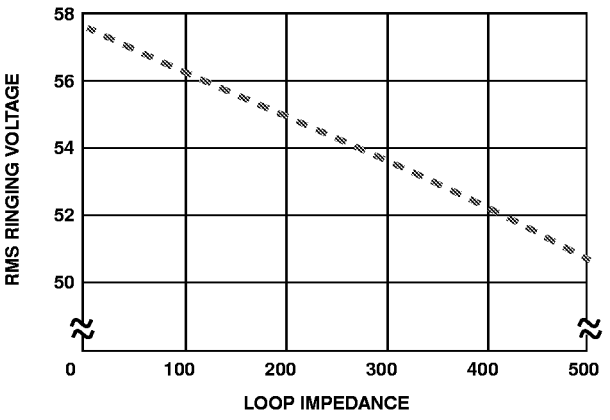


FIGURE 12. RMS RINGING VOLTAGE vs LOOP LENGTH REN = 2

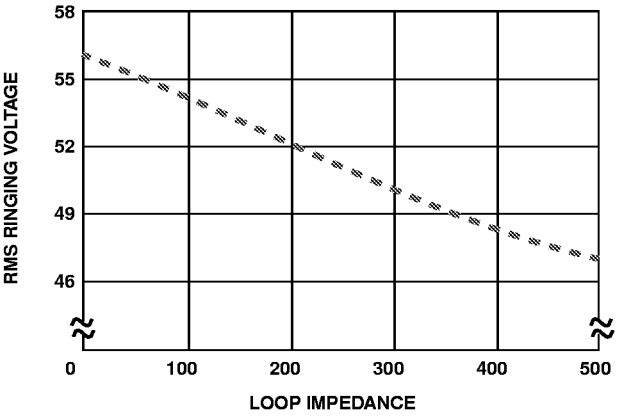


FIGURE 13. RMS RINGING VOLTAGE vs LOOP LENGTH REN = 3

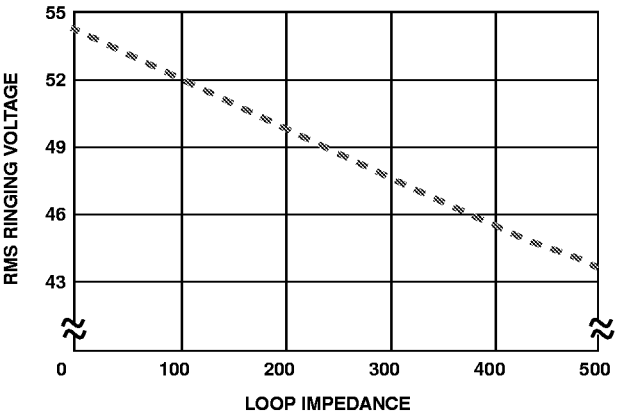


FIGURE 14. RMS RINGING VOLTAGE vs LOOP LENGTH REN = 4

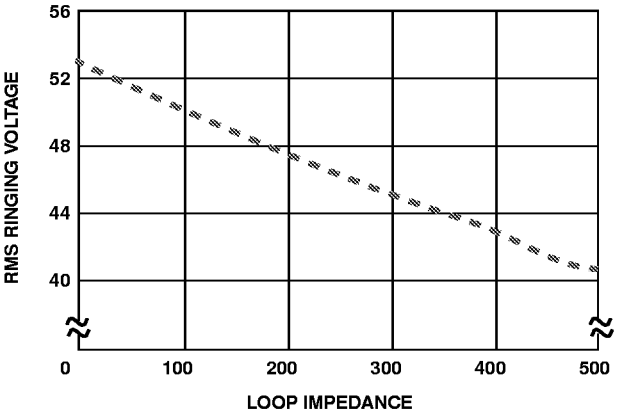


FIGURE 15. RMS RINGING VOLTAGE vs LOOP LENGTH REN = 5

Low Level Ringing Interface

The trapezoidal application circuit only requires a cadenced logic signal applied to the wave shaping RC network to achieve ringing. When not ringing, the logic signal should be held low. When the logic signal is low, Tip will be near ground and Ring will be near battery. When the logic signal is high, Tip will be near battery and Ring will be near ground.

Loop Detector Interface

The $\overline{RTD}$ output should be monitored for off hook detection during the ringing period. At all other times, the $\overline{SHD}$ should be monitored for off hook detection. The application circuit can be modified to redirect the ring trip information through the $\overline{SHD}$ interface. The change can be made by rewiring the application circuit, adding a pullup resistor to pin 23 and setting F0 low for the entire duration of the ringing period. The modifications to the application circuit for the single detector interface are shown in Figure 16.

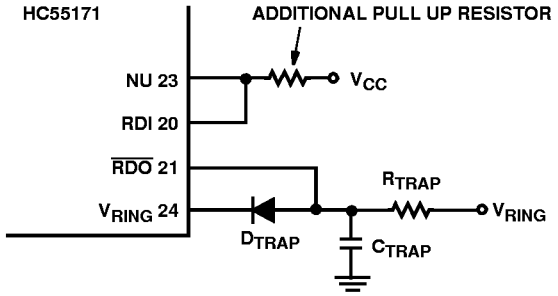


FIGURE 16. APPLICATION CIRCUIT WIRING FOR SINGLE LOOP DETECTOR INTERFACE

SLIC Operating State During Ringing

The SLIC control pin F1 should always be a logic high during ringing. The control pin F0 will either be a constant logic high (two detector interface) or a logic low (single detector interface). Figure 17 shows the control interface for the dual detector interface and the single detector interface.

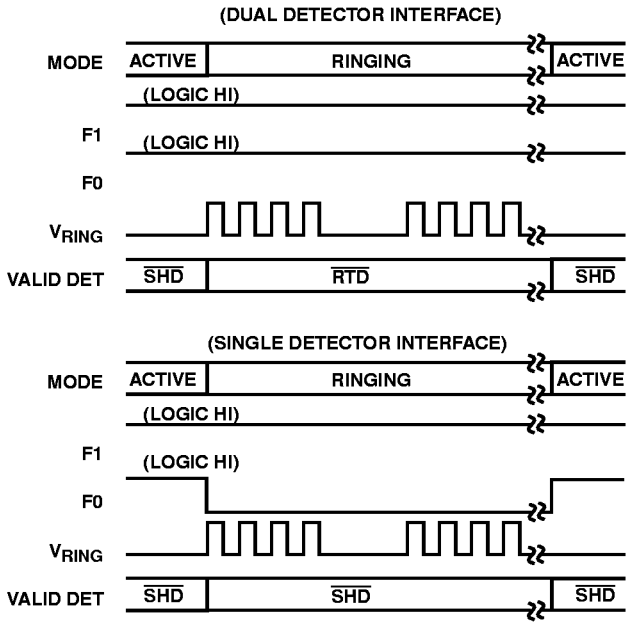


FIGURE 17. DETECTOR LOGIC INTERFACES

Additional Application Information

Tip-to-Ring Open Circuit Voltage

The tip-to-ring open-circuit voltage, V_{OC}, of the HC55171 may be programmed to meet a variety of applications. The design of the HC5517 defaults the value of V_{OC} to:

$$V_{OC} \cong |V_{BAT}| - 8$$

Using a zener diode clamping circuit, the default open circuit voltage of the SLIC may be defeated. Some applications that have to meet Maintenance Termination Unit (MTU) compliance have a few options with the HC55171. One option is to reduce the ringing battery voltage until MTU compliance is achieved. Another option is to use a zener clamping circuit on V_{REF} to over ride the default open circuit voltage when operating from a high battery.

If a clamping network is used it is important that it is disabled during ringing. The clamping network must be disabled to allow the SLIC to achieve its full ringing capability. A zener clamping circuit is provided in Figure 18.

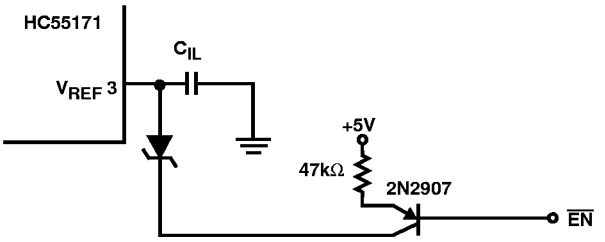


FIGURE 18. ZENER CLAMP CIRCUIT WITH DISABLE

The following equations are used to predict the DC output of the ring feed amplifier when using the zener clamping network, V_{RDC}.

$$\left|\frac{V_{BAT}}{2}\right| < V_Z \qquad V_{RDC} = 2\left(\frac{V_{BAT}}{2}\right) + 4 \qquad \text{(EQ. 33)}$$

$$\left|\frac{V_{BAT}}{2}\right| \geq V_Z \qquad V_{RDC} = 2(-V_Z + (V_{CE} - V_{BE})) + 4 \qquad \text{(EQ. 34)}$$

Where V_Z is the zener diode voltage and V_{CE} and V_{BE} are the saturation voltages of the pnp transistor. Using Equations 31 and 32, the tip-to-ring open-circuit voltage can be calculated for any value of zener diode and battery voltage.

$$\left|\frac{V_{BAT}}{2}\right| < V_Z \qquad V_{OC} = V_{TDC} - 2\left(\frac{V_{BAT}}{2}\right) - 4 \qquad \text{(EQ. 35)}$$

$$\left|\frac{V_{BAT}}{2}\right| \geq V_Z \qquad V_{OC} = V_{TDC} - 2(-V_Z + (V_{CE} - V_{BE})) - 4 \qquad \text{(EQ. 36)}$$

When the base of the pnp transistor is pulled high (+5V), the transistor is off and the zener clamp is disabled. When the base of the transistor is pulled low (0V) the transistor is on and the zener will clamp as long as half the battery voltage is greater than the zener voltage.

Polarity Reversal

The HC55171 supports applications that use polarity reversal outside the speech phase of a call connection. The most common implementation of this type of polarity reversal is used with pay phones. By reversing the polarity of the tip and ring terminals of a pay phone, DC current changes direction in a solenoid and the coins are released from the phone. To reverse the polarity of the HC55171, simply toggle the V_{RING} input high. Setting the V_{RING} input high will cause Tip and Ring to reverse polarity.

Transhybrid Balance

Since the receive signal and its echo are 180 degrees out of phase, the summing node of an operational amplifier can be used to cancel the echo. Nearly all CODECs have an internal amplifier for echo cancellation. The following Figure 19 shows the cancellation amplifier circuit.

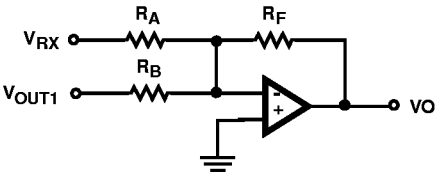


FIGURE 19. TRANHYBRID AMPLIFIER CIRCUIT

When the SLIC is matched to a 600Ω load, the echo amplitude is 1/3 the receive input amplitude. Therefore, by configuring the transhybrid amplifier with a gain of 3 in the echo path, cancellation can be achieved. The following equations:

$$V_O = -\left(V_{RX}\left(\frac{R_F}{R_A}\right) + V_{OUT1}\left(\frac{R_F}{R_B}\right)\right) \quad \text{(EQ. 37)}$$

Substituting the fact that V_{OUT1} is -1/3 of V_{RX}

$$V_O = -\left(V_{RX}\left(\frac{R_F}{R_A}\right) - V_{RX}\left(\frac{1}{3}\right)\left(\frac{R_F}{R_B}\right)\right) \quad \text{(EQ. 38)}$$

Since cancellation implies that under these conditions, the output V_O should be zero, set Equation 37 equal to zero and solve for R_B.

$$R_B = \frac{R_A}{3} \quad \text{(EQ. 39)}$$

Another outcome of the transhybrid gain selection is the 2-wire to 4-wire gain of the SLIC as seen by the CODEC. The 1/3 voltage gain in the transmit path is relevant to the receive input as well as any signals from the 2-wire side. Therefore by setting the V_{OUT1} gain to three in the previous analysis, the 2-wire to 4-wire gain was set to unity.

Single Supply Codec Interface

The majority of CODECs that interface to the ringing SLIC operate from a single +5V supply and ground. Figure 20 shows the circuitry required to properly interface the ringing SLIC to the single supply CODEC.

The CODEC signal names may vary from different manufacturers, but the function provided will be the same. The DC reference from the CODEC is used to bias the analog signals between +5V and ground. The capacitors are required so that the DC gain is unity for proper biasing from the CODEC reference. Also, the capacitors block DC signals that may interfere with SLIC or CODEC operation.

Layout Guidelines and Considerations

The printed circuit board trace length to all high impedance nodes should be kept as short as possible. Minimizing length will reduce the risk of noise or other unwanted signal pickup. The short lead length also applies to all high gain inputs. The set of circuit nodes that can be categorized as such are:

- V_{RX} pin 27, the 4-wire voice input.
- -IN1 pin 13, the inverting input of the internal amplifier.
- V_{REF} pin 3, the noninverting input to ring feed amplifier.
- V_{RING} pin 24, the 20V/V input for the ringing signal.

For multi layer boards, the traces connected to tip should not cross the traces connected to ring. Since they will be carrying high voltages, and could be subject to lightning or surge depending on the application, using a larger than minimum trace width is advised.

The 4-wire transmit and receive signal paths should not cross. The receive path is any trace associated with the V_{RX} input and the transmit path is any trace associated with V_{TX} output. The physical distance between the two signal paths should be maximized to reduce crosstalk.

The mode control signals and detector outputs should be routed away from the analog circuitry. Though the digital signals are nearly static, care should be taken to minimize coupling of the sharp digital edges to the analog signals.

The part has two ground pins, one is labeled AGND and the other BGND. Both pins should be connected together as close as possible to the SLIC. If a ground plane is available, then both AGND and BGND should be connected directly to the ground plane.

A ground plane that provides a low impedance return path for the supply currents should be used. A ground plane provides isolation between analog and digital signals. If the layout density does not accommodate a ground plane, a single point grounding scheme should be used.

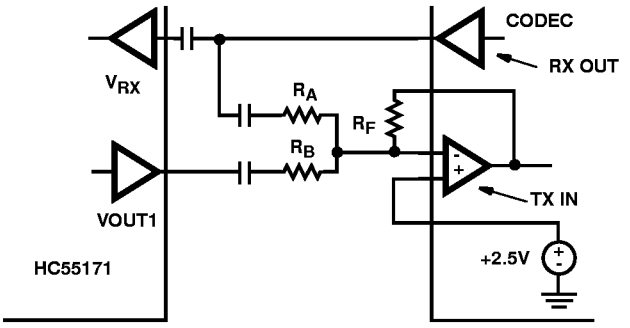


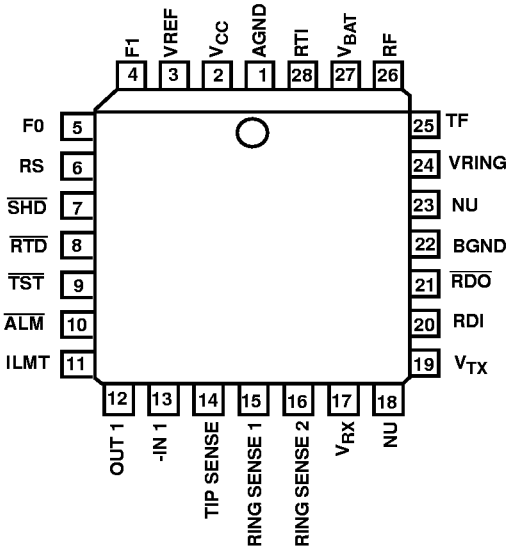
FIGURE 20. SINGLE SUPPLY CODEC INTERFACE

Pin Descriptions

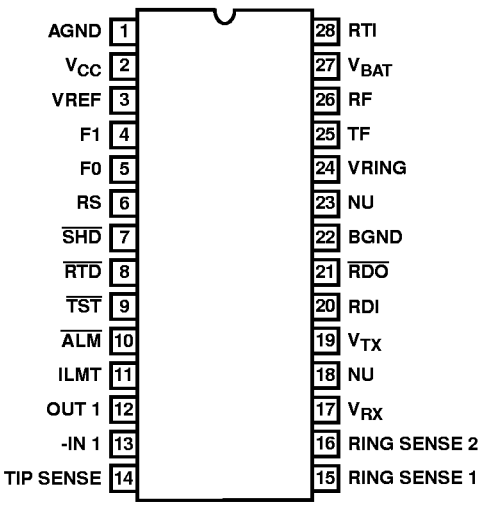
PLCC	SYMBOL	DESCRIPTION
1	AGND	Analog Ground - Serves as a reference for the transmit output and receive input terminals.
2	V_{CC}	Positive Voltage Source - Most Positive Supply.
3	V_{REF}	An external voltage connected to this pin will override the internal $V_{BAT}/2$ reference.
4	F1	Power Denial - An active low TTL compatible logic control input. When enabled, the output of the ring amplifier will ramp close to the output voltage of the tip amplifier.
5	F0	TTL compatible logic control input that must be tied high for proper SLIC operation.
6	RS	TTL compatible logic control input that must be tied high for proper SLIC operation.
7	$\overline{SHD}$	Switch Hook Detection - An active low TTL compatible logic output. Indicates an off-hook condition.
8	$\overline{RTD}$	Ring Trip Detection - An active low TTL compatible logic output. Indicates an off-hook condition when the phone is ringing.
9	$\overline{TST}$	A TTL logic input. A low on this pin will keep the SLIC in a power down mode. The $\overline{TST}$ pin in conjunction with the $\overline{ALM}$ pin can provide thermal shutdown protection for the SLIC. Thermal shutdown is implemented by a system controller that monitors the $\overline{ALM}$ pin. When the $\overline{ALM}$ pin is active (low) the system controller issues a command to the $\overline{TST}$ pin (low) to power down the SLIC. The timing of the thermal recovery is controlled by the system controller.
10	$\overline{ALM}$	A TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded.
11	I_{LMT}	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions.
12	OUT1	The analog output of the spare operational amplifier.
13	-IN1	The inverting analog input of the spare operational amplifier. The non-inverting input is internally connected to AGND.
14	TIP SENSE	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor. Functions with the RING terminal to receive voice signals and for loop monitoring purpose.
15	RING SENSE 1	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals and for loop monitoring purposes.
16	RING SENSE 2	This is an internal sense mode that must be tied to RING SENSE 1 for proper SLIC operation.
17	V_{RX}	Receive Input, 4-Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers deferentially.
18	NU	Not used in this application.This pin should be left floating.
19	V_{TX}	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	RDI	TTL compatible input to drive the uncommitted relay driver.
21	$\overline{RDO}$	This is the output of the uncommitted relay driver.
22	BGND	Battery Ground - All loop current and some quiescent current flows into this terminal.
23	NU	Not used in this application. This pin should be either grounded or left floating.
24	V_{RING}	Ring signal input.
25	TF	This is the output of the tip amplifier.
26	RF	This is the output of the ring amplifier.
27	V_{BAT}	The negative battery source.
28	RTI	Ring Trip Input - This pin is connected to the external negative peak detector output for ring trip detection.

Pinouts

HC55171 (PLCC)
TOP VIEW



HC55171 (SOIC)
TOP VIEW



Trapezoidal Ringing Application Circuit

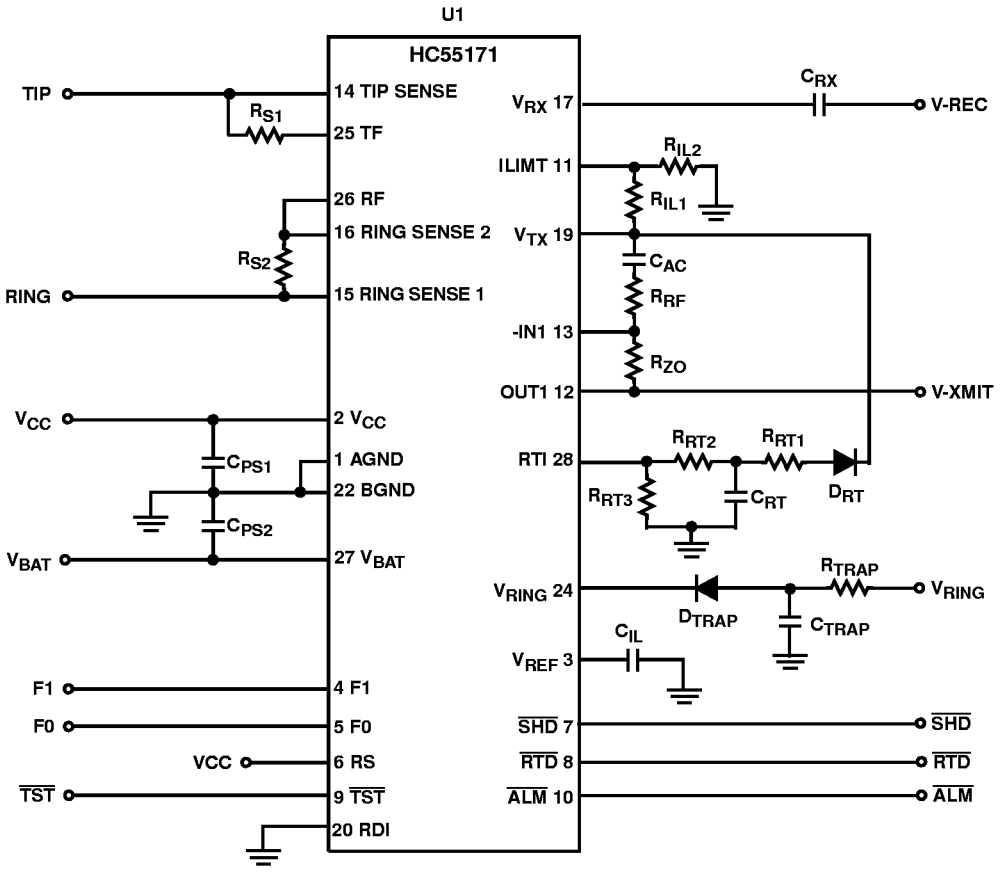
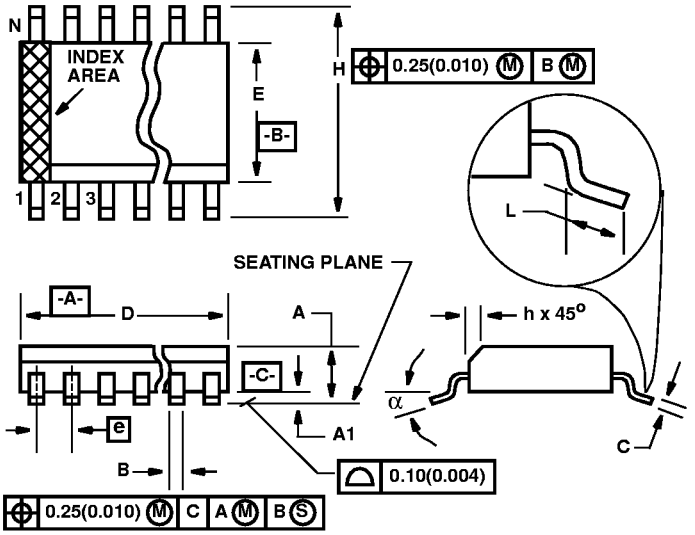


FIGURE 21. TRAPEZOIDAL RINGING APPLICATION CIRCUIT

HC55171 Trapezoidal Ringing Application Circuit Parts List

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
U1 - Ringing Slic	HC55171	N/A	N/A	R_{IL2}	7.68kΩ	1%	1/8W
R_{S1}, R_{S2}	49.9Ω	1%	1/2W	R_{TRAP}	App Driven	1%	1/8W
R_{ZO}, R_{IL1}	56.2kΩ	1%	1/8W	C_{PS1}, C_{PS2}	0.1µF	10%	100V
R_{RT1}	49.9kΩ	1%	1/8W	C_{IL}, C_{RT}, C_{AC}, C_{RX}	0.47µF	10%	50V
R_{RT2}	1.5MΩ	1%	1/8W	C_{TRAP}	4.7µF	10%	10V
R_{RT3}	51.1kΩ	1%	1/8W	D_{RT}, D_{TRAP}	1N914	Generic Rectifier Diode	
R_{RF}	45.3kΩ	1%	1/8W				

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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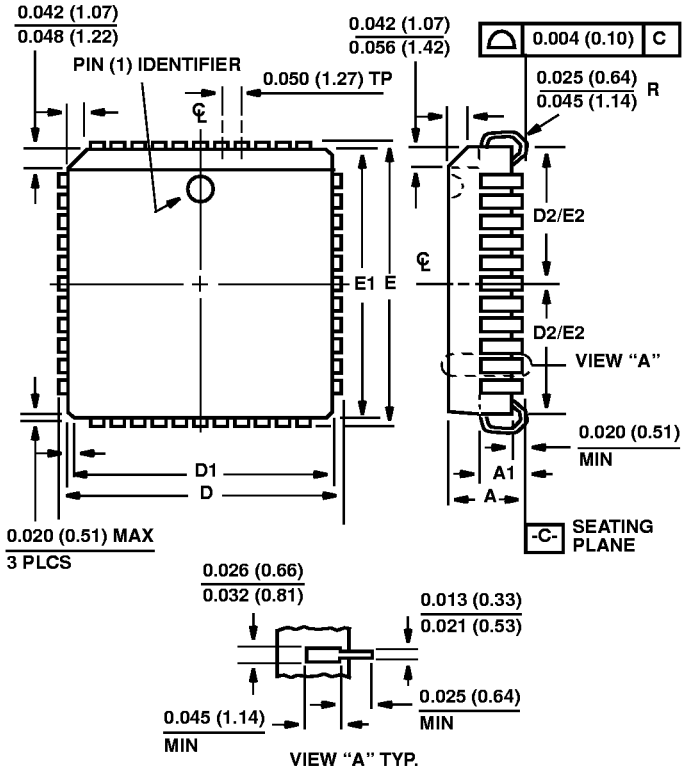
NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.