HD49430F

Preliminary Specification

HITACHI

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General Description

HD49430F is a highly integrated Downstream Processor optimized for applications such as Cable Modems and Set-top boxes and forms a complete and optimal solution with its companion HD49429F Upstream processor. The down-stream channel is processed by a high performance 256/64 QAM Demodulator and a MCNS compliant Forward Error Correction (FEC) decoder. HD49430F is highly programmable via a general purpose microprocessor port and a I^2C serial port.

HD49430F is implemented in an advanced CMOS process and uses a single 3.3V (+/- 10%) power supply, and is packaged in a low cost 100pin PQFP.

Features

- State of the art QAM Demodulator
  - — 256/64 QAM Demodulator.
  - — Uses the proven HD49428 QAM Demodulator Architecture with significant enhancements.
  - — For 6 MHz Channels, implements 30Mbits/s system (64QAM) and 40Mbits/s (256QAM).
  - — Uses 8 or 10 bit input sampling.
  - — On-chip tone canceler removes narrow band interference.
  - — High phase -noise immunity.
  - — Special algorithms to handle impulse noise.
- Highly programmable MCNS Compliant Reed-Soloman Forward Error Correction(FEC) Decoder.
  - — MCNS Compliant FEC decoder (including Trellis decoder and RS Decoder).
  - — On-chip 56Kbit De-interleaver RAM.
- High Performance Analog circuits to optimize system implementation and reduce system cost.
  - — On-chip VCXOs for generation of 64Q and 256Q symbol rates.
  - — On-chip VCO to generate serial bit rates for 64Q and 256Q.
- Enhanced Observability with low cost uP interface.
  - — QAM demodulator has a very high degree of observability via the general purpose microprocessor and I^2C interfaces. This information can be used to implement an inexpensive remote or local channel monitoring system for channel debug.
- Low Component and System Cost.
  - — Low Power
  - — Surface -mount PQFP-100 packaging

Simplified Chip Block Diagram

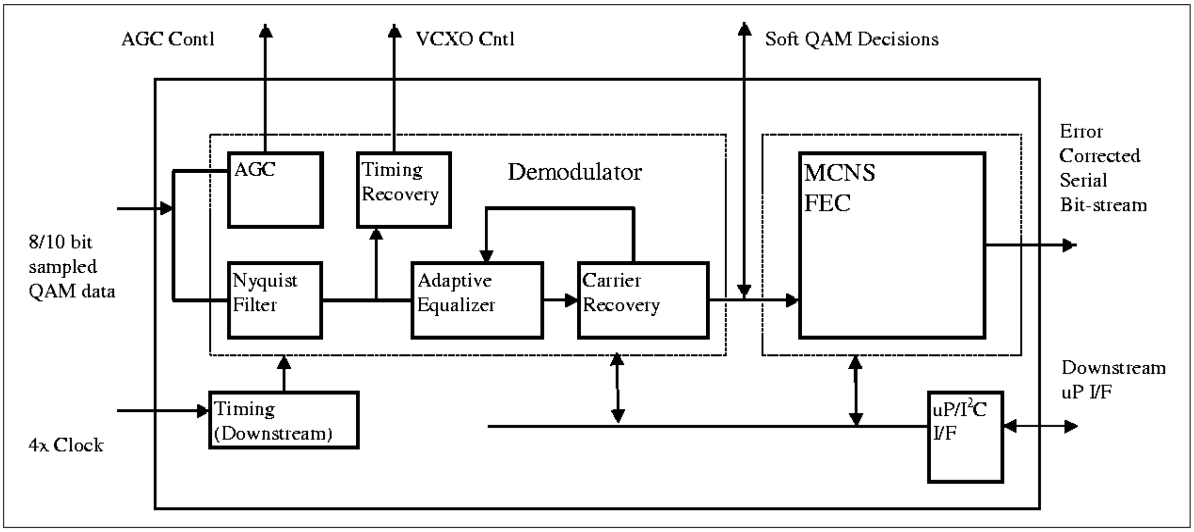


Figure 1 Simplified Block Diagram

Detailed System Specifications

QAM 64 Specifications

Table 1 64 QAM specifications

Parameter	Specification	
Frequency	+/- 300 kHz	
Phase noise:	-73 dBc/Hz at 10 kHz from carrier	
CNR	23 dB signal power to noise power in 5 MHz for corrected BER of 10-8.	
Hum (120 Hz Modulation)	10% peak to peak Square hum (infinite bandwidth)	
	20% peak to peak Sinusoidal hum	
	26% peak to peak Triangular hum	
Residual FM	50 kHz peak to peak deviation when modulated by 120 Hz sine wave.	
Discrete RF Interference	Single tone -15 dBc	
Multipath(when reference tap is ~ 1/3 of total delay range of equalizer taps)	Delay Amplitude	(reflection/signal ratio)
	0-300ns	10db
	300-700 ns	10 dB
	700-1400 ns	15 dB
Spectral Tilt	+/- 5 dB	
Saw Filter Ripple	< +/-0.50 dB	
Saw Filter Group Delay Variation	< +/- 75 ns	
Acquisition Time:	< 100 msec	Operating Condition is -11 dB, 600 ns multipath, 26 dB SNR
	< 100msec	Operating Condition is -73 dBc @10 kHz phase noise, 26 dB SNR
Dynamic multipath	Single multipath at 1 usec: -20 dBc, phase rotation = 5 Hz.	
AGC Voltage	0-3.3 Volts	

QAM 256 Specifications

Table 2 256 QAM Specifications

Parameter	Specification	
Frequency	+/-300 kHz	
Phase noise:	-77 dBc/Hz at 10 kHz from carrier	
CNR	30 dB for corrected BER of 10-8.	
Hum (120 Hz Modulation)	7% peak to peak Square hum (infinite bandwidth) 18% peak to peak Sinusoidal hum 23% peak to peak Triangular hum	
Residual FM	50 KHz peak to peak deviation when modulated by 120 Hz sine wave.	
Discrete RF Interference	Single tone -21 dBc	
Multipath (when reference tap is ~ 1/3 of total delay range of equalizer taps)	Delay Amplitude 0-300 ns 300-700 ns 700-1400 ns	(reflection/signal ratio) -10db -13 dB -15 dB
Spectral Tilt	+/- 3dB	
Saw Filter Ripple	< +/- 0.2 dB	
Preferred SAW Filter Shape	dB Bandwidth > 40 dB Rejection	5 MHz 6Mhz
Saw Filter Group Delay Variatio	< +/-20ns	
Acquisition Time:	<150 msec	Operating Condition is -15 dB, 600 ns multipath, 33dB SNR
	<100msec	Operating Condition is -77 dBc @10 KHz phase noise, 33dB SNR
Dynamic multipath	Single multipath at 1 usec: -20 dBc, phase rotation = 5 Hz.	
AGC Voltage	0-3.3 Volts	

Detailed Register Description

Program Registers

Table 3 Program Register Table

Register Name	Addr	Pos	Description	
EQUALIZER CENTER TAP	1	[3:0]	**d7**	Equalizer center tap location
AGC POWER REFERENCE	2	[7:0]	**d64**	Power Reference for AGC
AGC LOW LIMIT	3	[7:0]	**d128**	Lower limit of the AGC control voltage. Default value in signed number system corresponds to -128 and will produce 0 volts.
AGC HIGH LIMIT	4	[7:0]	**d127**	Upper limit of the AGC control voltage. Default value in signed number system corresponds to 127 and will produce 3.3 volts.
AGC JAM VALUE	5	[7:0]	**0**	Value to be jammed in AGC sigma-delta modulator. The value is jammed using JAM AGC register.
VCXO LOW LIMIT	6	[7:0]	**d128**	Lower limit of the VCXO control voltage. Default value in signed number system corresponds to -128 and will produce 0 volts.
VCXO HIGH LIMIT	7	[7:0]	**d127**	Upper limit of the VCXO control voltage. Default value in signed number system corresponds to 127 and will produce 3.3 volts.
VCXO JAM VALUE	8	[7:0]	**0**	Value to be jammed in VCXO sigma-delta modulator. The value is jammed using JAM VCXO register.
AGC INVERT	9	[0:0]	**0**	Pos. External AGC gain slope
			1	Neg. External AGC gain slope
AGC LOCK ENABLE	9	[1:1]	0	Updating of Equalizer is always done regardless of AGC lock.
			1	Updating of Equalizer is done only when AGC lock is achieved.
AGC GAIN	9	[3:2]	00	Fast AGC loop gain
			01	Medium fast
			10	Medium slow
			11	Slow AGC Loop Gain
JAM AGC	9	[4:4]	**0**	Normal Operation
			1	AGC control voltage jammed
INPUT SIGNAL TYPE	9	[5:5]	**0**	input is unsigned (0 to 255)
			1	input is signed(-128 to 127)
VCXO POLARITY	10	[0:0]	0	Neg. xfer function VCXO slope
			1	Pos. xfer function VCXO slope
BIT SYNC LOCK_ENABLE	10	[1:1]	0	Constant timing loop gain
			1	Lowered loop gain in lock mode.
BIT SYNC GAIN	10	[2:2]	0	High VCXO loop gain
			1	Low

Register Name	Addr	Pos	Description	
JAM VCXO	10	[3:3]	**0**	Normal Operation
			1	VCXO control voltage jammed
EQUALIZER UPDATE DISABLE	11	[2:2]	**0**	Normal Operation (Equalizer Updated)
			1	Equalizer Frozen
DDAGC DISABLE	11	[3:3]	**0**	Normal Operation (Digital AGC Updated)
			1	Digital AGC disabled
AUTO RESET DISABLE	11	[4:4]	**0**	Auto reset is enabled System will automatically perform a soft reset if carrier lock is not achieved in about 4 seconds
			1	Auto reset is disabled
SWAP IQ OUTPUT	12	[0:0]	**0**	I and Q outputs not swapped
			1	I and Q outputs swapped
RESERVED1	12	[2:1]	**11**	This reserved register must be programmed to “11”
FLL ENABLE	13	[0:0]	**0**	Frequency Lock Loop in Carrier Recovery disabled
			1	Frequency Lock Loop enabled
FLL GAIN	13	[2:1]	**00**	High Frequency Lock Loop Gain
			01	Medium High
			10	Medium Low
			11	Low
FREQUENCY RANGE	13	[3:3]	**0**	+/- 150 kHz Range for Carrier Recovery
			1	+/- 300 kHz Range for Carrier Recovery
Carrier Recovery lock mode PLL 1st order gain	14	[3:2]	**00**	high gain
			01	medium high
			10	medium low
			11	low gain
Carrier Recovery lock mode PLL 2nd order gain	14	[1:0]	00	high gain
			01	medium high
			10	medium low
			11	low gain
Q64 MSE lock/nolock Threshold	15	[7:0]	**d92**	Mean square sliced error compared to this value for 64 QAM. lock condition is set if average error is below this limit.
Q256 MSE lock/nolock Threshold	16	[7:0]	**d28**	Mean square sliced error compared to this value for 256 QAM. lock condition is set if average error is below this limit.
TONE CANCELER DISABLE	18	[0:0]	**0**	Enable Tone Canceler
			1	Disable Tone Canceler
TONE CANCEL PF	18	[1:1]	**0**	Tone canceler Pre-filter enabled

Register Name	Addr	Pos	Description	
DISABLE			1	Tone Canceler Pre-filter disabled
TONE CANCELER PREFILTER QUADRANT	18	[3:2]	**00**	-1.75 MHz w.r.t Carrier Freq (NTSC co-channel quadrent)
			01	+2.0 Mhz w.r.t. Carrier Freq
			10	-0.5 Mhz w.r.t. Carrier Freq
			11	0.75 Mhz w.r.t Carrier Freq
IMPULSE BLANKER ENABLE	19	[0:0]	0	Disable Impulse blanker
			1	Enable Impulse blanker
Impulse detection Multiplies	20	[7:6]		scale factor used for dynamic impulse detection circuit.
			00	Large multiplier
			01	medium large
			10	medium low
			11	Low multiplier
Impulse detection Threshold limit (256 QAM)	20	[3:2]	00	Large limit
			01	medium large
			10	medium small
			11	Small limit
Impulse detection Threshold limit (64 QAM)	20	[1:0]	00	Large limit
			01	medium large
			10	medium small
			11	Small limit
ACQUISITION MODULUS	21	[7:0]	**d84**	Radius square size of constellation, below which during acquisition, no carrier updating occurs.
REED_SOLOMON FREEZE	22	[0:0]	**0**	Reed-Solomon Decoder is frozen
			1	
REED-SOLOMON BYPASS	23	[0:0]	**0**	Reed-Solomon decoder is bypassed.
			1	
TRELLIS RESYNC ENABLE	24	[0:0]	0	Resynchronization is disabled.
			1	Allows the trellis decoder to resynchronize itself automatically, using either manual or automatic renormalization threshold as the criterion
TRELLIS RESYNC FORCE	24	[1:1]	**0**	Automatic resynchronization is disabled
			1	Puncture synchronization will automatically retard by one state
TRELLIS AUTOTHRESH	24	[2:2]	0	A manually set renormalization rate threshold is used as a criterion for resynchronization.
			1	The automatic renormalization rate threshold circuit is used to determine the renormalization rate threshold used as a criterion

Register Name	Addr	Pos	Description	
				for resynchronization
EXT IQ INPUT	24	[3:3]	**0**	IQ_SYMBOL[7:0] port acts as a output, allowing output of QAM demodulator to appear on this port
			1	IQ_SYMBOL[7:0] port acts as a input, allowing external IQ data to be fed to FEC decoder.
IQ MASK DISABLE	24	[4:4]	**0**	IQ symbols are masked, so that IQ_SYMBOL[7:0] port does not toggle.
			1	IQ symbols are not masked, allowing IQ symbols to appear on IQ_SYMBOL[7:0] port
MANUAL RENORM THRESHOLD	25	[7:0]	**d45**	This register is used to program a manual renormalization rate threshold used as a criterion for resynchronization
TRELLIS MAX CONF	26	[3:0]	**d3**	This register is the maximum value used in the up/down counter associated with automatic resynchronization. It is used when TR_RESYNC_EN is high
TRELLIS AUTO THRESHOLD	26	[7:4]	**d8**	This register is the offset number used in the automatic renormalization rate threshold calculation
FRAMESYNC LOCK THRESHOLD	27	[3:0]	**d1**	Number of successive hits required before frame sync will be considered locked.
FRAMESYNC UNLOCK THRESHOLD	27	[7:4]	**d4**	Number of successive miss-hits required before frame sync will be considered unlocked
MPEG LOCK THRESHOLD	28	[3:0]	**d5**	Number of successive hits required before MPEG sync recovery is considered locked
MPEG UNLOCK THRESHOLD	28	[7:4]	**d9**	Number of successive mis-hits required before MPEG sync recovery is considered unlocked
DERANDOMIZER BYPASS	29	[0:0]	**0**	Normal operation
			1	De-randomizer Bypassed
DEINTERLEAVER BYPASS	29	[1:1]	**0**	Normal operation
			1	De-interleaver Bypassed
MPEG BYPASS	29	[2:2]	**0**	Normal operation
			1	MPEG Sync recovery Bypassed
MPEG ERROR INSERTION	29	[3:3]	**0**	MPEG packet header is not modified when there is an error
			1	Error bit in MPEG packet header is set when there is an error.
SERIAL OUT ENABLE	29	[4:4]	**0**	FEC output is byte-wide (parallel)
			1	FEC output is bit-wide(serial)
FRAME SYNC TEST	29	[5:5]	**0**	Normal Operation
			1	Test mode for frame sync

Register Name	Addr	Pos	Description	
MCNS PID0	30	[4:0]	**d15**	MCNS PID1 and MCNS PID0 form a single 13 bit register called MCNS PID (MCNS PID0 supplies 5 least significant bits).
MCNS PID1	31	[7:0]	**d254**	When the PID of a MPEG packet matches this register, the MCNS_PID output is asserted during the MPEG packet.

Status Registers

Table 4 Status Registers

Register Name	Addr	Position	Description
REV NUMBER	0	[4:0]	QAM demod chip rev number
VCXO CONTROL	35	[7:0]	VCXO control signal, used for monitoring bit timing circuit
AGC CONTROL	36	[7:0]	AGC control signal, used for monitoring AGC circuit
AGC LOCK	37	[0:0]	AGC lock (0=F, 1=T)
BIT SYNC LOCK	37	[1:1]	Bitsync Lock (0=F, 1=T)
SIGNAL POWER	38	[7:0]	Average Absolute input signal power after A/D
CARRIER LOCK	39	[0:0]	Indicates Carrier is acquired and locked
QAM TYPE	39	[1:1]	Indicates chosen QAM type. 1=Q256, 0=Q64
AVG ERROR LSB	40	[7:0]	This 16 bit register contains the sliced error value summed over 4096 symbols (used for SNR estimation)
AVG ERROR MSB	41	[7:0]	
FREQ OFFSET	42	[7:0]	Frequency offset of carrier recovery loop.
TONE CANCEL I	43	[7:0]	
TONE CANCEL Q	44	[7:0]	
TC COEFF I	45	[7:0]	
TC COEFF Q	46	[7:0]	
DDAGC GAIN	47	[7:0]	Value of fast internal AGC gain control.
PHASE ERROR	48	[7:0]	Indicates instantaneous value of phase error. This register is meaningful only when averaged over large sample size.
IMPULSE COUNT MSB	49	[7:0]	Number of impulses counted over last 2^{12} symbols.
IMPULSE COUNT LSB	50	[7:0]	
IMPULSE EVENT	51	[7:0]	This indicates that current symbol was interpreted as an impulse. This is meaningful only when viewed in real time using blast mode.
NUMBER OF PACKETS1	52	[7:0]	These 2 registers form a single register with NUMBER OF PACKETS1 supplying the MSBs. This register shows the number of packets over which statistics are taken
NUMBER OF PACKETS0	53	[7:0]	
PACKET ERROR1	54	[7:0]	These 2 registers form a single register with PACKET ERRORS2 supplying the MSBs. This register indicates the number of packet errors.

Register Name	Addr	Position	Description
PACKET ERROR0	55	[7:0]	
BAD PACKET1	56	[7:0]	These 2 registers form a single register with BAD PACKET1 supplying the MSBs. This register indicates the number of bad packets.
BAD PACKET0	57	[7:0]	
SYM ERRORS2	58	[7:0]	These 3 registers form a single register with SYM ERRORS2 supplying the MSBs. This register indicates the number of symbol errors.
SYM ERRORS1	59	[7:0]	Number of erroneous symbols
SYM ERRORS0	60	[7:0]	
BIT ERRORS2	61	[7:0]	These 3 registers form a single register with BIT ERROR2 supplying the MSBs. This register indicates the number of bit errors.
BIT ERRORS1	62	[7:0]	
BIT ERRORS0	63	[7:0]	
ITAP[1]	64	[7:0]	In-Phase tap weight of Adaptive Equalizer (tap [1])
QTAP[1]	65	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[2]	66	[7:0]	""
QTAP[2]	67	[7:0]	""
ITAP[3]	68	[7:0]	""
QTAP[3]	69	[7:0]	""
ITAP[4]	70	[7:0]	""
QTAP[4]	71	[7:0]	""
ITAP[5]	72	[7:0]	""
QTAP[5]	73	[7:0]	""
ITAP[6]	74	[7:0]	""
QTAP[6]	75	[7:0]	""
ITAP[7]	76	[7:0]	""
QTAP[7]	77	[7:0]	""
ITAP[8]	78	[7:0]	""
QTAP[8]	79	[7:0]	""
ITAP[9]	80	[7:0]	""
QTAP[9]	81	[7:0]	""
ITAP[10]	82	[7:0]	""
QTAP[10]	83	[7:0]	""

Register Name	Addr	Position	Description
ITAP[11]	84	[7:0]	""
QTAP[11]	85	[7:0]	""
ITAP[12]	86	[7:0]	"" .....(tap[12])
QTAP[12]	87	[7:0]	"" .....(tap[12])
TRELLIS RENORM RATE	88	[7:0]	This status register provides a number indicative of how often the cumulative sums are being renormalized.
RENORM RATE AUTO	89	[7:0]	This status register provides the automatically-generated renormalization rate threshold.
FRAME SYNC LOCK	90	[0:0]	Indicates MCNS Frame Sync is acquired
MPEG LOCK	90	[1:1]	Indicates MPEG Sync Recovery is locked
DEINT MODE	91	[3:0]	Indicates current De-interleaver mode.

Testability Registers

Table 5 Testability Register Table

Register Name	Addr	Pos	Description	
DEINT MEM ADDR0	92	[7:0]	**d0**	These registers are concatenated to form a single 13 bit register. This acts as the address pointer register for the De-interleaver RAM
DEINT MEM ADDR1	93	[4:0]	**d0**	
DEINT MEM DATA0	94	[7:0]	**d0**	These registers are concatenated to form a single 14 bit register This is used as a data register for the De-interleaver RAM.
DEINT MEM DATA1	95	[5:0]	**d0**	When this register is accessed, address pointer register for this RAM is auto incremented.
PNTR MEM ADDR	96	[7:0]	**d0**	Address pointer register for pointer memory
PNTR MEM DATA	97	[7:0]	**d0**	Data register for the Pointer memory When this register is accessed, address pointer register for this RAM is auto incremented
MPEG MEM ADDR	98	[7:0]	**d0**	Address pointer register for the MPEG memory
MPEG MEM DATA	99	[7:0]	**d0**	Data register for the MPEG memory. When this register is accessed, address pointer register for this RAM is auto incremented
RS MEM ADDR	100	[7:0]	**d0**	Address Pointer register for the RS Memory
RS MEM DATA	101	[7:0]	**d0**	Data register for the RS memory. When this register is accessed, address pointer register for this RAM is auto incremented
DEINT OVERRIDE	102	[0:0]	**0**	Normal Operation
			1	To access De-interleaver RAM using uP I/f
PNTR OVERRIDE	102	[1:1]	**0**	Normal Operation
			1	To access Pointer RAM using uP I/F
RS OVERRIDE	102	[2:2]	**0**	Normal Operation
			1	To access Reed-Soloman RAM using uP I/F
MPEG OVERRIDE	102	[3:3]	**0**	Normal Operation
			1	To access MPEG RAM using uP I/F
AUTO INC DISABLE	102	[4:4]	**0**	Normal Operation
			1	Disable Auto-increment of Address pointer
RC BYPASS	102	[5:5]	**0**	Normal Operation
			1	Bypass Rate Equalizer
VCO BYPASS	102	[6:6]	**0**	Normal Operation

Register Name	Addr	Pos	Description	
			1	Bypass VCO (use external serial clock)
SLPN	102	[7:7]	**0**	Normal Operation
			1	Disable Analog Current Sources

PACKAGE I/O

Detailed Pin Description

Table 6 Pin Description Table

Name	I/O	Description	Num
Downstream Channel Pins(43)			
SIG_IN[9:0]	I	Sampled input signal (From A/D Converter.) Can be signed or unsigned	10
CLK4XOUT	O	4x Symbol clock for external A/D.	1
DAGC_SL	O	Sigma-Delta modulated control output. This signal is externally low-pass filtered and then used to control gain of an analog AGC amplifier or attenuator.	1
VCXO_SL	O	Sigma-Delta modulated control output. This signal is externally low pass filtered and then used to control the frequency of a VCXO.	1
SYMBOL_IQ[7:0]	BI	In-phase and Quadrature Phase soft decision output (Multiplexed) in output mode. Parallel FEC input in input mode.	8
LOCK	O	Carrier Recovery Lock Indicator	1
QAM_64	I	Selects between 64 and 256 QAM. 64 QAM when high.	1
MASTER_CLK64	I	The clock input is 4x Symbol rate (64 QAM)	1
MASTER_CLK64X	O	Clock Output. (64 QAM)	1
MASTER_CLK256	I	The clock input is 4x Symbol rate (256 QAM)	1
MASTER_CLK256X	O	Clock Output (256 QAM)	1
EXT_SER_CLK	I	External serial clock input. (Used when internal serial clock is disabled.)	1
CLK_10M	O	2x Symbol clock	1
CLK_5M	O	1X Symbol clock.	1
CLK_SERIAL	O	Serial Bit-rate clock	1
DATA_OUT	O	Error Corrected Data Output	8
DATA_EN	O	Indicates a new byte on DATA_OUT(Byte Sync)	1
SYNC	O	Indicates position of MPEG Sync Byte	1
MCNS_PID	O	Indicates that the current MPEG transport packet is a MCNS packet (based on the PID programmed internally).	1
UNCORRECTABLE	O	Indicates Error	1
Downstream uP Interface Pins(14)			
SELI2C	I	Selects I^2C mode for Downstream control Interface when high. Selects GP uP when low.	1
CS_BAR[SCL]	I	Chip Select Input for general purpose uP interface when SELI2C is low.	1

		I^2C Clock input when SELI2C is high.	
GP_READ	I	Read/Write indicator for general purpose uP I/F	1
READY_BAR	O	Open Drain Output for general purpose uP I/F. De-assertion (low) of this signal after start of a transaction indicates to the master that the slave chip is ready to complete the transaction.	1
ADREGEN	I	Chooses accessing of internal address pointer register or the register pointed to for general purpose uP I/F	1
BLAST_MODE_BAR	I	Allows a selected internal register to drive the D[7:0] port continuously.	1
MICRODATA[7:0]	Bi	General Purpose uP Interface bi-directional Data bus when SELI2C is low. MICRODATA[0] acts as I^2C Data I/O when SELI2C is high. MICRODATA[7:1] acts as I^2C Device address input.	8
Downstream Control Pins(3)			
RESET_BAR	I	Power-on Reset	1
SCAN_BAR	I	For Test Purposes only	1
TEST_BAR	I	For Test Purposes only	1
Analog Block Pins(2)			
CPOUT	I/O	VCO Filter Pin	1
RFREQ	I	VCO Frequency Setting Pin	1
POWER PINS (38)			
VDD	P		12
VSS	P		24
VCOAVDD	P	VCO Analog Power	1
VCOAVSS	P	VCO analog ground	1
NC			0
TOTAL			100

Package Pin Assignment

Table 7 Pin Assignment Table

Name	Package Pin No.
VSS	1
VSS	2
SIGNAL_IN[6]	3
SIGNAL_IN[7]	4
SIGNAL_IN[8]	5
SIGNAL_IN[9]	6
ADREGEN	7
RESET_BAR	8
MICRODATA[0]	9
vdd1	10
vss2	11
vddr1	12
MICRODATA[1]	13
MICRODATA[2]	14
MICRODATA[3]	15
MICRODATA[4]	16
MICRODATA[5]	17
MICRODATA[6]	18
MICRODATA[7]	19
READY_BAR	20
GP_READ	21
CS_BAR	22
DATA_OUT[0]	23
VSS	24
VSS	25
VSS	26
VSS	27
DATA_OUT[1]	28
DATA_OUT[2]	29
DATA_OUT[3]	30
DATA_OUT[4]	31
VDD	32
DATA_OUT[5]	33
VDD	34

Name	Package Pin No.
VSS	35
DATA_OUT[6]	36
DATA_OUT[7]	37
DATA_EN	38
SYNC	39
MCNS_PID	40
UNCORRECTABLE	41
CLK_SERIAL	42
VDD	43
VDD	44
VSS	45
BLAST_MODE_BAR	46
RFREQ	47
CPOUT	48
VSS	49
VSS	50
VSS	51
VSS	52
VCOAVSS	53
VCOAVDD	54
SELI2C	55
SCAN_MODE	56
TEST_BAR	57
SYMBOL_IQ[7]	58
SYMBOL_IQ[6]	59
SYMBOL_IQ[5]	60
VDD	61
SYMBOL_IQ[4]	62
SYMBOL_IQ[3]	63
SYMBOL_IQ[2]	64
SYMBOL_IQ[1]	65
VDD	66
VSS	67
SYMBOL_IQ[0]	68
X_MASTER_CLK64	69
X_MASTER_CLK64X	70
X_MASTER_CLK256	71

Name	Package Pin No.
X_MASTER_CLK256X	72
VSS	73
VSS	74
VSS	75
VSS	76
VSS	77
EXT_SER_CLK	78
QAM_64	79
CLK_10M	80
CAR_LOCK	81
VDD	82
VSS	83
CLK_5M	84
CLK_20M	85
VDD	86
VCXO_SL	87
VSS	88
DAGC_SL	89
SIGNAL_IN[0]	90
SIGNAL_IN[1]	91
SIGNAL_IN[2]	92
SIGNAL_IN[3]	93
VDD	94
SIGNAL_IN[4]	95
VDD	96
SIGNAL_IN[5]	97
VSS	98
VSS	99
VSS	100

Theory of Operation (Downstream Channel)

QAM Demodulator

Signal Processing

The HD49430F QAM demodulator uses the proven HD49428 QAM demodulator architecture, with significant enhancements. These include

- 10 bit input samples, and higher precision signal processing. This gives improved implementation loss which is important in case of 256QAM.
- Higher capture range of +/- 300kHz for the Carrier recovery loop. Setting the FREQUENCY RANGE register to '1' selects the higher capture range.
- Frequency Lock Loop for carrier recovery is implemented. This feature is selected by setting FLL ENABLE register to '1'. The gain of FLL is selected by the FLL GAIN register.
- 2 on-chip VCXO's are provided for generating 4x symbol clocks for 64 QAM and 256QAM. The clock is selectable using the QAM64 input pin. This pin also selects the QAM mode for signal processing circuits. **Since the clock is switched when a new QAM mode is selected, the chip must be reset using RESET_BAR pin after the QAM64 pin is toggled**.

QAM Interface

Demodulated QAM symbols are available on the SYMBOL_IQ[7:0] port I and Q symbols are multiplexed on this port as shown below.

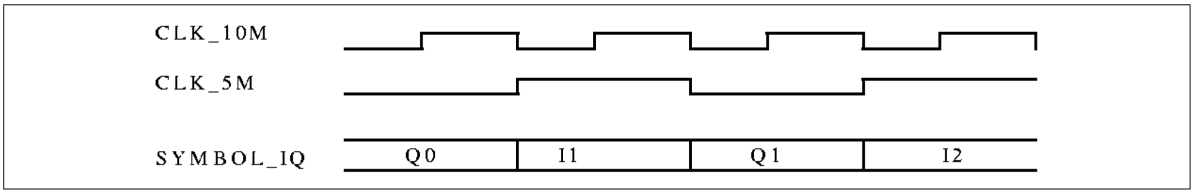


Figure 2 QAM Output Interface Timing

64 QAM Constellation: In 64 QAM mode, the demodulated 7 bit soft symbols are available on SYMBOL_IQ[7:1] pins. The 64 QAM constellation is shown below. The 7 bit values are represented as signed numbers with a range of -64 to +63.

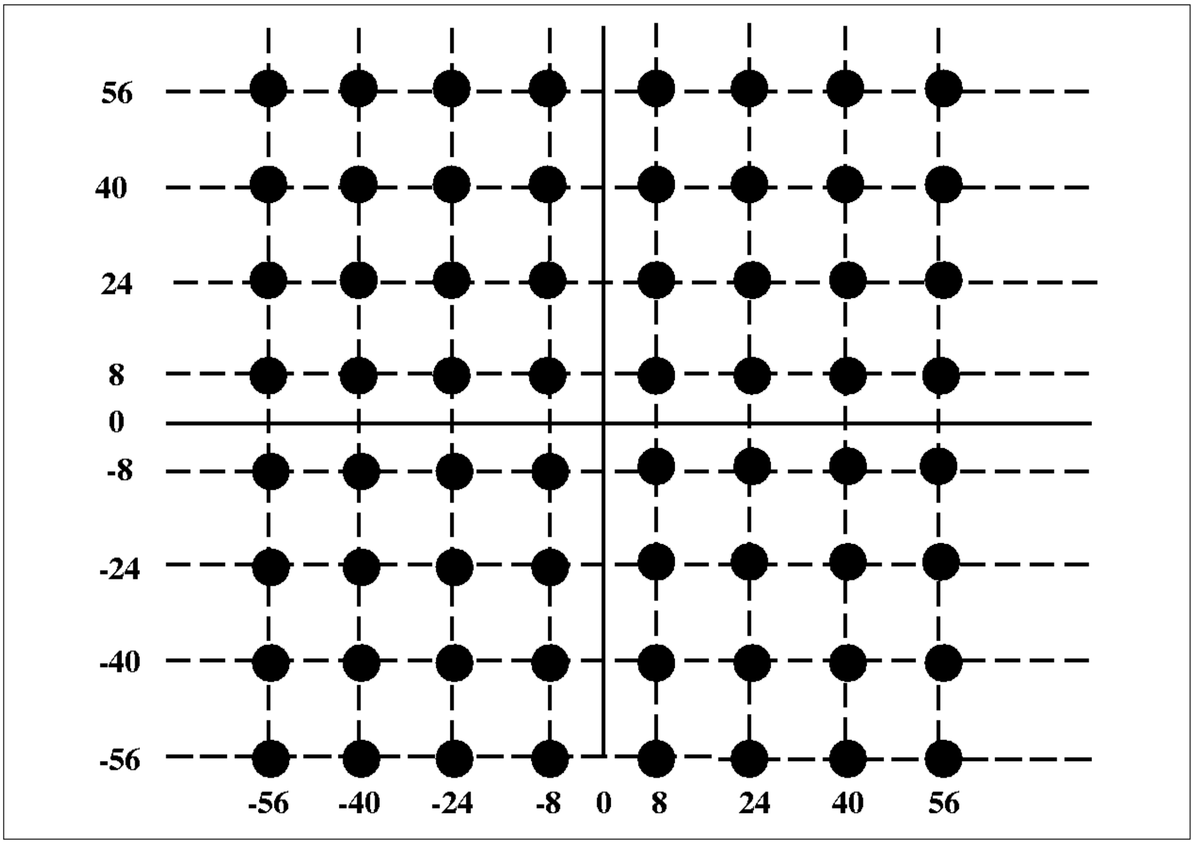


Figure 3 64 QAM Constellation

256 QAM Constellation: In 256 QAM mode, the demodulated 8 bit soft symbols are available on SYMBOL_IQ[7:0] pins. The 256 QAM constellation is shown below. The 8 bit values are represented as signed numbers with a range of -128 to +127.

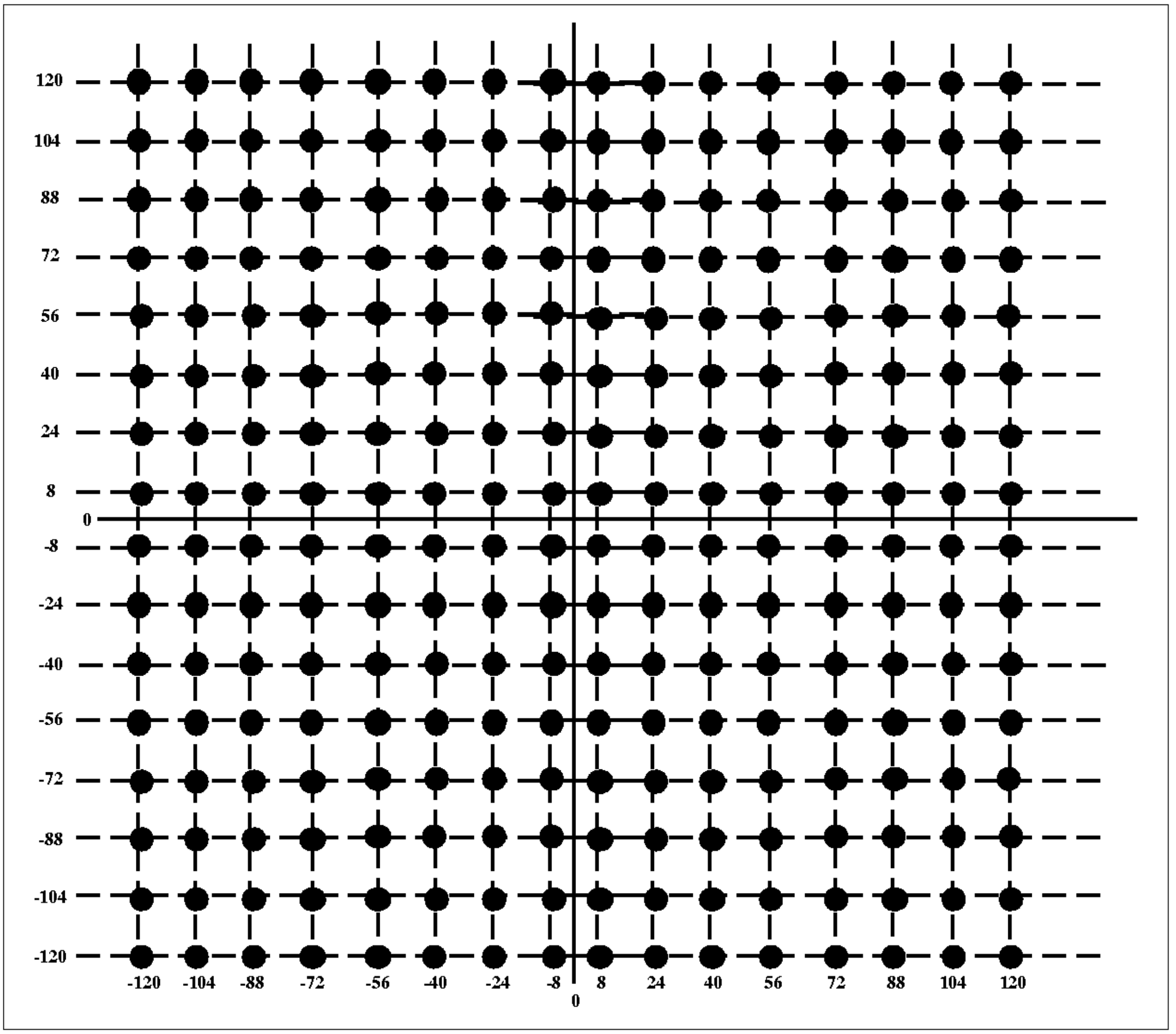


Figure 4 256 QAM Constellation

FEC Decoder

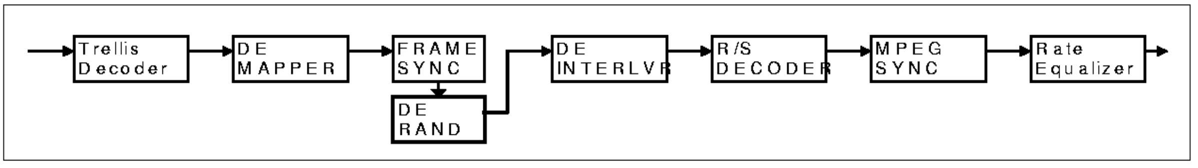


Figure 5 FEC Decoder Block Diagram

The above diagram is a simplified representation of the HD49430F FEC decoder system.

TRELLIS DECODER

DEMAPPER

The de-mapper takes the Trellis Decoder Output symbols , and maps into bits.

The Symbol-to-bits de-mapping depends on the QAM type of the incoming signal.

FRAME SYNCRONIZATION

The frame sync takes the de-mapped symbols and locates the frame syncs. A simple flywheel algorithm is used in the Sync detection to improve the noise immunity of this detector.

DE-RANDOMIZER

The 7 bit symbols obtained after frame synchronization are de-randomized using a MCNS compliant de-randomizer circuit.

DE-INTERLEAVER

The De-interleaver uses the synchronization from the frame sync circuit and de-interleaves the incoming symbol stream using the on-chip RAM The de-interleaving mode is automatically selected by the mode specified in the frame synchronization word.

REED_SOLOMON DECODER

MCNS Compliant Decoder.

MPEG SYNC RECOVERY

This block locates the encoded MPEG Sync using CRC checking, and aligns to original byte boundaries. If there is CRC error, it is indicated using the UNCORRECTABLE output pin, and will set the error bit in MPEG packet header if programmed to do so. This block also checks the MPEG PID, and if it matches the MCNS_PID register, then the MCNS_PID output is asserted while the MPEG packet with matching PID is being output.

RATE EQUALIZER

This block uses RAM buffering to convert stuttering data in the QAM Symbol Clock Domain to a uniform bit rate clock domain. The uniform bit-rate clock is generated on-chip using a PLL. The FEC data can be output either in serial(bit) or parallel(byte) mode.

FEC Interface

FEC Interface with Rate Equalization

The FEC Interface uses Rate Equalization when RC BYPASS signal is '0'. This is the default mode of the FEC interface. In the QAM symbol clock domain, the FEC decoder produces a stuttering data stream. In this mode, stuttering data stream is stored in a local buffer, and read out at a uniform rate using a Clock generated on-chip using PLL. The Interface is available as either a serial interface or a parallel interface. Further, the interface details will vary depending on whether the MPEG function is enabled or disabled.

Parallel Interface with MPEG Sync Recovery Enabled

The parallel interface with rate equalization and MPEG recovery is available when the SERIAL OUT ENABLE register is set to '0' and the RC BYPASS register is set to '0' and MPEG BYPASS is set to '0'. This is the default mode of the FEC interface. Following diagram describes the FEC interface.

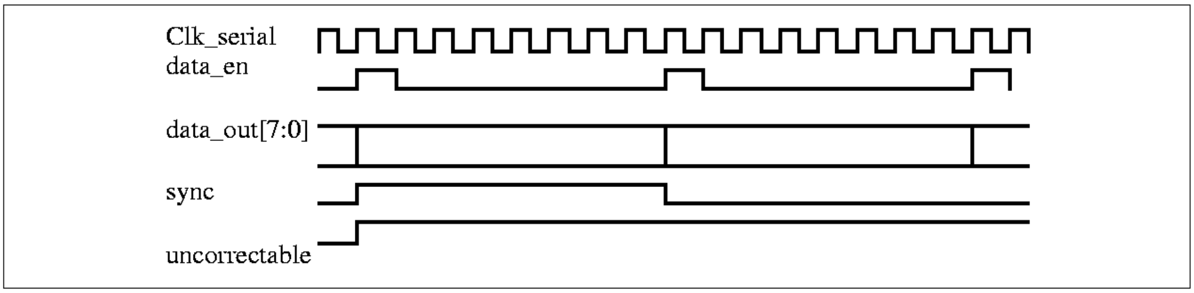


Figure 6 Parallel Output with Rate Equalization (MPEG enabled)

In this mode, the DATA_EN signals the availability of new data byte on DATA_OUT[7:0] port. The SYNC signal indicates a MPEG sync and UNCORRECTABLE signal indicates a MPEG packet error. The error signal is on during the entire duration of a MPEG packet.

Serial Interface with MPEG Sync Recovery Enabled

The serial interface with rate equalization and MPEG recovery is available when the SERIAL OUT ENABLE register is set to '1', the RC BYPASS register is set to '0' and MPEG BYPASS register is set to '0'. This is **not the default** mode of the FEC interface. Following diagram describes the FEC interface

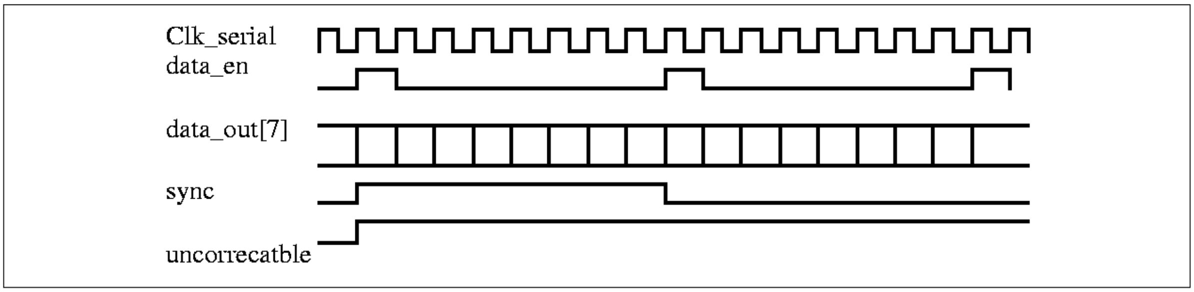


Figure 7 Serial Interface with Rate Equalization (MPEG Enabled)

In this mode, the DATA_OUT[7] pin has the serial FEC data and DATA_EN pin indicates the first bit of each byte. The SYNC signal indicates a MPEG sync and ERROR signal indicates a MPEG packet error. The error signal is on during the entire duration of a MPEG packet.

Parallel Interface with MPEG Sync Recovery Disabled

The parallel interface with rate equalization and without MPEG recovery is available when the SERIAL OUT ENABLE register is set to '0' and the RC BYPASS register is set to '0' and MPEG BYPASS is set to '1'. This is **not the default mode** of the FEC interface. Following diagram describes the FEC interface.

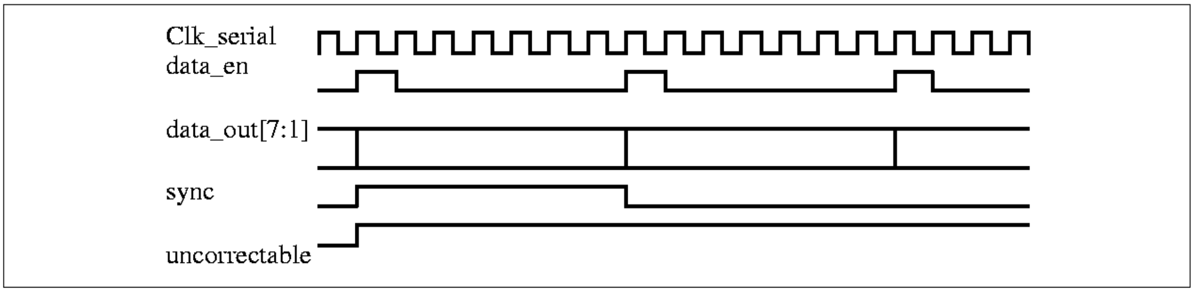


Figure 8 Parallel Interface with Rate Equalization(MPEG Disabled)

In this mode, the 7 bit FEC symbols appear on the DATA_OUT[7:1] pins, and DATA_EN indicates a new symbol. SYNC pin indicates start of a new FEC block and UNCORRECTABLE signal indicates an uncorrectable block. UNCORRECTABLE signal is on during the entire duration of a uncorrectable block.

Serial Interface with MPEG Sync Recovery Disabled

The serial interface with rate equalization and without MPEG recovery is available when the SERIAL OUT ENABLE register is set to '1' and the RC BYPASS register is set to '0' and MPEG BYPASS is set to '1'. This is **not the default mode** of the FEC interface. Following diagram describes the FEC interface.

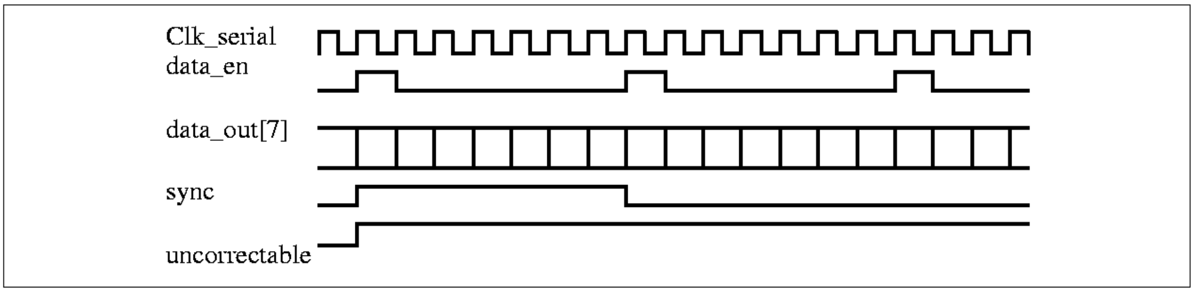


Figure 9 Serial Interface with Rate Equalization (MPEG Disabled)

In this mode, the 7 bit FEC symbols appear serially on the DATA_OUT[7] pin, and DATA_EN indicates the first bit of a symbol. SYNC pin indicates first symbol of a new FEC block and UNCORRECTABLE signal indicates an uncorrectable block. UNCORRECTABLE signal is on during the entire duration of a uncorrectable block.

FEC Interface without Rate Equalization

The FEC Interface does not use Rate Equalization when RC BYPASS signal is ‘1’. This is **not the default mode** of the FEC interface. In the QAM symbol clock domain, the FEC decoder produces a stuttering data stream. In this mode, stuttering data stream is read out directly. **The Interface is available only as a parallel interface in this mode**. Hence, the SERIAL OUT ENABLE register must be ‘0’. Further, the interface details will vary depending on whether the MPEG function is enabled or disabled

Parallel Interface with MPEG Sync Recovery Enabled

This mode is available when SERIAL OUT ENABLE is ‘0’ and MPEG BYPASS is ‘0’. Following diagram describes the FEC interface.

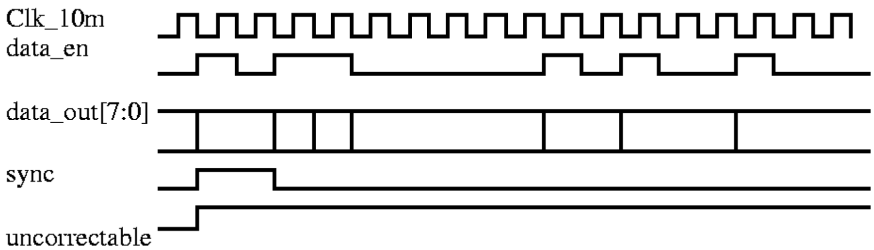


Figure 10 Parallel Interface with No Rate Equalization (MPEG Enabled)

In this mode, the output of the MPEG sync recovery circuit appears as bytes on the DATA_OUT[7:0] port. The DATA_EN pin indicates when a new byte is available. The SYNC signal indicates the MPEG sync byte. The UNCORRECTABLE signal goes high during the entire duration of a MPEG packet containing an error.

Parallel Interface with MPEG Sync Recovery Disabled

This mode is available when SERIAL OUT ENABLE is ‘0’ and MPEG BYPASS is ‘1’. Following diagram describes the FEC interface.

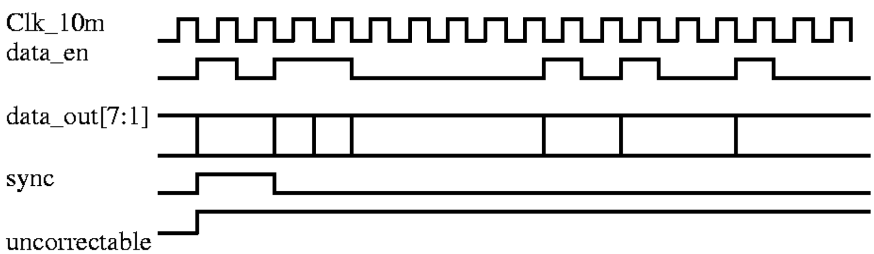


Figure 11 Parallel Interface with No Rate Equalization (MPEG Disabled)

In this mode, the output of the Reed-Solomon decoder circuit appears as 7-bit symbols on the DATA_OUT[7:1] port. The DATA_EN pin indicates when a new 7-bit symbol is available. The SYNC signal indicates the first 7-bit symbol of the FEC block. The UNCORRECTABLE signal goes high during the entire duration of a uncorrectable FEC block.

Control Interfaces

The programming and status registers can be accessed via the chip's control interface. For maximum System flexibility, a general purpose Microprocessor Interface and an I^2C (TM) compatible serial interface are available on the chip. The two interfaces share I/O pins, and only one Interface can be selected in a system implementation by hardwiring the SELI2C input appropriately. Details of each interface are given below.

General Purpose uP Interface

The following I/O pins constitute the uP Interface. The uP interface is available when the SELI2C pin is low. The following table gives a detailed description of the I/O pins involved.

Table 8 General Purpose uP Interface

Pin Name	Type	Description
CS_BAR	I	The chip select input activates a transaction. The type of the transaction is determined by the state of the GP_READ and ADREGEN pins. The READY_BAR output deasserts itself when the chip is ready to complete the transaction. The external micro-controller then finishes the transaction by de-asserting the CS_BAR pin.
GP_READ	I	This input indicates whether a transaction will be read or write transaction. In a read transaction, data from an on-chip register will be read by the external controller. In a write transaction, data will be written into one of the chip's on-chip registers.
ADREGEN	I	When this input is asserted during a write, data from the MICRODATA[7:0] bus is written into the on-chip address pointer register. When this input is de-asserted, an on-chip register pointed to by the address pointer register is read or written.
MICRODATA[7:0]	Bi	This bi-directional parallel bus is used to read and write on-chip registers.
READY_BAR	O	This is a tri-state output. It is driven only when the chip is selected (by asserting CS_BAR input). The chip indicates that it is ready to complete the transaction by de-asserting this pin. The transaction is formally complete when the external controller de-asserts CS_BAR input.
BLAST_MODE_BAR	I	This input pin is provided for implementation of special board level system debug modes. When the BLST_MODE_BAR pin is acteivated along with CS_BAR pin when GP_READ pin is high, the register pointed to by the address pointer register will become visible on MICRODATA bus in real time. These registers can then be viewed in real time using a oscilloscope or logic analyzer.

This interface uses an indirect addressing mode for accessing the on-chip registers. The Address Pointer Register acts as the pointer. Hence, a random register access typically will require 2 I/F transactions. During the first transaction, ADREGEN input is asserted, and the address of the register that needs to be accessed is written to the Address Pointer Register. During the next transaction, the appropriate register is accessed. However, if registers are to be accessed sequentially, then an auto-increment feature will allow one access per transaction for all subsequent sequential accesses. The auto-increment feature can be turned off by setting the AUTOINC_DISABLE register to ‘1’.

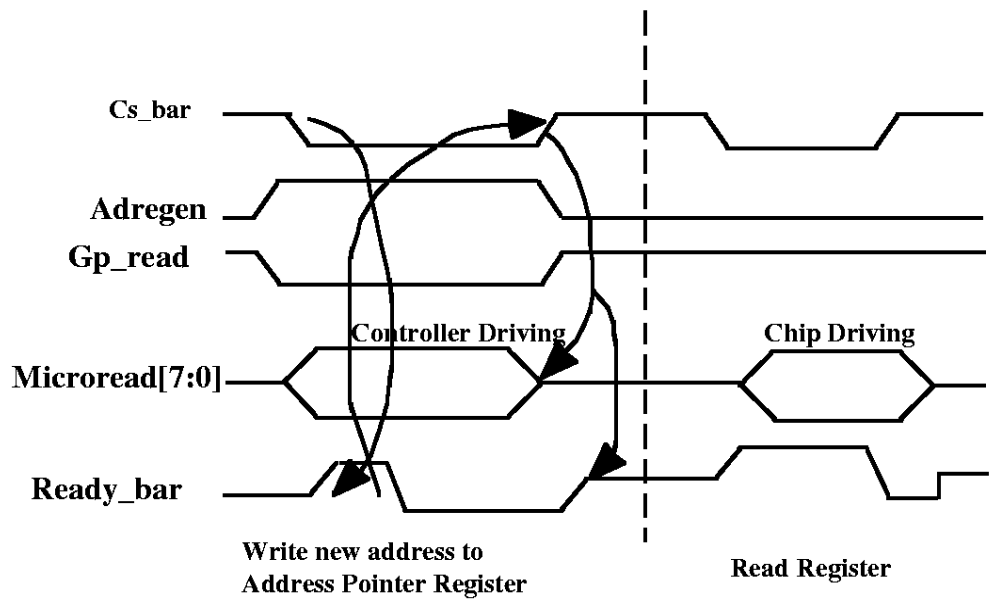


Figure 12 uP Interface Protocol

Serial Interface

The Serial interface is active when the SELI2Cinput pin is wired high. The serial interface is I^2C (TM) compatible and involves the following I/O pins.

Table 9 Serial Interface

Pin Name	Type	Description
SDA (MICRODATA[0])	I/O	This is the bi-directional data pin of the I^2C (TM) compatible serial interface.
SCL (CS_BAR)	I	This is the clock pin of the I^2C (TM) compatible interface. Since the chip is programmed to be a slave only, this is an input pin.

The I^2C compatible serial interface is configured to be a slave.

I^2C Protocol

The following figure describes the I^2C protocol that is implemented and timing relationship between various pins in a serial transfer. As shown, the SDA pin can change state during the low period of the SCL pin. The two exceptions to this rule occur during the start and stop conditions. During the "start" condition, SDA pin makes a high to low transition while the SCL pin is high. A low to high transition of SDA pin while SCL is high represents a "stop" condition. I^2C (TM) specification requires that each transaction is in multiples of 8 serial clocks with the MSB bit transmitted first. Each 8-bit transaction is ended by the receiver sending an acknowledgment by driving the SDA pin low as shown.

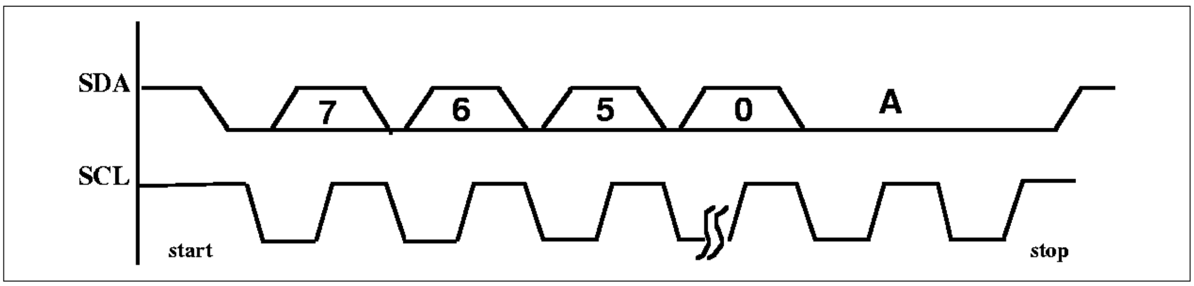


Figure 13 I^2C Serial Transfer

An I^2C serial transfer begins with a I^2C master (usually a micro-controller) starting a new transaction. Each such transaction is composed of multiple transfers, each of which involves a 8-bit serial transfer followed by an acknowledgment from the receiver, as described in the previous paragraph. The first serial transfer in a transaction involves the I^2C master broadcasting a 7-bit I^2C device address over the bus. The 8th bit of this transfer indicates the direction of subsequent transfers. A "1" indicates that the - I^2C master wants to read from a slave device and a "0" indicates that the - I^2C master wants to write to a slave device. The addressed device sends an acknowledgment if it is available. A typical transaction is shown in figure 4. The address byte (7 bits of address and read/write bit) is referred to as byte A. Subsequent data bytes are referred to as D0 to Dn. This terminology is used in all subsequent discussions.

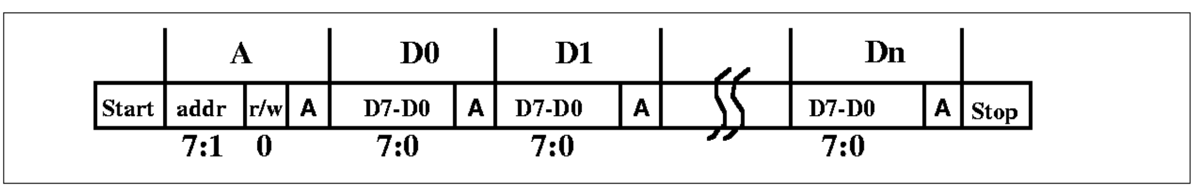


Figure 14 I^2C Address and Data Protocol

Programming Protocol

I^2C is a serial transfer protocol that specifies how bytes of data are transferred over a serial interface. However the interpretation of what these bytes mean and the specification of the order in which they are sent is unique to each system.

The HD49430F uses the I^2C bus to allow an external controller to access its on-chip registers. The on-chip registers are accessed using the address pointer register. A transaction can contain an arbitrary number of byte transfers. The direction of the transfer is set by the read/write bit (bit 0 in byte A).

Write Transactions: A transaction is determined to be a write transaction when bit A[0] equals "0". During a write transaction, data is written to HD49430F on-chip registers by the I^2C master. The 7 LSBs of the 1st data byte (D0) are written to the address pointer register. We will refer to this address as A0. Byte D1 is written to register A0, byte D2 is written to register A0 + 1 and so on.

Read Transactions: A transaction is determined to be a read transaction when bit A[0] equals "1". During a read transaction, data is read from HD49430F on-chip registers by the I^2C master. During the first data transaction, the 7 LSBs of data byte D1 read from HD49430F represent the contents of the address pointer register. We will refer to this address location as A0. Byte D1 represents data from register at location A0, byte D2 represents data from location A0 + 1 and so on.

The following table specifies the semantics.

Table 10 HD49430F Serial Protocol Specification

Byte Name	Specification (Write)	Specification (read)
A	This is the address byte with following specification A[7:1] : IIC slave address	
	A[0] = 0	A[0] = 1
D0	Byte is written to address pointer register and points to register A0.	Byte is read from address pointer register and points to register A0
D1	Byte is written to register at address A0	Byte is read from register at address A0
D2	Byte is written to register at address (A0 + 1)	Byte is read from register at address (A0 + 1)
D3	Byte is written to register at address (A0 + 2)	Byte is read from register at address (A0 + 2)
Dn	Byte is written to register at address (A0 + n - 1)	Byte is read from register at address (A0 + n - 1)

DC Characteristics

Table 11 Absolute Maximum Ratings

Parameter	Abs Maximum
Supply Voltage	4 V.
Input Voltage	-0.3 ~ VDD+0.3 V.
Operating Temperature	0 ~70°C
Storage Temperature	125° C

AC Characteristics

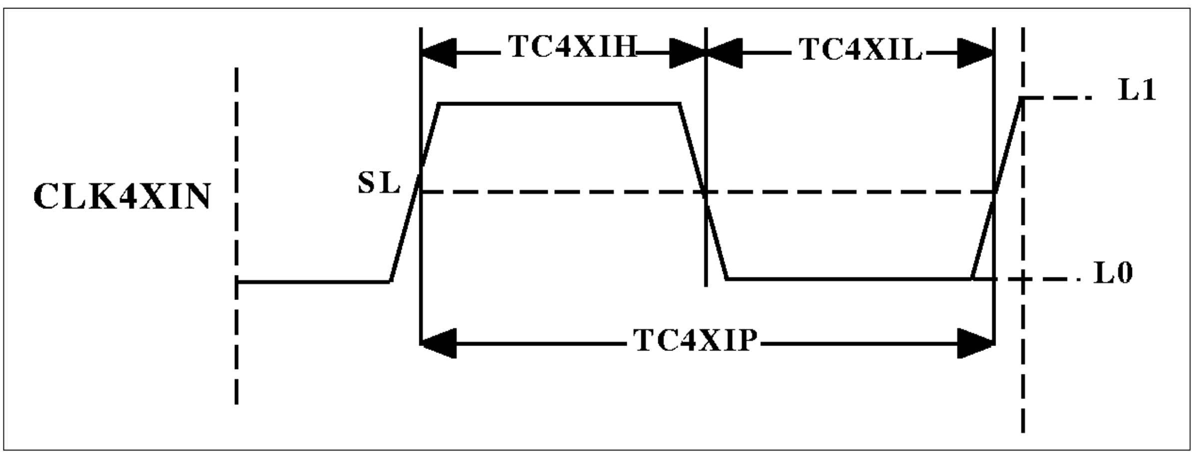


Figure 15 Clock Inputs

Table 12 Clock Inputs

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TC4XIP	MASTER_CLK64 MASTER_CLK256	46.29	49.43		ns	SL= 0.5Vdd L1 = 0.7Vdd	CLK4XIN Period
TC4XIH	MASTER_CLK64	15			ns	L0 = 0.3Vdd	CLK4XIN HighTime
TC4XIL	MASTER_CLK64	15			ns		CLK4XIN LowTime

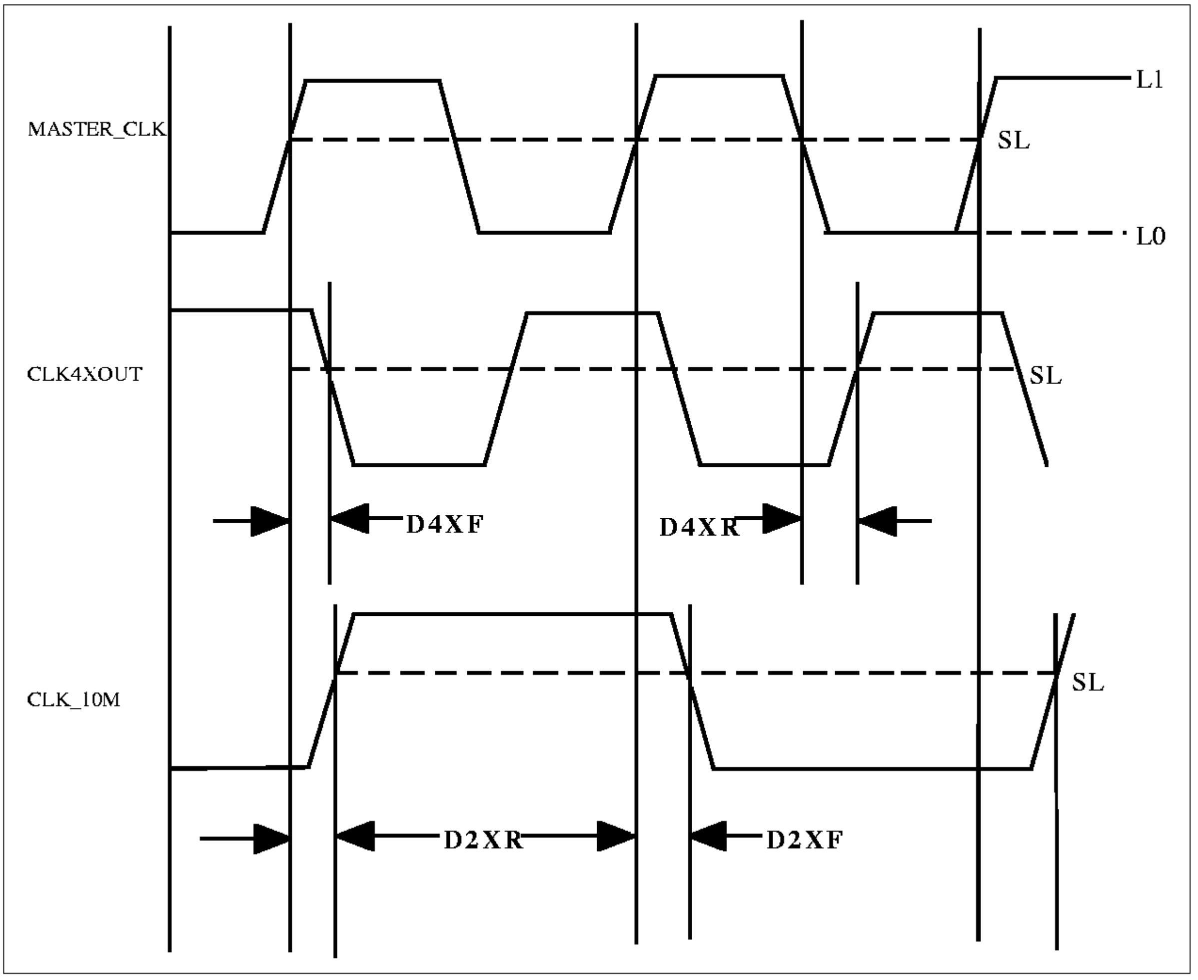


Figure 16 Clock Outputs

Table 13 Clock Outputs

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
D4XF	CLK4XOUT			28	ns	SL= 0.5Vdd Cload=30pf	Delay from rising edge of MASTER_CLK64 (MASTER_CLK256) to falling edge of CLK4XOUT.
D4XR	CLK4XOUT			28	ns	SL+0.5Vdd Cload=30pf	Delay from rising edge of MASTER_CLK 64(MASTER_CLK256) to falling edge of CLK4XOUT.
D4XM	CLK4XOUT	0		10	ns		Difference between D4XF and D4XR
D2XF	CLK_10M			18	ns	SL=0.5Vdd Cload=30pf	Delay from rising edge of MASTER_CLK64(MASTER_CLK256) to falling edge of CLK_10M.
D2XR	CLK_10M			18	ns	SL=0.5Vdd Cload=30pf	Delay from rising edge of MASTER_CLK64(MASTER_CLK256) to rising edge of CLK_10M.

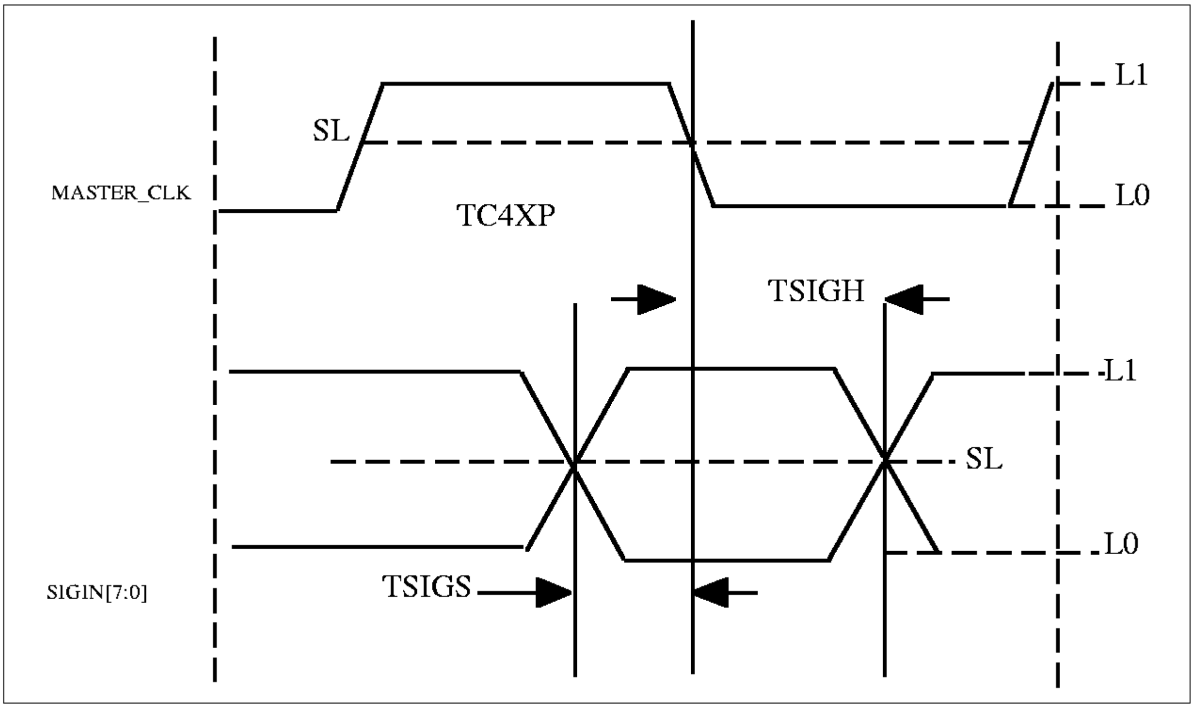


Figure 17 Input QAM Signal

Table 14 Input QAM Signal

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TSIGS	SIG_IN[7:0]	0			ns	SL= 0.5Vdd L1 = 0.7Vdd L0 = 0.3Vdd	Setup time of SIG_IN[[7:0] wrt Falling edge of MASTER_CLK64 or MASTER_CLK256
TSIGH	SIG_IN[7:0]	D4XR			ns		Hold time of SIG_IN[[7:0] wrt Falling edge of MASTER_CLK64 or MASTER_CLK256.

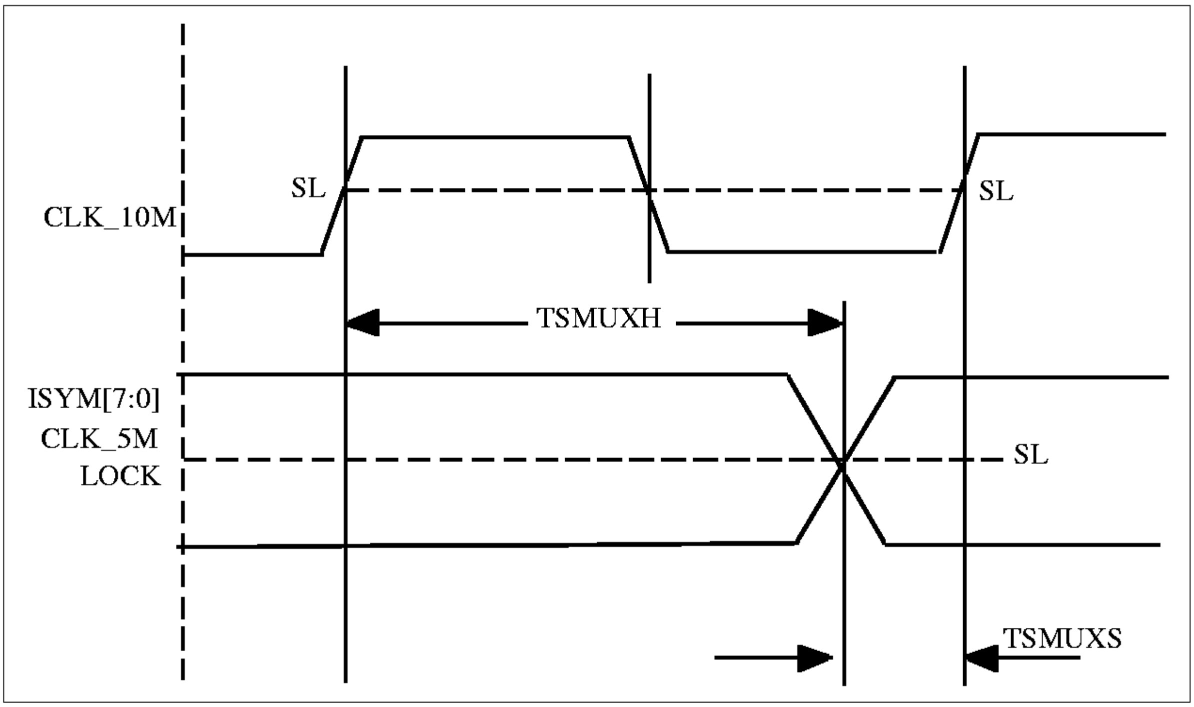
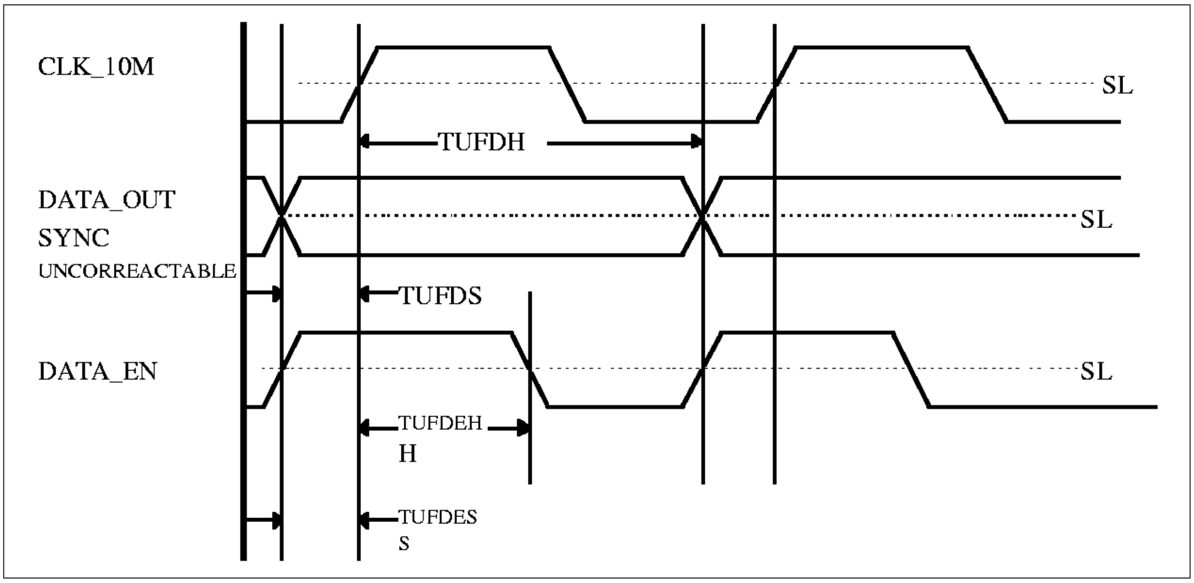


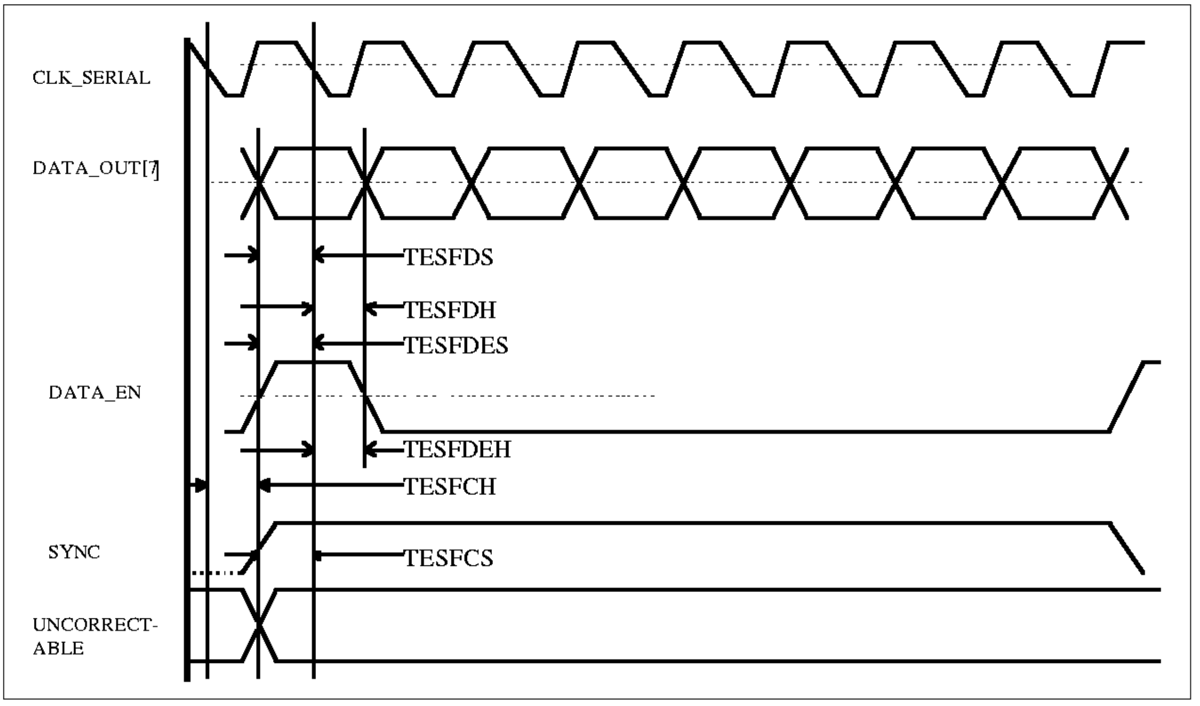
Figure 18 QAM Outputs

Table 15 QAM Outputs

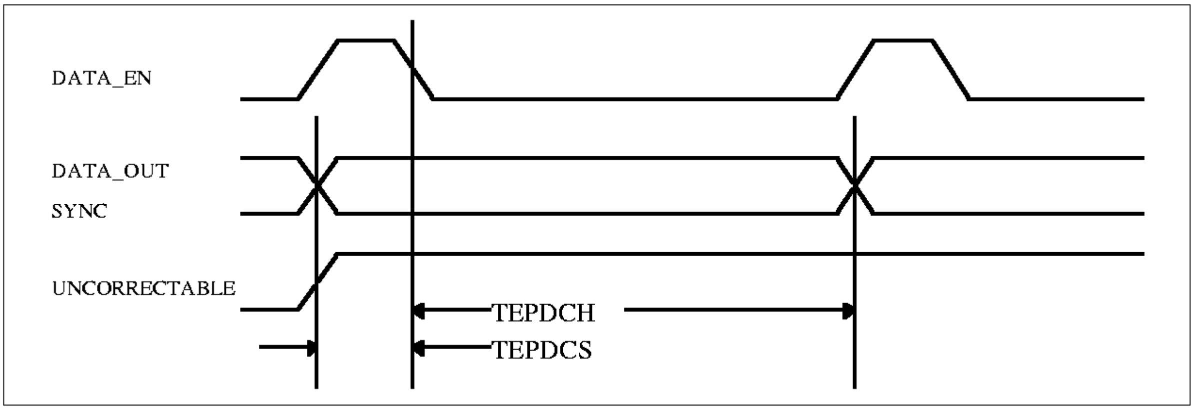
Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TSMUXS	SYMBOL_IQ[7:0] CLK_5M LOCK	20			ns	SL= 0.5Vdd Cload=30pf	Setup time of SYMBOL_IQ[7:0], CLK_5M and LOCK wrt rising edge of CLK_10M.
TSMUXH	SYMBOL_IQ[7:0] CLK_5M LOCK	20			ns		Hold time of SYMBOL_IQ[7:0], CLK_5M and LOCK wrt rising edge of CLK_10M.



Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TUFDS	DATA_OUT[7:0] SYNC UNCORRECTABLE	10			ns	SL= 0.5Vdd Cload=30pf	Setup time of DATA_OUT[7:0], SYNC and UNCORRECTABLE outputs wrt rising edge of CLK_10M
TUFDH	DATA_OUT[7:0] SYNC UNCORRECTABLE	20			ns	SL= 0.5Vdd Cload=30pf	Hold time of DATA_OUT[7:0], SYNC and UNCORRECTABLE outputs wrt rising edge of CLK_10M
TUFDES	DATA_EN	10			ns	SL= 0.5Vdd Cload=30pf	Setup time of DATA_EN wrt rising edge of CLK_10M
TUFDEH	DATA_EN	20			ns	SL= 0.5Vdd Cload=30pf	Setup time of DATA_EN wrt rising edge of CLK_10M



Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TESFDS	DATA_OUT[7:0]	5			ns	SL= 0.5Vdd Cload=30pf	Setup time of DATA_OUT[7] outputs wrt falling edge of CLK_SERIAL
TESFDH	DATA_OUT[7:0]	5			ns	SL= 0.5Vdd Cload=30pf	Hold time of DATA_OUT[7] outputs wrt falling edge of CLK_SERIAL
TESFDES	DATA_EN	5			ns	SL= 0.5Vdd Cload=30pf	Setup time of DATA_EN output wrt falling edge of CLK_SERIAL
TESFDEH	DATA_EN	5			ns	SL= 0.5Vdd Cload=30pf	Hold time of DATA_EN output wrt falling edge of CLK_SERIAL
TESFCS	SYNC UNCORRECTABLE	5			ns	SL= 0.5Vdd Cload=30pf	Setup time of SYNC and UNCORRECTABLE outputs wrt falling edge of CLK_SERIAL
TESFCH	SYNC UNCORRECTABLE	5			ns	SL= 0.5Vdd Cload=30pf	Setup time of SYNC and UNCORRECTABLE outputs wrt falling edge of CLK_SERIAL



Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TEPDCS	DATA_OUT[7:0] SYNC UNCORRECTABLE	10			ns	SL= 0.5Vdd Cload=30pf	Setup time of DATA_OUT[7:0], SYNC and UNCORRECTABLE outputs wrt falling edge of DATA_EN output
TEPDCH	DATA_OUT[7:0] SYNC UNCORRECTABLE	150			ns	SL= 0.5Vdd Cload=30pf	Hold time of DATA_OUT[7:0], SYNC and UNCORRECTABLE outputs wrt falling edge of DATA_EN output.

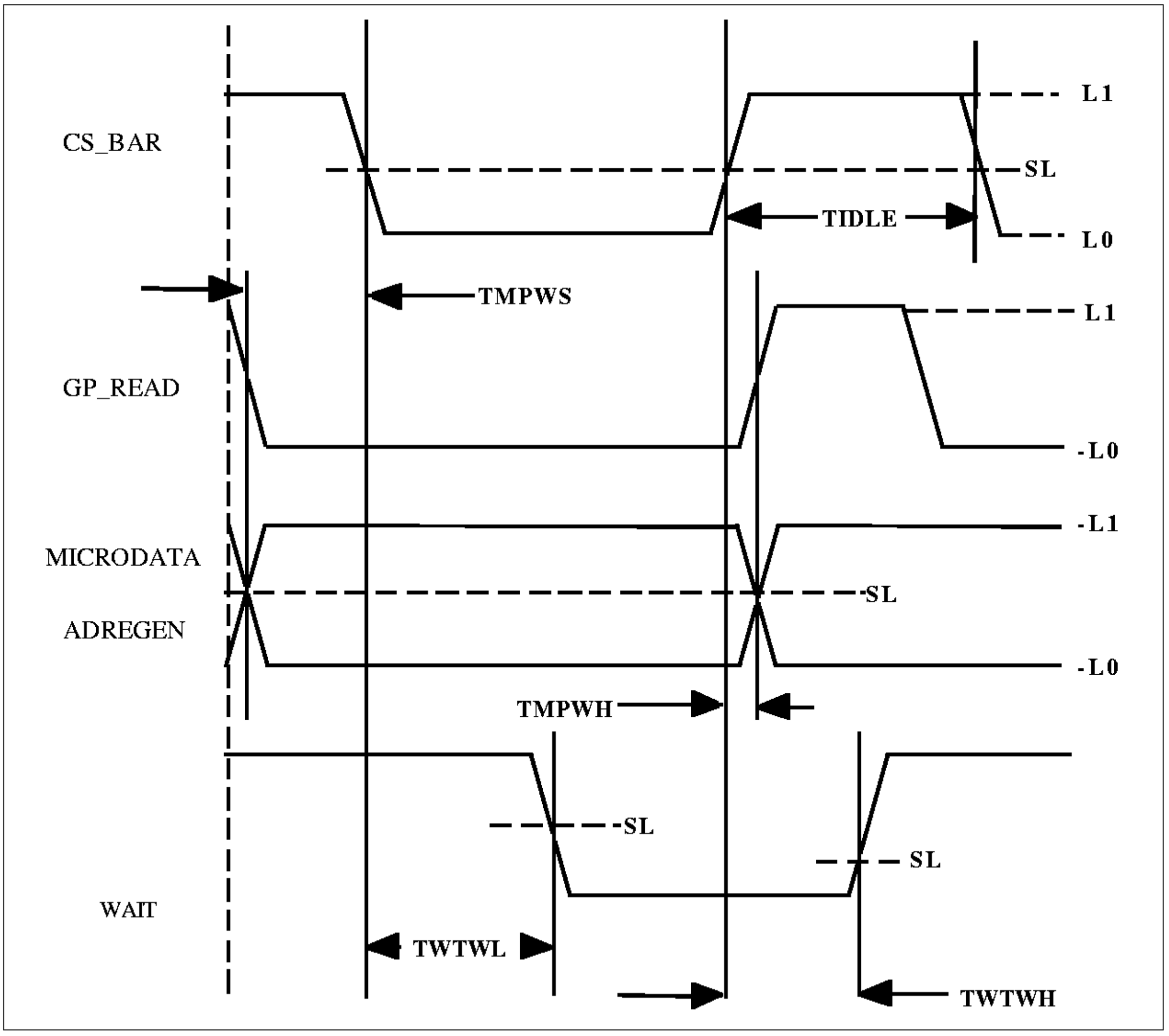


Figure 19 Microprocessor Write Cycle

Table 16 Microprocessor Write Cycle

Sym	Pin	Min	Typ	MAx	U	Test Conditions	Description
TMPWS	MICRODATA[7:0] ADREGEN GP_READ	TC4XIP			ns	SL= 0.5Vdd L1 = 0.7Vdd L0=0.3Vdd	Setup Time of GP_READ,ADREGEN, and MICRODATA[7:0] wrt CS_BAR.
TMPWH	MICRODATA[7:0] ADREGEN GP_READ	TC4XIP			ns		Hold Time of GP_READ,ADREGEN, and MICRODATA[7:0] wrt CS_BAR.
TWTWL	READY_BAR			TC4XIP *2 + 18	ns	SL=0.5Vdd Cload=100pf Rpullp = 1K	Delay from falling edge of CS_BAR to falling edge of READY_BAR.
TWTWH	READY_BAR			10	ns	Rpullup = 1K	Delay from rising edge of CS_BAR to rising edge of READY_BAR.
TIDLE	CS_BAR	TC4XIP *2			ns	SL= 0.5Vdd L1 = 0.7Vdd L0=0.3Vdd	Delay between consecutive microprocessor transactions.

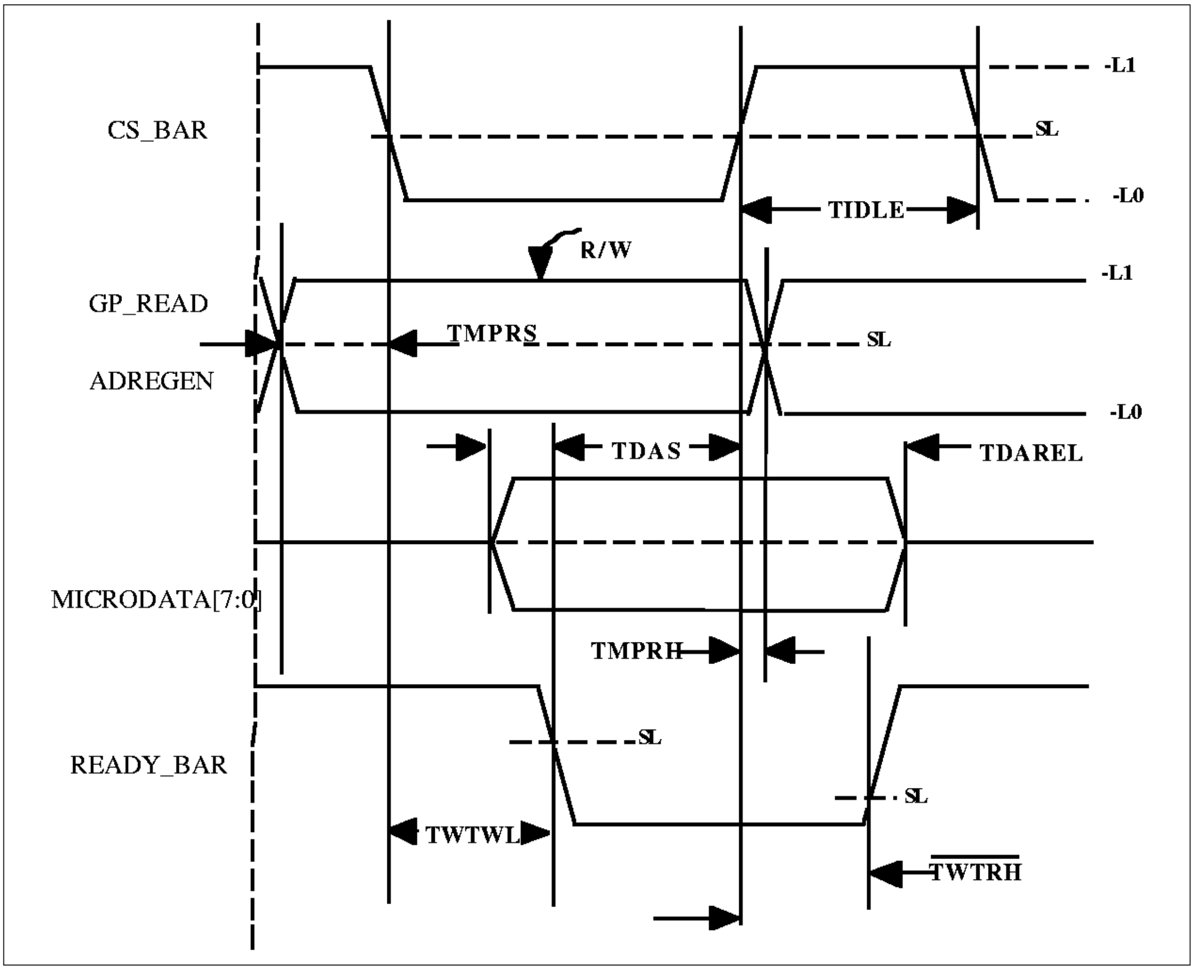


Figure 20 Microprocessor Read Cycle

Table 17 Microprocessor Read Cycle

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TMPRS	ADREGEN GP_READ	TC4XIP			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Setup Time of GP_READ,ADREGEN, and MICRODATA[7:0] wrt CS.
TMPRH	ADREGEN GP_READ	TC4XIP			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Hold Time of GP_READ,ADREGEN, and MICRODATA[7:0] wrt CS.
TWTRL	READY_BAR			TC4XIP *6+ 18	ns	SL=0.5Vdd Cload=100pf Rpullup=1K	Delay from falling edge of CS_BAR to falling edge of READY_BAR.
TWTRH	READY_BAR			10	ns	SL=0.5V Cload=100pf Rpullup=1K	Delay from rising edge of CS_BAR to rising edge of READY_BAR.
TDAS	MICRODATA[7:0]	0			ns	SL=0.5V Cload=100pf	Setup time of DATA[7:0] wrt falling edge of READY_BAR.
TDAREL	MICRODATA[7:0]	10			ns	SL=0.5V Cload=100pf	Delay between rising edge of CS_BAR and tristating of MICRODATA
TIDLE	CS_BAR	TC4XIP *2			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Delay between consecutive microprocessor transactions.

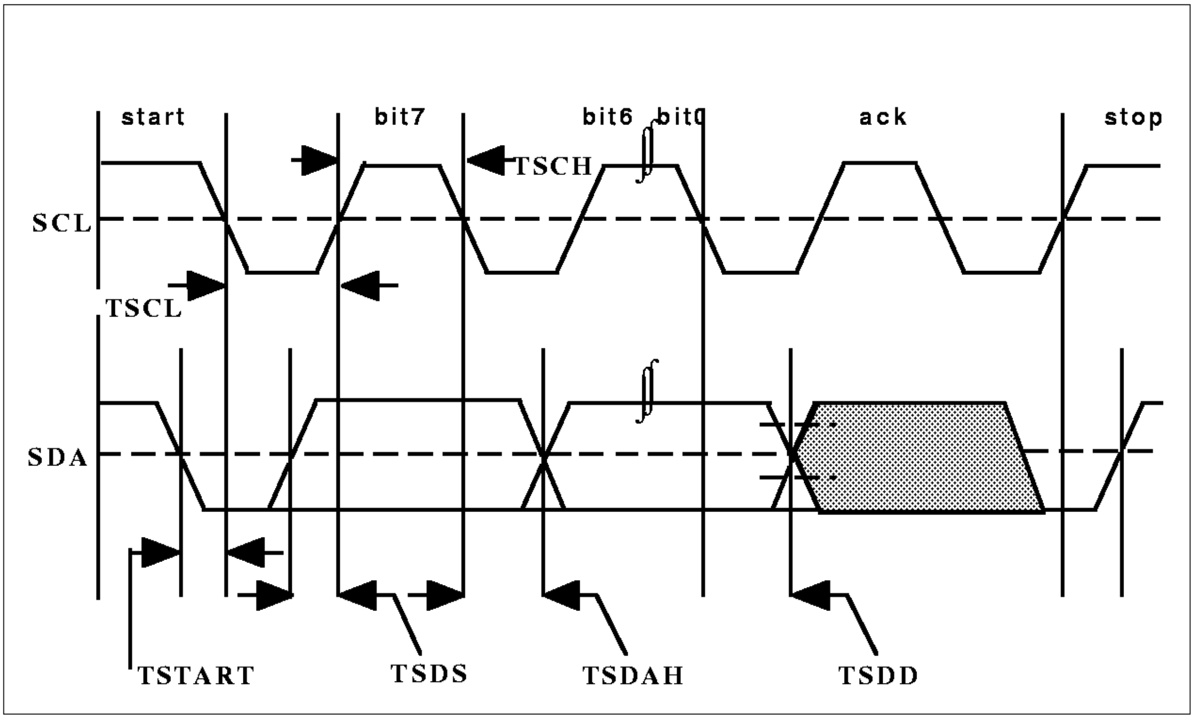


Figure 21 I²C Interface

Table 18 I^2C Interface Timing

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TSTART	CS_BAR (SCL)	60			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Setup time of SDA falling edge(start) with respect to falling edge of SCL.
TSTOP	MICRODATA(0) (SDA)	60			ns		Setup time of SCL rising edge wrt rising edge of SDA(stop).
TSCL	CS_BAR (SCL)	120			ns		Low time of SCL clock pulse.
TSCH	CS_BAR (SCL)	120			ns		High time of SCL clock pulse.
TSDS	MICRODATA(0) (SDA)	60			ns		Setup time of SDA wrt rising edge of SCL.
TSDH	MICRODATA(0) (SDA)	30			ns		Hold time of SDA wrt falling edge of SCL.
TSDD	MICRODATA(0) (SDA)	80			ns	SL=0.5V (0-1 Transition) SL+0.5Vdd (1-0 Transition) Rpullup=1K CLoad=100pf	Delay from falling edge of SCL to SDA valid when HD49430F is driving SDA (eg acknowledge on write).

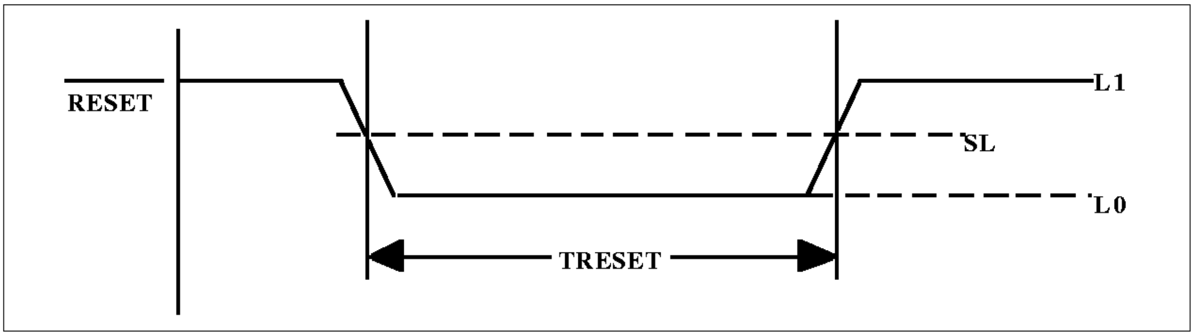


Figure 22 Reset

Table 19 Reset

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TRESET	RESET_BAR	TC4XIP	*10		ns	SL=0.5Vdd L1=0.7Vdd L0= 0.3Vdd	Low time of RESET_BAR signal

System Implementation

TBD