SiI3531

PCI Express to Serial ATA Controller

Data Sheet

Document # SiI-DS-0162-B

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Revision History

Revision	Comment	Date
A	Derived from preliminary specification rev 0.8	06/23/06
B	Updated Company Logo	08/16/06

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1 Overview

The Silicon Image SiI3531 is a PCI Express to single port Serial ATA controller. The SiI3531 is designed to provide serial ATA connectivity with minimal host overhead and host to device latency. The SiI3531 supports a 1-lane 2.5 Gb/s PCI Express bus and the Serial ATA Generation 2 transfer rate of 3.0 Gb/s (300 MB/s).

1.1 Features

1.1.1 Overall Features

- Host Protocol
  - Optimized for transaction oriented designs – minimal Host overhead
  - Supports two command issuance mechanisms
    - Efficient in both embedded and PC implementations
    - Reduces dependency on bridge behavior
- Support for Device Mode Operation
- Fabricated in a 0.18µ CMOS process with a 1.8 volt core and 3.3 volt I/Os
- Available in a 48-pin QFN package (7x7 mm, 0.4 mm lead pitch). **EPAD must be soldered to PCB GND.**

1.1.2 PCI Express Features

- Supports 1-lane 2.5 Gb/s PCI Express
- All registers appear in unified memory space
- All registers accessible through I/O space
- Full-chip command completion status accessible with single PCI Express access

1.1.3 Serial ATA Features

- Integrated Serial ATA Link and PHY logic
- Compliant with Serial ATA 1.0 specifications
- Supports Serial ATA Generation 2 transfer rate of 3.0 Gb/s
  - Output Swing Control
- Supports Native Queuing
- Supports First Party DMA
- Supports Port Multipliers
- 31 Commands and Scatter/Gather Tables on-chip
- Protocol Override per Command

1.2 References

- Serial ATA / High Speed AT Attachment specification, Revision 1.0a
- Serial ATA II: Extensions to Serial ATA 1.0a, Revision 1.2
- Serial ATA II: Port Multiplier, Revision 1.1 and Revision 1.2
- Serial ATA II: Electrical Specification, Revision 1.0
- Serial ATA II: Cables and Connectors, Volumes 1 and 2
- PCI Express Base Specification Revision 1.0a
- PCI Express Card Electromechanical Specification Revision 1.1

2 Electrical Characteristics

2.1 Device Electrical Characteristics

Specifications are for Commercial Temperature range, 0°C to +70°C, unless otherwise specified.

Symbol	Parameter	Ratings	Unit
VDDO	I/O Supply Voltage	4.0	V
VDDD	Core Supply Voltage	2.15	V
VDDSRX VDDSTX VDDSPLL VDDPRX VDDPTX VDDPPLL VDDX	Supply Voltage for S-ATA Receivers, Transmitters, PLLs Oscillator, respectively	2.15	V
V_{IN}	Input Voltage	-0.3 ~ VDD+0.3	V
I_{OUT}	DC Output Current	16	mA
θ_{JA}	Thermal Resistance, Junction to Ambient, Still Air	29.9[1]	°C/W
T_{STG}	Storage Temperature	-65 ~ 150	°C

Note1: **EPAD must be soldered to PCB GND**

Table 2-1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Type	Limits			Unit
				Min	Typ	Max	
VDDD	Core Supply Voltage	-	-	1.71	1.8	1.89	V
VDDSRX	S-ATA Receiver Supply Voltage	-	-				
VDDSTX	S-ATA Transmitter Supply Voltage	-	-				
VDDSPLL	S-ATA SerDes PLL Supply Voltage	-	-				
VDDPRX	PCI Exp Receiver Supply Voltage	-	-				
VDDPTX	PCI Exp Transmitter Supply Voltage	-	-				
VDDPPLL	PCI Exp SerDes PLL Supply Voltage	-	-				
VDDX	Oscillator Power	-	-				
VDDO	Supply Voltage(I/O)	-	-	3.0	3.3	3.6	V
$IDD_{1.8V}$	Supply Current (1.8V Supply)	3GHz Operating	-	-	290*	330*	mA
V_{IH}	Input High Voltage	-	-	2.0	-	-	V
V_{IL}	Input Low Voltage	-	-	-	-	0.8	V
V+	Input High Voltage	-	Schmitt	2.0	-	-	V
V-	Input Low Voltage	-	Schmitt	-	-	0.8	V
V_H	Hysteresis Voltage	-	Schmitt	0.4	-	-	V
I_{IH}	Input High Current	V_{IN} = VDD	-	-10	-	10	µA
I_{IL}	Input Low Current	V_{IN} = VSS	-	-10	-	10	µA
V_{OH}	Output High Voltage	-	-	2.4	-	-	V
V_{OL}	Output Low Voltage	-	-	-	-	0.4	V
I_{OZ}	3-State Leakage Current	-	-	-10	-	10	µA

*3.3V power consumption depends on LED status. If all LEDs are disabled, 3.3V power consumption will be uA.

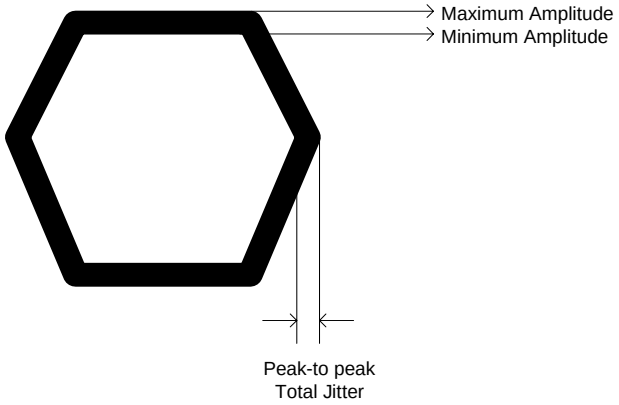
Table 2-2 DC Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{DOUT}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 1100	400	500	700	mV
V_{DIN}	RX+/RX- differential peak-to-peak input sensitivity		200			mV
V_{SATA_SQ}	RX+/RX- OOB Signal Detection Threshold		50	125	200	mV
V_{SATA_ACCM}	Tx AC common-mode voltage				50	mV
Z_{SATA_DIN}	Tx Pair Differential impedance		85	100	115	ohms
Z_{SATA_DOUT}	Rx Pair Differential impedance		85	100	115	ohms
Z_{SATA_SIN}	Tx Single-Ended impedance		40			ohms
Z_{SATA_SOUT}	Rx Single-Ended impedance		40			ohms

Table 2-3 SATA Interface DC Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{PCI_DOUT}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms.	800	1000	1200	mV
$V_{PCI\_DE\text{-}RATIO}$	Tx De-Emphasized Differential Output Voltage	Ratio	- 3.0	-3.5	-4.0	dB
V_{PCI_DIN}	RX+/RX- differential peak-to-peak input sensitivity		175		1200	mV
Z_{PCI_DIN}	Tx Pair Differential impedance	DC impedance	80	100	120	ohms
Z_{PCI_DOUT}	Rx Pair Differential impedance	DC impedance	80	100	120	ohms
Z_{PCI_SIN}	Tx Single-Ended impedance	DC impedance	40	50	60	ohms
Z_{PCI_SOUT}	Rx Single-Ended impedance	DC impedance	40	50	60	ohms
$Z_{PCI\_RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Rx Powered Down Impedance	DC impedance	200k			ohms
$Z_{PCI\_RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Electrical Idle Detect Threshold	Measured at the Rx pins	65		175	mV

Table 2-4 PCI Express Interface DC Specifications



Eye Diagram

2.2 SATA Interface Timing Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
$T_{TX\_RISE\_FALL}$	Rise and Fall time at transmitter	20%-80% at Gen 1 20%-80% at Gen 2	100 67		273 136	ps
$T_{TX\_TOL\_FREQ}$	Tx Frequency Long Term Stability		-350		+350	ppm

Table 2-5 SATA Interface Timing Specifications

2.3 SATA Interface Transmitter Output Jitter Characteristics

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
TJ_{5UI_15G}	Total Jitter, Data-Data 5UI	Measured at Tx output pins peak to peak phase variation Random data pattern		80		ps
DJ_{5UI_15G}	Deterministic Jitter, Data-Data 5UI	Measured at Tx output pins peak to peak phase variation Random data pattern		50		ps
TJ_{250UI_15G}	Total Jitter, Data-Data 250UI	Measured at Tx output pins peak to peak phase variation Random data pattern		85		ps
DJ_{250UI_15G}	Deterministic Jitter, Data-Data 250UI	Measured at Tx output pins peak to peak phase variation Random data pattern		55		ps

Table 2-6 SATA Interface Transmitter Output Jitter Characteristics, 1.5 Gb/s

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
$TJ_{fBAND/10\_3G}$	Total Jitter, $f_{C3dB}=f_{BAUD}/10$	Measured at SATA Compliance Point clock pattern* Load = LL Laboratory Load		70*		ps
$DJ_{fBAND/10\_3G}$	Deterministic Jitter, $f_{C3dB}=f_{BAUD}/10$	Measured at SATA Compliance Point clock pattern* Load = LL Laboratory Load		45*		ps
$TJ_{fBAND/500\_3G}$	Total Jitter, $f_{C3dB}=f_{BAUD}/500$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		80		ps
$DJ_{fBAND/500\_3G}$	Deterministic Jitter, $f_{C3dB}=f_{BAUD}/500$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		55		ps

Table 2-7 SATA Interface Transmitter Output Jitter Characteristics, 3 Gb/s

* With $f_{C3dB}=f_{BAUD}/10$ bandwidth, jitter analysis algorithm provided by oscilloscope manufacture requires full transition density which is clock pattern. A series resistor of 75ohms should be populated close to the VDDX pin

2.4 PCI Express Interface Timing Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
T_{PCI_UI}	Tx / Rx Unit Interval	SSC disabled	399.88	400	400.12	ps
$T_{PCI\_TX\_RISE\_FALL}$	Rise and Fall time at transmitter	20%-80%	0.125			UI
$T_{PCI\_TX-IDLE-MIN}$	Minimum time spent in Electrical Idle		50			UI
$T_{PCI\_TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered set				20	UI
$T_{PCI\_TX-IDLE-TO-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical Idle condition				20	UI
T_{PVPERL}	Power stable to PERST# inactive		100			ms
$T_{PERST-CLK}$	REFCLK stable before PERST# inactive		100			us
T_{PERST}	PERST# active time		100			us

Table 2-8 PCI Express Interface Timing Specifications

2.5 PCI Express Interface Transmitter Output Jitter Characteristics

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
TJ_{PCIe}	Total Jitter	Defined by PCI Express Base Specification Rev 1.1		80		ps

Table 2-9 PCI Express Interface Transmitter Output Jitter Characteristics

2.6 XTALI Requirements

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
T_{XTAL_FREQ}	Nominal Frequency			25		MHz
T_{XTALI_J}	XTALI frequency tolerance	-	-50		+50	ppm

Table 2-10 XTALI Requirements

2.7 Power Supply Noise Requirements

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{NOISE_VDDA}	1.8V Analog Power Noise	peak-to-peak sinewave across 50KHz to 50MHz frequency range. Measured with differential probe trigger by noise source			50	mV
V_{NOISE_VDDD}	1.8V Digital Power Noise				100	mV
V_{NOISE_VDDO}	3.3V IO Power Noise				200	mV

Table 2-11 Power Supply Noise Requirements

3 Pin Definition

3.1 SiI3531 Pin Listing

This section describes the pin-out of the SiI3531 PCI Express to Serial ATA host controller. The table below gives the pin numbers, pin names, pin types, drive types where applicable, internal resistors where applicable, and descriptions. Power pins (VDD and VSS) are excluded from this listing.

Table 3-1 SiI3531 Pin Listing

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
2	XTALO	Analog			Crystal Output
3	XTALI	Analog			Crystal Input
7	SRx+	Diff In			Serial ATA differential receiver + input
8	SRx-	Diff In			Serial ATA differential receiver – input
10	STx-	Diff Out			Serial ATA differential transmitter – output
11	STx+	Diff Out			Serial ATA differential transmitter + output
15	PRx+	Diff In			PCI Express differential receiver + input
16	PRx-	Diff In			PCI Express differential receiver – input
19	PTx-	Diff Out			PCI Express differential transmitter – output
20	PTx+	Diff Out			PCI Express differential transmitter + output
23	REFCLK+	Diff In			PCI Express differential reference clock + input
24	REFCLK-	Diff In			PCI Express differential reference clock - input
25	PERST_N	I-Schmitt			PCI Express Reset
27	LED0	OD	12 mA		Activity LED indicator
30	LED1	OD	12 mA		Connect LED indicator
31	HPL_N	I-Schmitt		70K Pull Up	Hot Plug Switch input
32	LED2	OD	12 mA		Hot Plug Attention LED indicator
33	LED3	OD	12 mA		Hot Plug Power LED indicator
34	NC	-		58K Pull Down	Do Not Connect to any circuitry
35	NC	-		58K Pull Down	Do Not Connect to any circuitry
36	HPLE_N	I		70K Pull Up	Hot Plug Enable
38	NC	-		70K Pull Up	Do Not Connect to any circuitry
39	NC	-		70K Pull Up	Do Not Connect to any circuitry
40	NC	-		70K Pull Up	Do Not Connect to any circuitry
41	NC	-		70K Pull Up	Do Not Connect to any circuitry
43	NC	-		70K Pull Up	Do Not Connect to any circuitry
44	NC	-		70K Pull Up	Do Not Connect to any circuitry
45	NC	-		70K Pull Up	Do Not Connect to any circuitry
47	NC	-		58K Pull Down	Do Not Connect to any circuitry

Table 3-2 Pin Types	
Pin Type	**Pin Description**
I	Input Pin with LVTTL Thresholds
I-Schmitt	Input Pin with Schmitt Trigger
Analog	Analog Input Pin
I/O-Schmitt	Bi-directional Pin with Schmitt Trigger
OD	Open Drain Output Pin

3.2 SiI3531 Pin Diagrams

The diagram below shows the pin layout for the SiI3531 in a 48 QFN package.

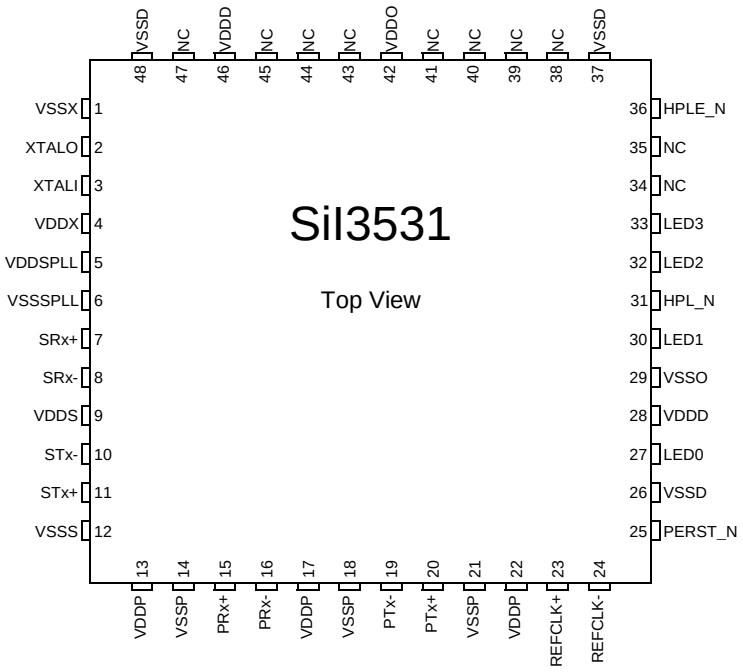


Figure 3-1 Pin Diagram for 48 QFN

3.3 SiI3531 Pin Descriptions

3.3.1 PCI Express Pins

Signal Name	Pin Number(s)	Description
PRx+	15	**Receive +.** Serial receiver differential signal, positive side.
PRx-	16	**Receive -.** Serial receiver differential signal, negative side.
PTx+	20	**Transmit +.** Serial transmitter differential signal, positive side.
PTx-	19	**Transmit -.** Serial transmitter differential signal, negative side.
REFCLK+	23	**Reference Clock +.** PCI Express system supplied differential reference clock, positive side.
REFCLK-	24	**Reference Clock -.** PCI Express system supplied differential reference clock, negative side.
PERST_N	25	**Reset.** PERST_N initializes the PCI Express interface and sets internal registers to their initial state.

3.3.2 LED / Hot Plug pins

Signal Name	Pin Number(s)	Description
LED0	27	**Activity LED.** Activity LED driver for the Serial ATA channel. This is an active low output (LED lit when pin is at 0V).
LED1	30	**Connect LED.** Connect LED driver for the Serial ATA channel. This is an active low output (LED lit when pin is at 0V).
LED2	32	**Hot Plug LED.** ATTENTION LED driver for Hot Plug. This is an active low output (LED lit when pin is at 0V).
LED3	33	**Hot Plug LED.** POWER LED driver for Hot Plug. This is an active low output (LED lit when pin is at 0V).
HPL_N	31	**Hot Plug Switch input.** Input for the Hot Plug Attention switch. This is an active low input (closed switch connects input to 0V).
HPLE_N	36	**Hot Plug enable.** Active low enable for the Hot Plug I/Os.

3.3.3 Serial ATA Signals

Signal Name	Pin Number(s)	Description
SRx+	7	**Receive +.** Serial receiver differential signal, positive side.
SRx-	8	**Receive -.** Serial receiver differential signal, negative side.
STx+	11	**Transmit +.** Serial transmitter differential signal, positive side.
STx-	10	**Transmit -.** Serial transmitter differential signal, negative side.
XTALI	3	**Crystal In.** Crystal oscillator pin for SerDes reference clock. The clock precision recommendation is ±50ppm.
XTALO	2	**Crystal Out.** Crystal oscillator pin for SerDes reference clock. A 25MHz crystal must be used.

3.3.4 NC Pins

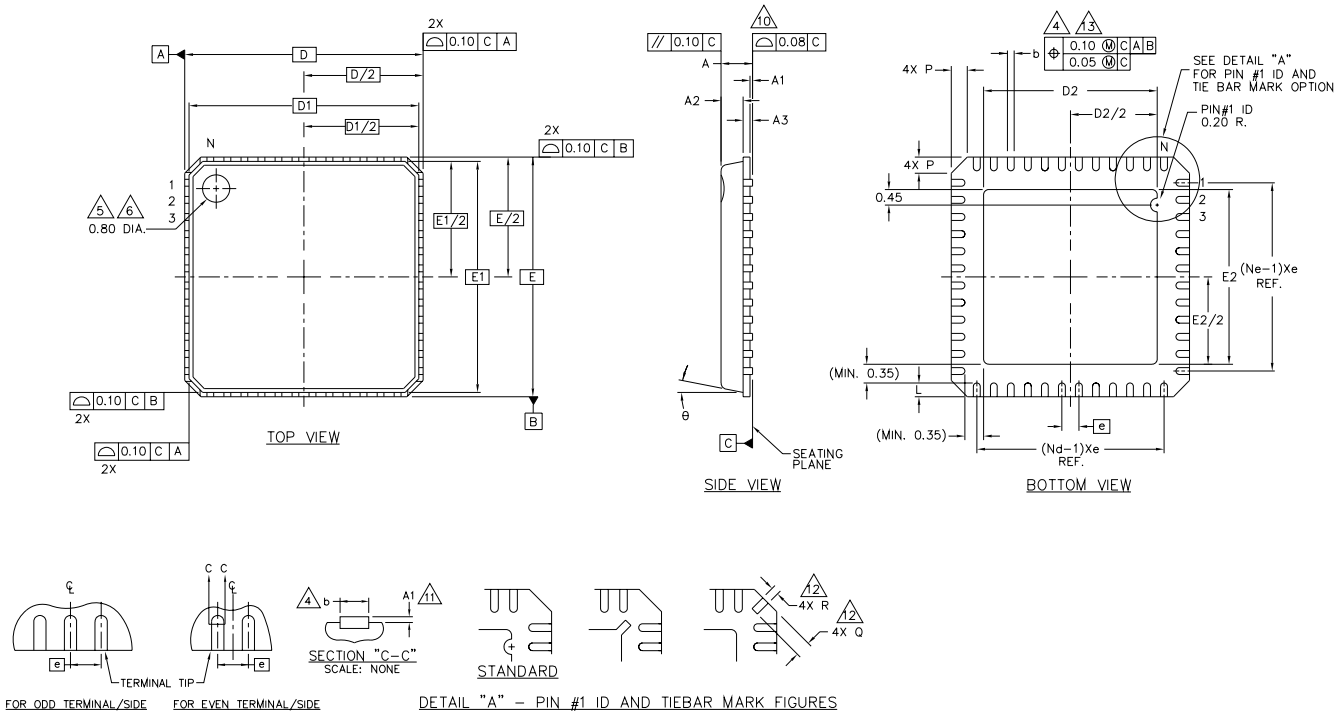
Signal Name	Pin Number(s)	Description
NC	34,35,38,39,40,41 43,44,45,47	**Do not connect.** Must leave open for normal operation

3.3.5 Power/Ground Pins

All like-named power/ground pins, in the table below, are connected together within the package.

Pin Name	Pin Number(s)	Description
VDDS	9	**SATA Power.** This pin provides 1.8V for the Serial ATA receivers and transmitters.
VSSS	12	**SATA Ground.** This pin provides the Ground reference for the Serial ATA receivers and transmitters.
VDDSPLL	5	**SATA PLL Power.** This pin provides 1.8V for the PLL of the Serial ATA PHY.
VSSSPLL	6	**SATA PLL Ground.** This pin provides the Ground reference for the PLL of the Serial ATA PHY.
VDDP	13, 17, 22	**PCI-E Power.** These pins provide 1.8V for the PCI Express receivers and transmitters.
VSSP	14, 18, 21	**PCI-E Ground.** These pins provide the Ground reference for the PCI Express SerDes.
VDDX	4	**Oscillator Power.** This pin provides 1.8V for the crystal oscillator (associated with XTALI and XTALO pins). To minimize this noise coupling to an integrated PLL, a series resistor of 75ohms should be populated close to the VDDX pin
VSSX	1	**Oscillator Ground.** This pin provides the Ground reference for the crystal oscillator (associated with XTALI and XTALO pins).
VDDO	42	**I/O Power.** This pin provides 3.3V for the digital I/O.
VSSO	29	**I/O Ground.** This pin provides the Ground reference for the digital I/O.
VDDD	28, 46	**Digital Power.** These pins provide 1.8V for the digital logic.
VSSD	26, 37, 48	**Digital Ground.** These pins provide the Ground reference for the digital portion of the chip.

4 Package Drawing



***EPAD must be soldered to PCB GND.**

Figure 4-1 Package Drawing 48 QFN

Symbol	Dimensions (mm)		
	Minimum	Nominal	Maximum
e		0.50	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
D2	5.31	5.46	5.61
E2	5.31	5.46	5.61
A	-	0.85	1.00
A1	0.00	0.02	0.05
A2	-	0.65	0.80
A3	0.20 REF		
D	7.00 BSC		
D1	6.75 BSC		
E	7.00 BSC		
E1	6.75 BSC		
θ			14°
P	0.24	0.42	0.60

Table 4-1 Package Dimensions

Part Ordering Number:
SiI3531CNU (48 pin QFN lead free package)

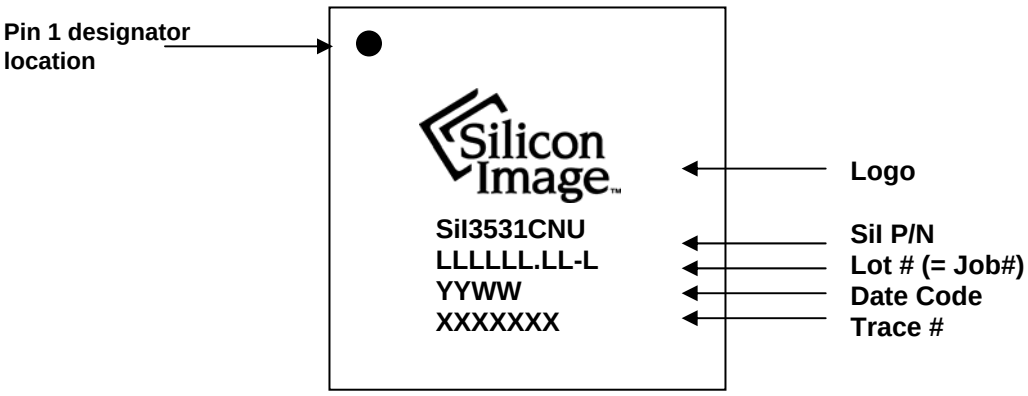


Figure 4-2 Marking Specification – SiI3531CNU

5 Block Diagram

5.1 Sil3531 Block Diagram

The Sil3531 contains the major logic modules shown below.

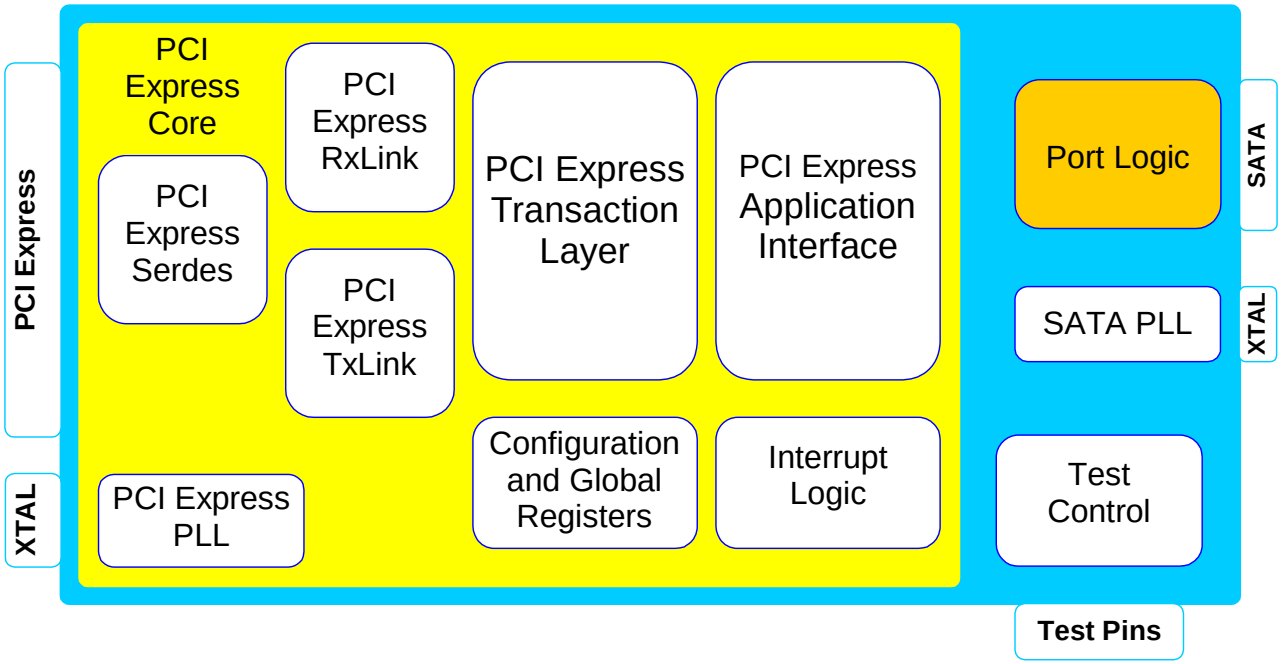


Figure 5-1 Sil3531 Block Diagram

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