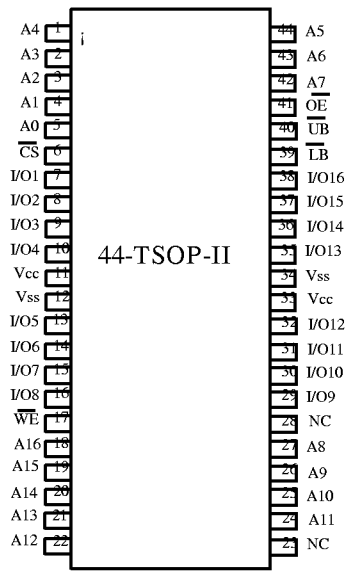
Description

The GM76FV216/ GM76FU216/ GM76FS216/ GM76FR216 is a 2,097,152 bits static random access memory organized as 131,072 words by 16 bits. It uses an advanced Full CMOS process technology and high speed and low power circuit technology. Thus it is suitable for high speed and low power applications, especially where battery back-up is required.

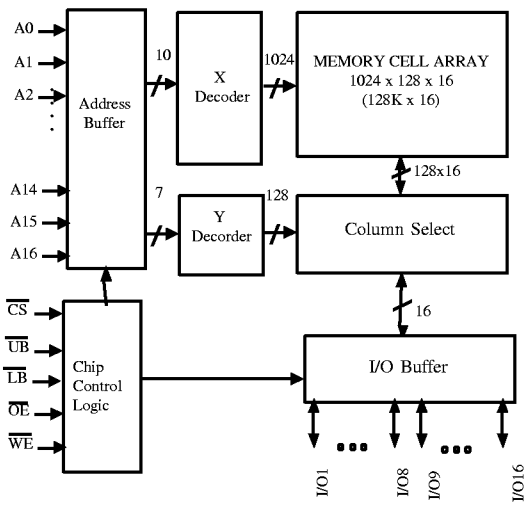
Features

- Fast Speed : 55/70ns
- Power Supply /Speed
  GM76FV216: 3.3V±0.3V / *55/70ns
  GM76FU216 : 3.0V±0.3V / *55/70ns
  GM76FS216 : 2.5V±0.2V / *70/85ns
  GM76FR216 : 2.0V±0.2V / *100/120ns
  * The parameter is measured with 30pF test load.
- Low Power Standby
  10uA(LL) / 2uA(SL)
- Completely Static RAM : No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- TTL compatible inputs and outputs
- Capability of Battery Back-up Operation
- Standard 44 TSOP-II
- Temperature Range
  Commercial(0 70°C)
  Industrial (-40 ~ 85°C)

Pin Configuration



Block Diagram



Pin Description

Pin	Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1-I/O16	Data Inputs/Outputs
$\overline{LB}$	Lower Byte (I/O1~ I/O8)
$\overline{UB}$	Upper Byte (I/O9~ I/O16)
Vcc	Power Supply (1.8V ~3.6V)
Vss	Ground
NC	No Connection

Absolute Maximum Ratings*

Symbol	Parameter		Rating	Unit
T_A	Ambient Temperature under Bias	GM76FV216 GM76FU216 GM76FS216 GM76FR216	0 ~ 70	°C
		GM76FV216-I GM76FU216-I GM76FS216-I GM76FR216-I	-40 ~ 85	
T_{STG}	Storage Temperature		-55 ~ 150	°C
T_{SOL}	Soldering Temperature and Time		260, 10 (at lead)	°C, S
V_{CC}	Supply Voltage		-0.2 ~ 4.0**	V
V_{IN}	Input Voltage		-0.2 ~ 3.6 ***	V
$V_{I/O}$	Input and Output Voltage		-0.2 ~ 3.6 ***	V
P_D	Power Dissipation		1	W

*: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** : Maximum Vcc = -0.2 to 4.6V for GM76FV216 -(I)

*** : $V_{IN}/V_{I/O}$ = -0.2 to 3.9V for GM76FV216 - (I)

Recommended DC Operating Conditions*

Symbol	Parameter	Product	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	GM76FV216 -(I) GM76FU216 -(I) GM76FS216 -(I) GM76FR216-(I)	3.0 2.7 2.3 1.8	3.3 3.0 2.5 2.0	3.6 3.3 2.7 2.2	V
V_{IH}	Input High Voltage	GM76FV216 -(I) GM76FU216 -(I) GM76FS216 -(I) GM76FR216 -(I)	2.2 2.2 2.0 1.6	-	Vcc+ 0.2	V
V_{IL}	Input Low Voltage	All Product	-0.2**	-	0.4	V

* 1) Commercial Product : Ta = 0 ~ 70 °C, unless otherwise specified
2) Industrial Product : Ta = -40 ~ 85 °C, unless otherwise specified

** V_{IL}(min) = -1.5V for ≤ 30ns pulse

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 ~ I/O8	I/O9 ~ I/O16	Vcc Current
H	X	X	X	X	Not Selected	Not Selected	Iccs1, Iccs2
L	L	H	L	L	Read	Read	Icc, Icc1, Icc2
			L	H	Read	High - Z	Icc, Icc1, Icc2
			H	L	High - Z	Read	Icc, Icc1, Icc2
L	X	L	L	L	Write	Write	Icc, Icc1, Icc2
			L	H	Write	Not Write/High - Z	Icc, Icc1, Icc2
			H	L	Not Write/High - Z	Write	Icc, Icc1, Icc2
L	H	H	X	X	High - Z	High - Z	Icc, Icc1, Icc2
L	X	X	H	H	High - Z	High - Z	Icc, Icc1, Icc2

*Note: X means don't care(Must be high or low states)

Capacitance (f = 1MHz, T_A = 25 °C)

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_I = 0V	-	8	pF
$C_{I/O}$	Output Capacitance	V_O = 0V	-	10	pF

*Note: This parameter is sampled and not 100% tested.

AC Operating Characteristics

Test Conditions (Commercial Product :Ta = 0 ~ 70 °C, Industrial Product : Ta = -40 ~ 85 °C)

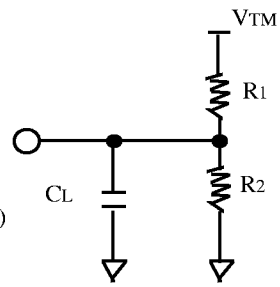
Parameter	Value
Input Pulse Level	0.4 to 2.2V for Vcc=3.3V,3.0V,2.5V 0.4 to 1.8V for Vcc=2.0V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V for Vcc=3.3V,3.0V 1.1V for Vcc=2.5V 0.9V for Vcc=2.0V
Output Load	C_L = 100pF + 1TTL Load or 30 pF + 1TTL Load

DC Operating Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{I(L)}$	Input Leakage Current	V_{IN} = Vss to V_{CC}		-1	-	1	uA
$I_{O(L)}$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{UB}$=V_{IH} or $\overline{LB}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$ = V_{IH}, $V_{SS} < V_{OUT} < V_{CC}$		-1	-	1	uA
V_{OH}	High Level Output Voltage	I_{OH}	-1.0mA at Vcc=3.3V -1.0mA at Vcc=3.0V -0.5mA at Vcc=2.5V -0.44mA at Vcc=2.0V	2.4 2.2 2.0 1.6	-	-	V
V_{OL}	Low Level Output Voltage	I_{OL}	2.1mA at Vcc=3.0/3.3V 0.5mA at Vcc=2.5V 0.33mA at Vcc=2.0V	-	-	0.4	V
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} , V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		-	-	10	mA
I_{CC1}	Average Operating Current	$\overline{CS}$ = V_{IL} V_{IN} = V_{IH} or V_{IL} , I_{OUT} = 0mA tcycle = Min, cycle	Vcc=3.3V@55ns	-	-	60	mA
			Vcc=3.0V@55ns	-	-	50	
			Vcc=2.5V@70ns	-	-	30	
			Vcc=2.0V@100ns	-	-	25	
I_{CC2}		$\overline{CS1}$ = 0.2V, V_{IN} = V_{CC} - 0.2V or 0.2V I_{OUT} = 0mA, tcycle = 1μs		-	-	10	mA
I_{CCS1}	Standby Current(TTL)	$\overline{CS}$ = V_{IH}		-	-	0.3	mA
I_{CCS2}	Standby Current(CMOS)	$\overline{CS}$ ≥ V_{CC}-0.2V	SL	-	-	2	uA
			LL	-	-	10	

AC Test Load Conditions.

1. Including scope and jig capacitance
2. R1=3070 Ω , R2=3150 Ω
3. V_{TM}=2.8V for Vcc=3.0V/3.3V
   V_{TM}=2.3V for Vcc=2.5V
   V_{TM}=1.8V for Vcc=2.0V
4. C_L= 100pF + 1TTL (70ns @3.3/3.0V, 85ns @2.5V,120ns @2.0V)
   30pF + 1TTL (55ns @3.3/3.0V, 70ns @2.5V, 100ns @2.0V)
   5pF + 1TTL (For tCLZ1,tCLZ2,tOLZ,tCHZ1
   tCHZ2,tOHZ,tWHZ,tOW)



AC Operating Characteristics

Read Cycle

(Commercial Product :Ta = 0 ~ 70 °C, Industrial Product : Ta = -40 ~ 85 °C)

Symbol	Parameter	55ns		70ns		85ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	55	-	70	-	85	-	ns
t_{AA}	Address access time	-	55	-	70	-	85	ns
t_{CO}	Chip select access time ($\overline{CS}$)	-	55	-	70	-	85	ns
t_{BA}	Byte enable access time ($\overline{UB}$, $\overline{LB}$)	-	30	-	35	-	45	ns
t_{OE}	Output enable access time ($\overline{OE}$)	-	30	-	35	-	45	ns
t_{CLZ}	Chip select to low - Z output ($\overline{CS}$)	5	-	5	-	10	-	ns
t_{OLZ}	Output enable to low - Z output ($\overline{OE}$)	5	-	5	-	5	-	ns
t_{BLZ}	Byte eanble to low - Z output ($\overline{UB}$, $\overline{LB}$)	5	-	5	-	5	-	ns
t_{CHZ}	Chip select to high - Z output ($\overline{CS}$)	0	20	0	25	0	30	ns
t_{OHZ}	Output enable to high -Z output ($\overline{OE}$)	0	20	0	25	0	30	ns
t_{BHZ}	Byte enable to high - Z output ($\overline{UB}$, $\overline{LB}$)	0	20	0	25	0	30	ns
t_{OH}	Output hold time	5	-	10	-	10	-	ns

Write Cycle

Symbol	Parameter	55ns		70ns		85ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	55	-	70	-	85	-	ns
t_{CW}	Chip select to end of write	50	-	65	-	75	-	ns
t_{BW}	Byte enable to end of write	50	-	60	-	70	-	ns
t_{AW}	Address valid to end of write	50	-	60	-	70	-	ns
t_{AS}	Address setup time	0	-	0	-	0	-	ns
t_{WP}	Write pulse width	45	-	50	-	60	-	ns
t_{WR}	Write recovery time	0	-	0	-	0	-	ns
t_{DW}	Data to write time overlap	25	-	30	-	35	-	ns
t_{DH}	Data hold from write time	0	-	0	-	0	-	ns
t_{WHZ}	Write to output in high - Z	0	20	0	25	0	30	ns
t_{OW}	Output active from end of write	5	-	5	-	5	-	ns

AC Operating Characteristics

Read Cycle

(Commercial Product :Ta = 0 ~ 70 °C, Industrial Product : Ta = -40 ~ 85 °C)

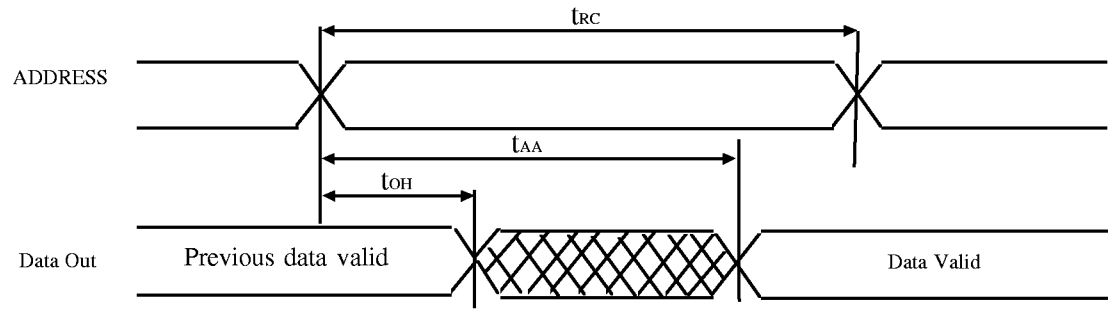
Symbol	Parameter	100ns		120ns		Unit
		Min	Max	Min	Max	
t_{RC}	Read cycle time	100	-	120	-	ns
t_{AA}	Address access time	-	100	-	120	ns
t_{CO}	Chip select access time ($\overline{CS}$)	-	100	-	120	ns
t_{BA}	Byte enable access time ($\overline{UB}$, $\overline{LB}$)	-	50	-	60	ns
t_{OE}	Output enable access time ($\overline{OE}$)	-	50	-	60	ns
t_{CLZ}	Chip select to low - Z output ($\overline{CS}$)	10	-	10	-	ns
t_{OLZ}	Output enable to low - Z output ($\overline{OE}$)	5	-	5	-	ns
t_{BLZ}	Byte eanble to low - Z output ($\overline{UB}$, $\overline{LB}$)	5	-	5	-	ns
t_{CHZ}	Chip select to high - Z output ($\overline{CS}$)	0	35	0	35	ns
t_{OHZ}	Output enable to high -Z output ($\overline{OE}$)	0	35	0	35	ns
t_{BHZ}	Byte enable to high - Z output ($\overline{UB}$, $\overline{LB}$)	0	35	0	35	ns
t_{OH}	Output hold time	15	-	15	-	ns

Write Cycle

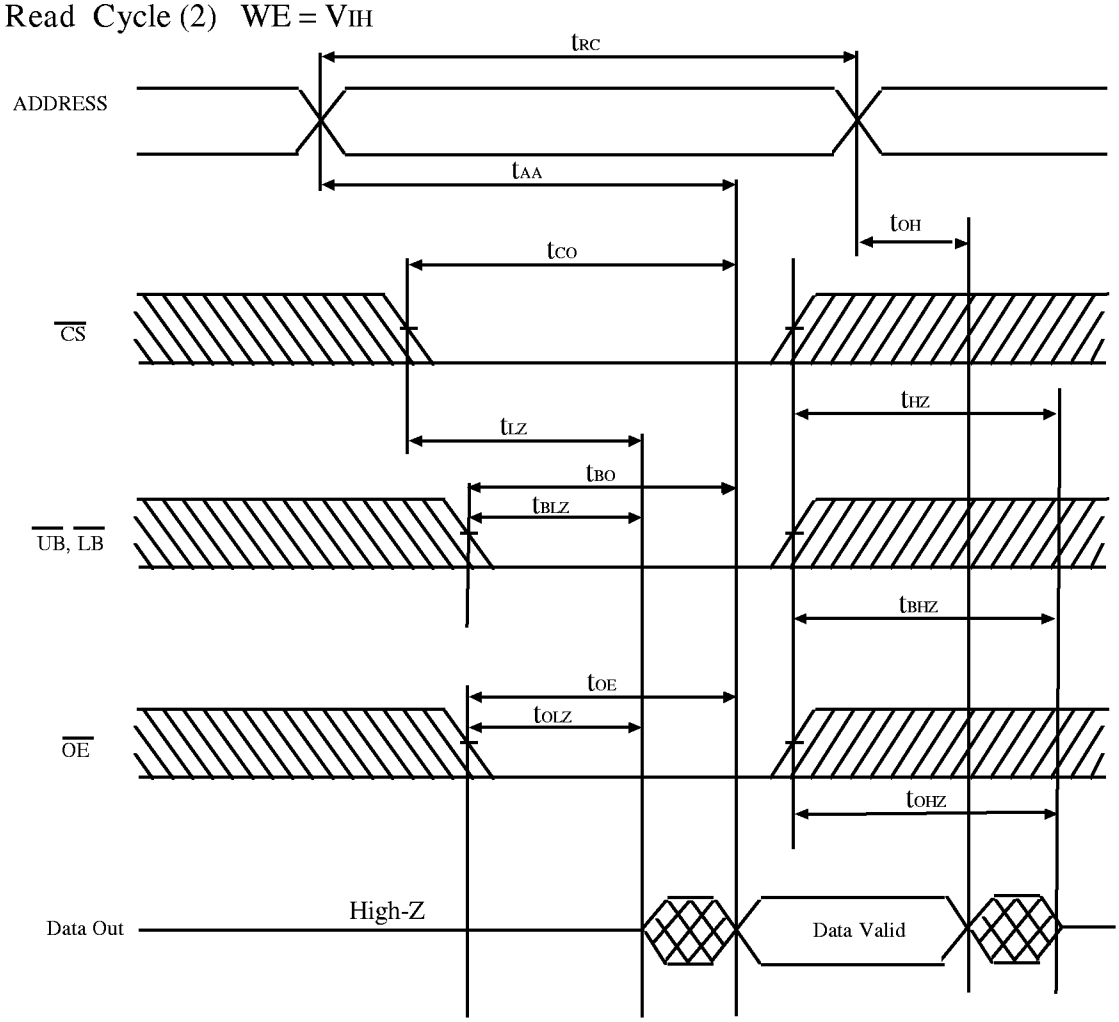
Symbol	Parameter	100ns		120ns		Unit
		Min	Max	Min	Max	
t_{WC}	Write cycle time	100	-	120	-	ns
t_{CW}	Chip select to end of write	80	-	100	-	ns
t_{BW}	Byte enable to end of write	80	-	100	-	ns
t_{AW}	Address valid to end of write	80	-	100	-	ns
t_{AS}	Address setup time	0	-	0	-	ns
t_{WP}	Write pulse width	70	-	80	-	ns
t_{WR}	Write recovery time	0	-	0	-	ns
t_{DW}	Data to write time overlap	40	-	50	-	ns
t_{DH}	Data hold from write time	0	-	0	-	ns
t_{WHZ}	Write to output in high - Z	0	30	0	35	ns
t_{OW}	Output active from end of write	10	-	10	-	ns

Timing Waveforms

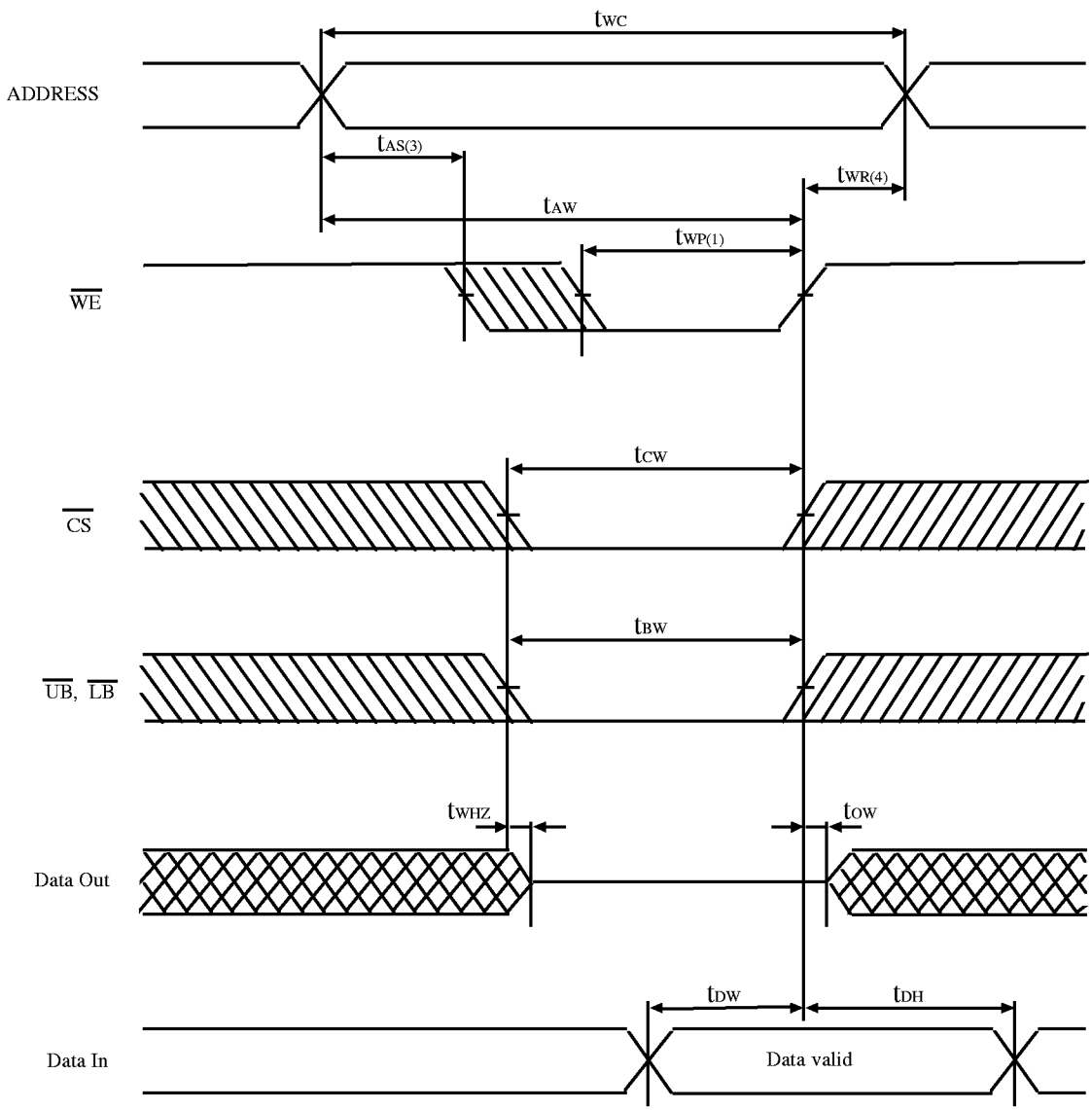
Read Cycle (1) ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, $\overline{UB}$ and, or $\overline{LB}$ = V_{IL})



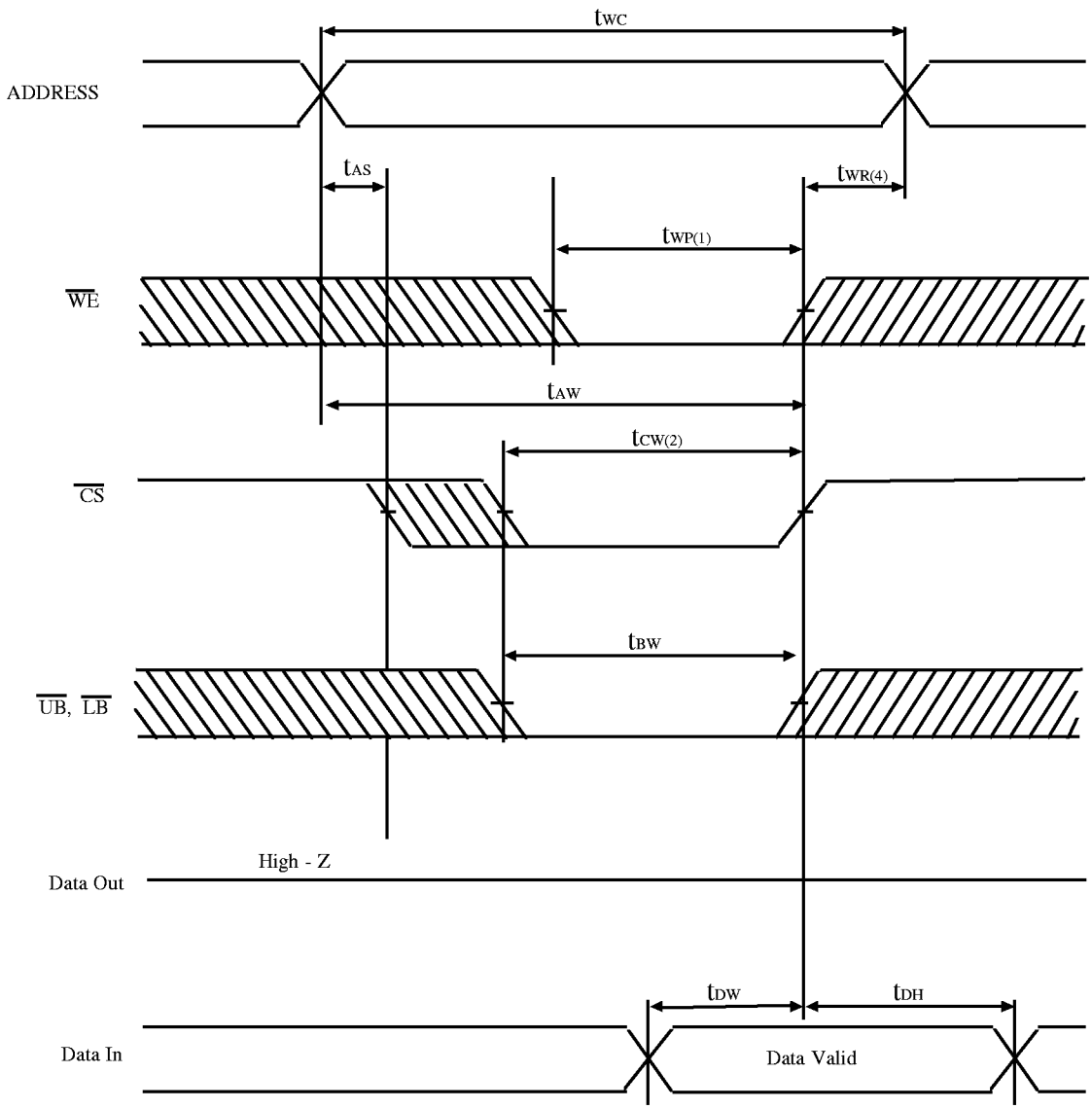
Read Cycle (2) $\overline{WE}$ = V_{IH}



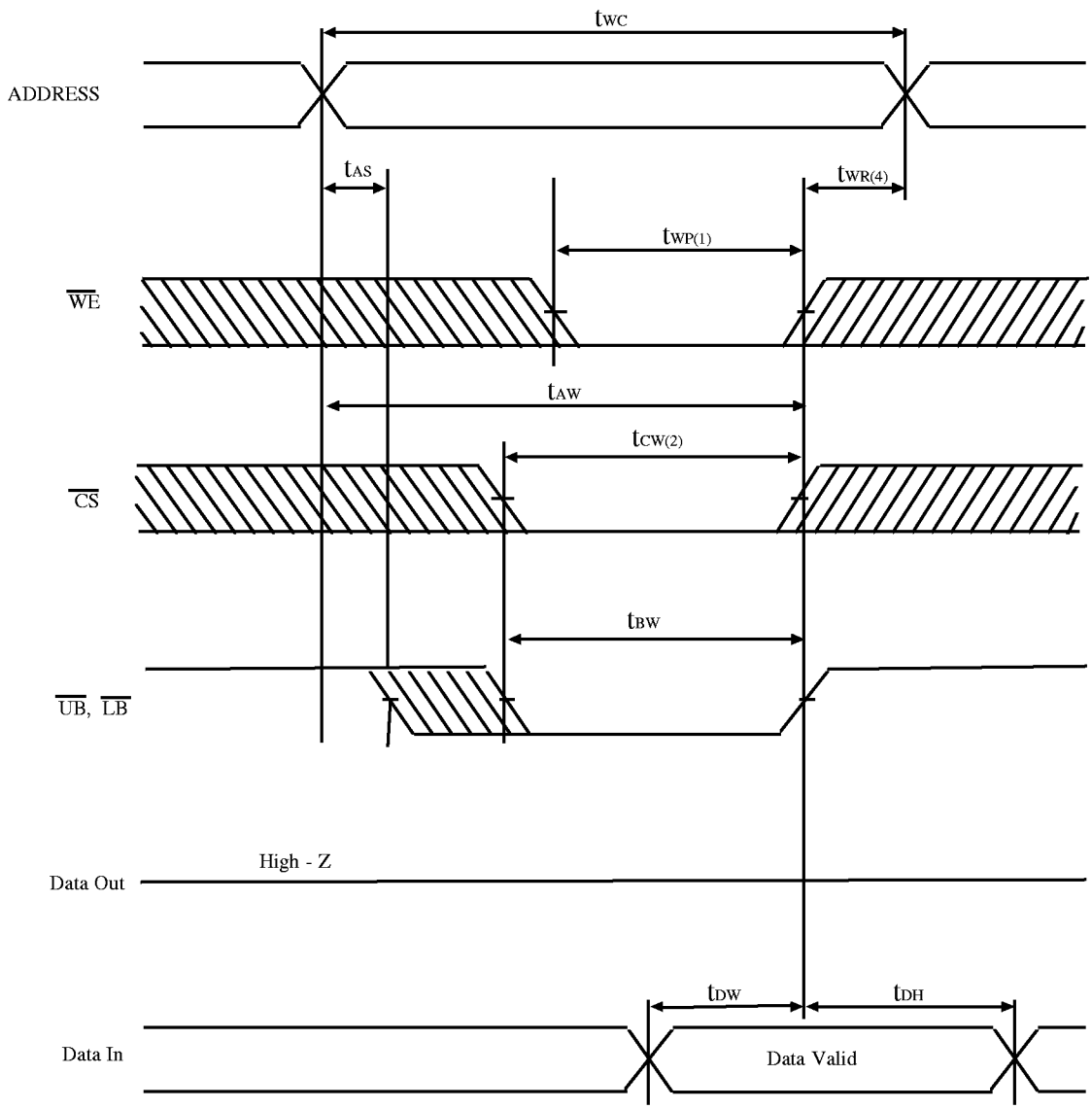
Write Cycle (1) ($\overline{WE}$ Controlled)



Write Cycle (2) ($\overline{CS}$ Controlled)



Write Cycle (3) ($\overline{UB}$, $\overline{LB}$ Controlled)



Notes(Write Cycle):

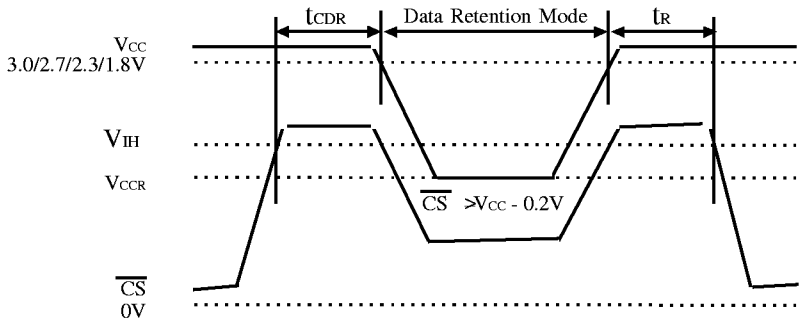
1. A write occurs during the overlap(tWP) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of $\overline{CS}$ going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$, or $\overline{UB}$, or $\overline{LB}$ going high.

Data Retention Characteristics

Symbol	Item	Test Condition		Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage	$\overline{CS}$ ≥Vcc-0.2 V		1.5	-	3.6	V
I_{CCR}	Data Retention Current	Vcc=2.0V, $\overline{CS}$ ≥Vcc-0.2 V	LL SL	- -	- -	10 2	*u*A
t_{CDR}	Chip Select to Data Retentiom Time	See data retention waveform		0	-	-	ns
t_R	Operation Recovery Time			t_{RC} [1)]	-	-	ns

1) tRC = Read cycle time

• Data Retention Waveform



Package Dimensions

Unit: Inches (mm)

44 TSOP-II