SMART MOSFET DRIVER

FEATURES

- **20 ns Rise and Fall into 1000 pF**
- **800 µA Stand-by Current Consumption**
- **Under Voltage Lockout Combined with First Pulse Wake-Up Feature***
- **Cycle by Cycle Current Limiting**
- **Virtually Eliminated Current Sense Voltage Spike when used with Gate Charge Recovery Circuit****
- **Thermal Overload Protection**
- **TTL/CMOS Compatible Input**
- **5-pin Surface Mount Package with 1 W Maximum Power Dissipation Limit**

APPLICATIONS

- **Driving of Power MOSFETs and IGBTs**
- **Switch Mode Power Supplies**
- **Step Motor Drivers**
- **Solenoid Drivers**

DESCRIPTION

The TK75050 is a novel noninverting buffer to drive high power insulated gate transistors (e.g. MOSFETs and IGBTs). The input is both TTL and V_{CC}- level compatible. The output can source or sink 1 A into 1000 pF equivalent load. The IC features built-in cycle-by-cycle current limiting. Its undervoltage lockout (UVLO) circuit is combined with a first pulse wake-up feature*. The chip has thermal overload protection. Using the IC in the Gate Charge Recovery** application, the switching spike developing across the current sense resistor practically becomes negligible. Due to its low stand-by current and first-pulse wake-up feature, the device can be used in self-biased power supplies. The IC's high-speed cycle-by-cycle current limiting capability eliminates the short circuit runaway problem, characteristic to most current controlled converters. The IC is well suited to provide supplementary overload protection in voltage-mode controlled converters, too. Besides the small footprint 5-pin and the 8-pin fused lead frame surface mount packages, the device is also available in the widely used 8-pin DIP package.

* The First Pulse Wake-Up is a built-in proprietary feature of the IC. When the IC is powered on, and the supply voltage exceeds the upper threshold of the UVLO circuit, the start-up circuit is enabled but the device remains in low quiescent current stand-by state. The IC wakes up from stand-by and begins normal operation when the first drive pulse arrives at the input. The normal operation ceases and the IC returns to stand-by when the supply voltage drops below the lower threshold of the UVLO circuit.

** The Gate Charge Recovery application was developed by TOKO Inc., to virtually eliminate the leading edge spikes generated across the current sense resistor by capacitive feedthrough of the MOSFET's gate drive signal. The application is proprietary but is granted for use wtih the IC.

ORDERING INFORMATION

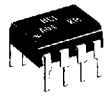
TK75050 □ □ □□

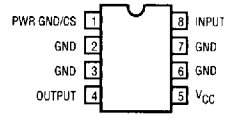
- □□ — Tape/Reel Code
- □ — Temp. Range
- □ — Package Code

PACKAGE CODE	TEMP. RANGE	TAPE/REEL CODE
U : SOT89-5	C : -20 to + 70 °C	BX : Bulk/Bag
D : DIP-8	I : -40 to + 85 °C	TL : Tape Left
M : SOP-8		MG: Magazine

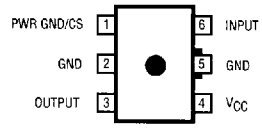
TK75050

DIP-8

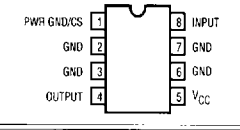




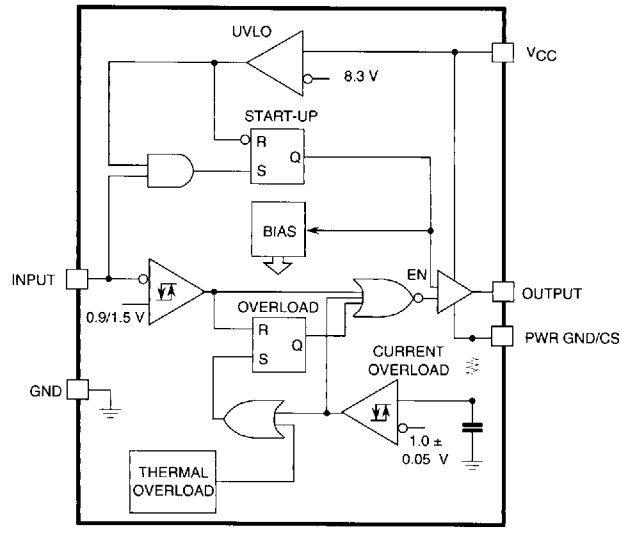
SOT89-5



SOP-8



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Voltage $V_{CC,MAX}$ ..... 18 V
Power Dissipation (Note 1) SOT89-5 ..... 1000 mW
Power Dissipation (Note 2) DIP-8 ..... 825 mW
Power Dissipation (Note 3) SOP-8 ..... 1000 mW
Junction Temperature (T_J) ..... 150 °C

Storage Temperature Range ..... -55 to +150 °C
Lead Soldering Temp. (10 s) ..... 240 °C
Operating Temperature Range (T_A)
C Version ..... -20 to +70 °C
I Version ..... -40 to +85 °C

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = Full operating temperature range, V_{CC} = 15 V, PwrGnd/CS pin is connected to Gnd, DC Test Setup 1 (See Figure 1), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{CC,L}$	Supply Current, Output Low	V_{IN} = 0.4 V after wake up		17	22	mA
$I_{CC,H}$	Supply Current, Output High	V_{IN} = 2.4 V after wake up		14	16	mA
$I_{CC,OFF}$	Supply Current, Stand-by (Note 4)	V_{IN} = 5 V before wake up V_{IN} = 15 V before wake up		250 800	350 1000	µA µA
$I_{PWRGND/CS}$	PwrGnd/CS Current, Output Low	V_{IN} = 0 V after wake up		4.0	6.0	mA
$V_{CC,OFF}$	Supply Voltage, UVLO Threshold	V_{CC} sweeps downwards	7.8	8.3	8.7	V
$V_{IN,L}$	Input Voltage, Low Threshold	$R_S \leq 10\ k\Omega$	0.6	0.9	1.1	V
$V_{IN,H}$	Input Voltage, High Threshold		1.2	1.5	1.8	V
$I_{IN,L}$	Input Current, Low (Note 5)	V_{IN} = 0.4 V, R_S = 100 Ω		-100		µA
$I_{IN,H}$	Input Current, High (Note 5)	V_{IN} = 2.4 V		1		µA
$V_{OUT,L}$	Output Voltage, Low	I_{SINK} = 50 mA I_{SINK} = 1000 mA		0.20 3.0	0.25 3.5	V V
$V_{OUT,H}$	Output Voltage, High	I_{SOURCE} = 50 mA I_{SOURCE} = 1000 mA	13.2 11.5	13.8 12.5		V V
$T_{J,OFF}$	Junction Temperature, Thermal Overload Shut-down Threshold (Note 5)	Temp sweeps upwards		150		°C
$T_{J,ON}$	Junction Temperature, Turn-back to Normal Threshold (Note 5)	Temp sweeps downwards after thermal shut-down		90		°C
V_{CL}	Current Sense Voltage, Current Limit Threshold (See Figure 2)	V_{CS} sweeps upwards. PwrGnd/CS pin is floating	0.75	1.0	1.20	V
$V_{CL,HYST}$	Current Sense Voltage, Current Limit Hysteresis (Note 5)	PwrGnd/CS pin is floating		100		mV
t_{DR}	Delay Time, Rise (See Figure 3)	C_L = 1000 pF		16	35	ns

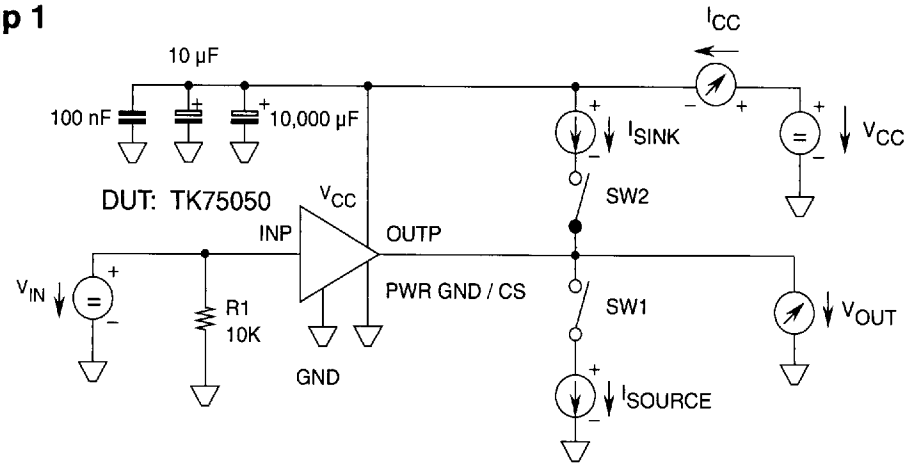
Note 1: For operation above T_A = 25 °C, power dissipation is derated at 8 mW/°C.
Note 2: For operation above T_A = 25 °C, power dissipation is derated at 6.6 mW/°C.
Note 3: For operation above T_A = 25 °C, power dissipation is derated at 8 mW/°C.
Note 4: Before wake-up, at any V_{CC} below $V_{CC,MAX}$ or after wake-up, if V_{CC} drops below $V_{CC,OFF}$.
Condition for wake-up: V_{CC} passes and stays above $V_{CC,OFF}$ when the wake-up pulse arrives.
Note 5: Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: T_A = Full operating temperature range, V_{CC} = 15 V, PwrGnd/CS pin is connected to Gnd, DC Test Setup 1 (See Figure 1), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_R	Rise Time (See Figure 3)	C_L = 1000 pF		20	35	ns
t_{DF}	Delay Time, Fall (See Figure 3)	C_L = 1000 pF		23	40	ns
t_F	Fall Time (See Figure 3)	C_L = 1000 pF		18	30	ns
$t_{D,COS}$	Delay Time, Current Overload Shut-down (See Figure 4) (Note 5)	PwrGnd/CS pin is floating C_L = 1000 pF ΔV_{CS} = 50 mV ΔV_{CS} = 200 mV		 100 60	 150 90	 ns ns
I_{CRC}	Average Cross-Current (Note 5)	f_{IN} = 1 MHz, duty cycle = 50 %		5	7	mA

Figure 1 - DC Test Setup 1



Note: SW1 and SW2 are open by default. To avoid excessive dissipation, they are exclusively closed only for less than 100 ms, while the appropriate output voltages $V_{OUT,H}$ and $V_{OUT,L}$ are measured at specified currents, I_{SOURCE} and I_{SINK}, respectively.

Figure 2 - DC Test Setup 2

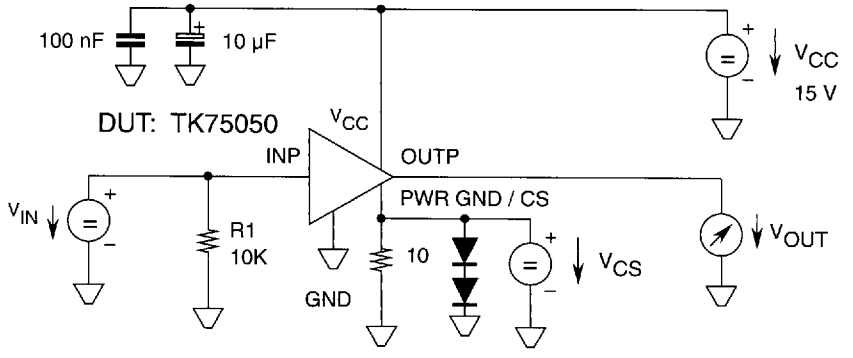


Figure 3 - AC Test Setup 3

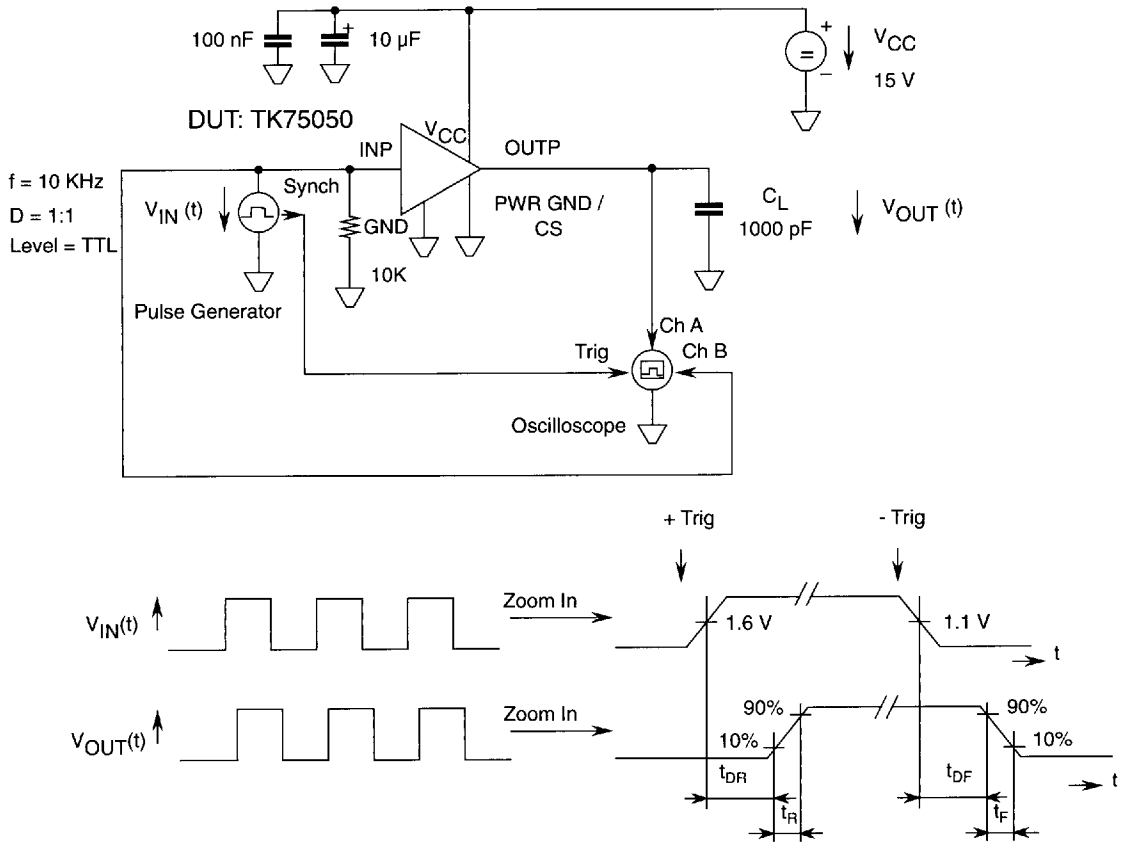
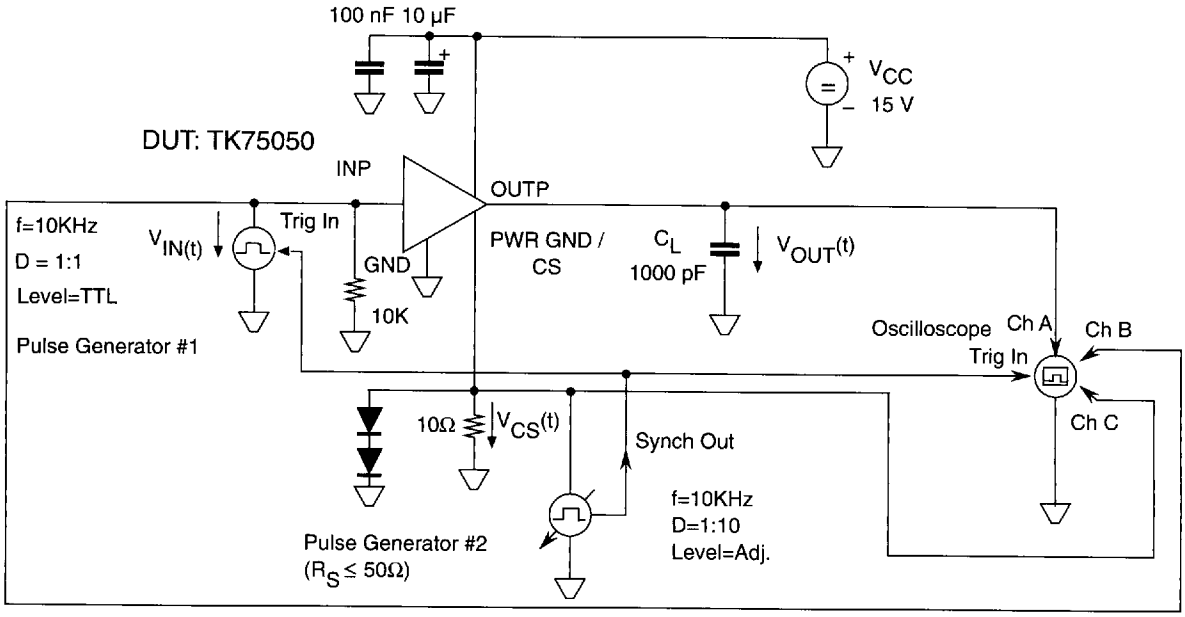


Figure 4 - AC Test Setup 2



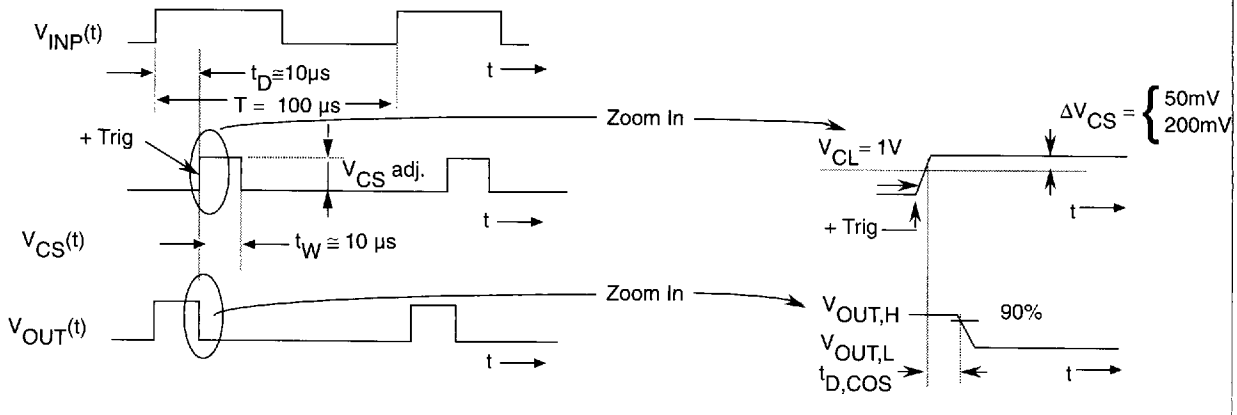
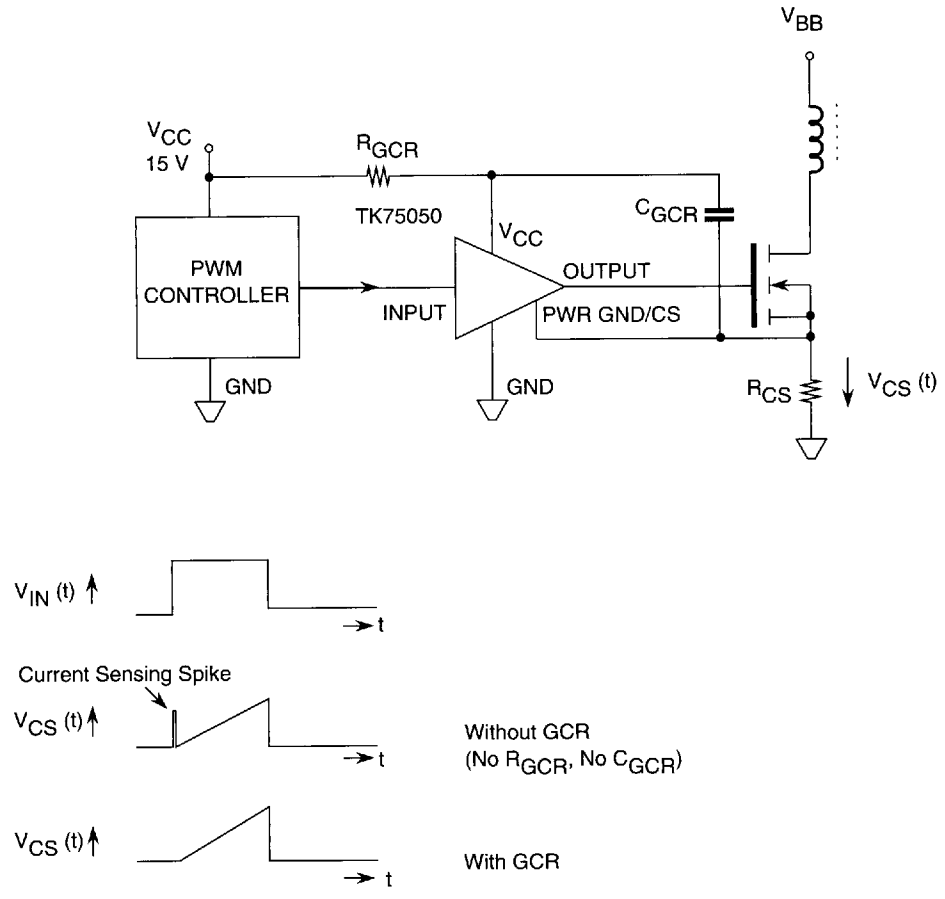
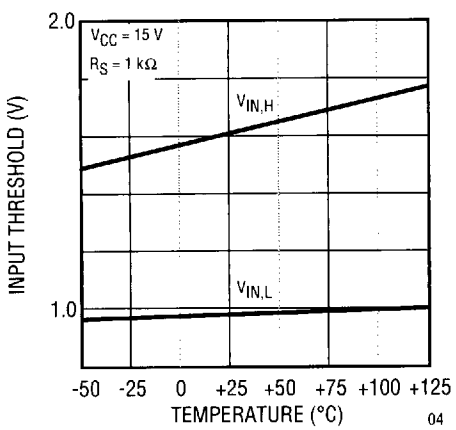


Figure 5 - Self-Biased Power Supply Configuration Combined with Gate Charge Recovery (GCR) Application

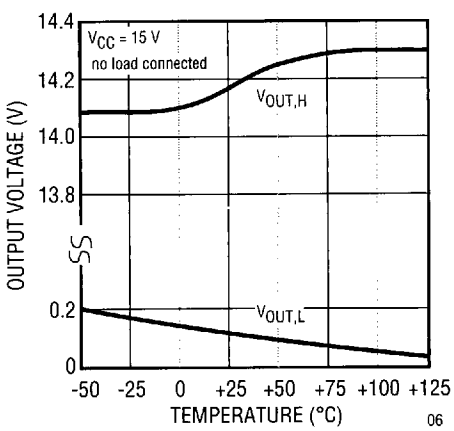


TYPICAL PERFORMANCE CHARACTERISTICS

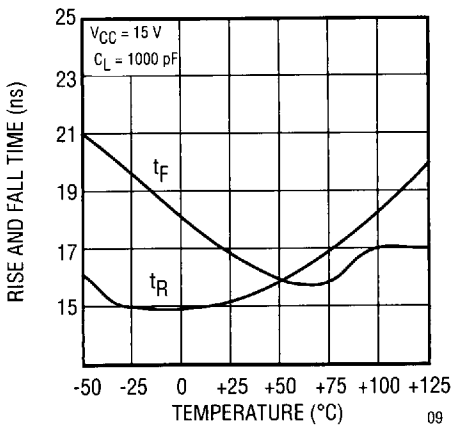
INPUT THRESHOLD vs TEMPERATURE



OUTPUT VOLTAGE vs TEMPERATURE

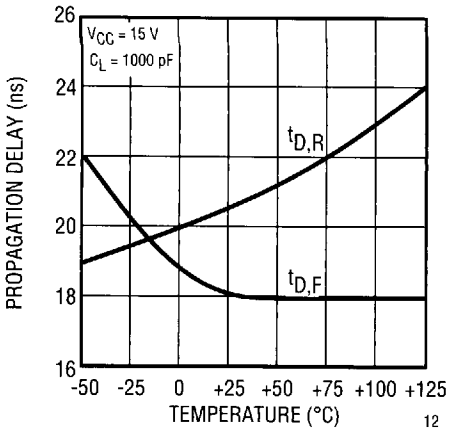


RISE AND FALL TIME vs TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

PROPAGATION DELAY vs TEMPERATURE



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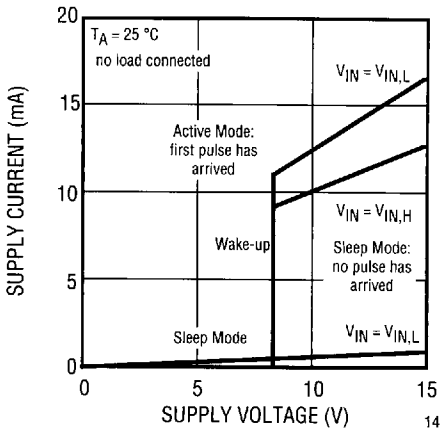
SUPPLY CURRENT vs SUPPLY VOLTAGE



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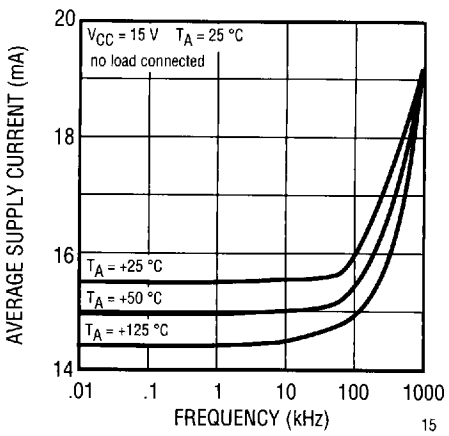
AVERAGE SUPPLY CURRENT vs FREQUENCY



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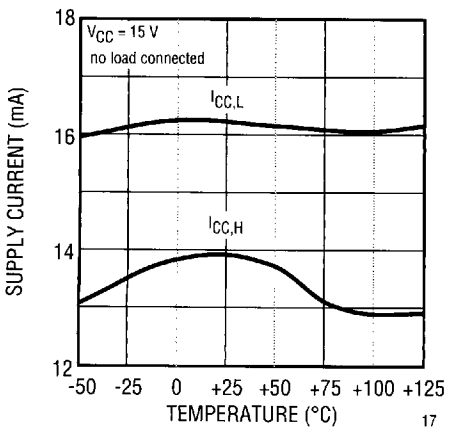
SUPPLY CURRENT vs TEMPERATURE



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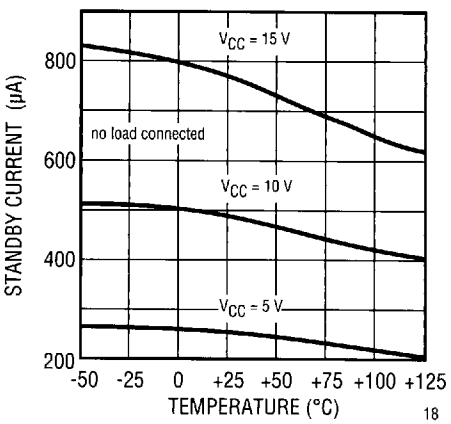
STANDBY CURRENT vs TEMPERATURE



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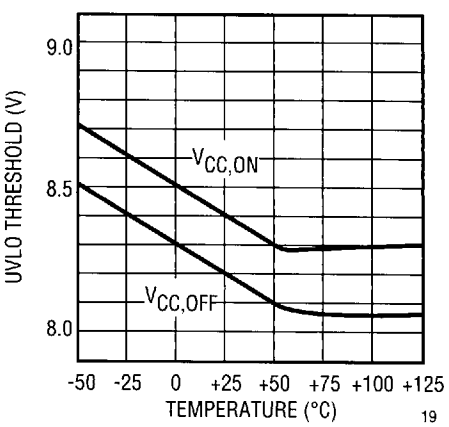
UVLO THRESHOLD vs TEMPERATURE



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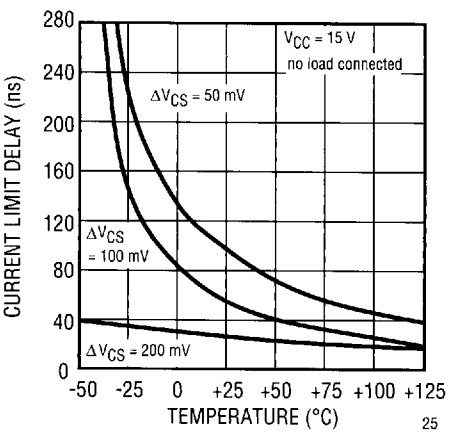
CURRENT LIMIT DELAY vs TEMPERATURE



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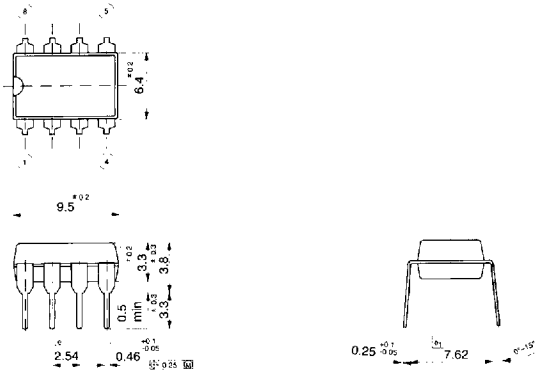
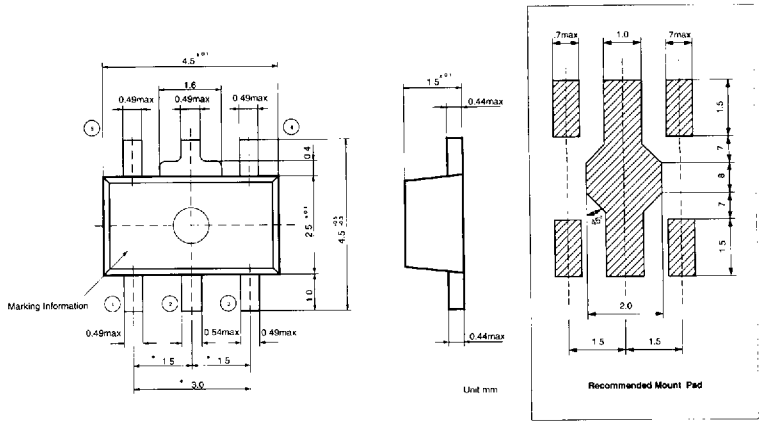
PACKAGE OUTLINES

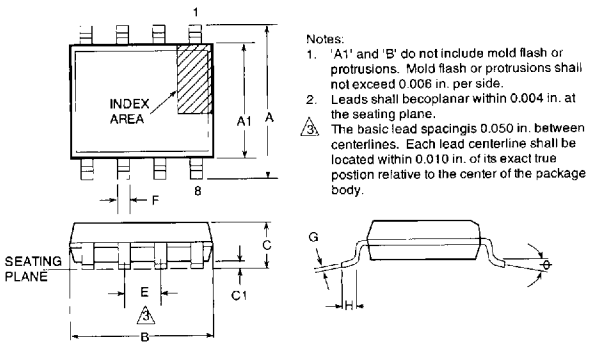
DIP8



SOT89-5



SOP-8



Notes:
1. 'A1' and 'B' do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.006 in. per side.
2. Leads shall becoplanar within 0.004 in. at the seating plane.
3. The basic lead spacingis 0.050 in. between centerlines. Each lead centerline shall be located within 0.010 in. of its exact true postion relative to the center of the package body.

	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050BSC		1.27BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

TOKO

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