HEWLETT PACKARD

MGA-63100
Medium Power
2 Stage GaAs FET Cascade

Features

- **Unmatched 2 Stage FET Cascade**
- **High Output Power:**
  22 dBm typical $P_{1\,dB}$ at 14 GHz
- **High Gain:**
  10.5 dB typical $G_{1\,dB}$ at 14 GHz
- **Single Supply Bias**

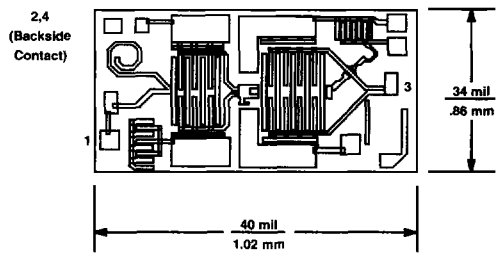
Description

The MGA-63100 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) chip designed for use as a broadband high frequency gain stage in industrial and military applications.

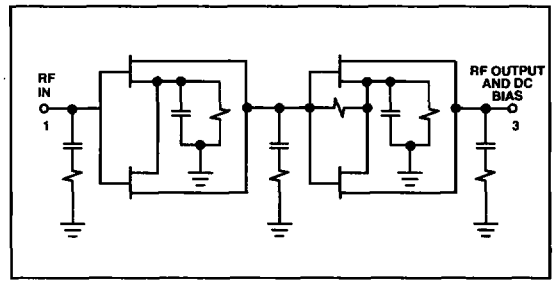
This MMIC uses a cascade of two FET pairs to yield a device with higher gain and higher input impedance than a conventional discrete FET. AC grounded sources and an internal resistive network allow for biasing from a single positive power supply.

The die is fabricated using HP's nominal .3 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

Chip Outline



Chip Schematic



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 10 V, Z_O = 50 Ω		Units	Min.[1]	Typ.	Max.[1]
$P_{1\,dB}$[2]	Power Output @ 1 dB Gain Compression	f = 6.0 GHz f = 14.0 GHz f = 18.0 GHz	dBm	20.0	21.0 22.0 21.0	
$G_{1\,dB}$[2]	1 dB Compressed Gain	f = 6.0 GHz f = 14.0 GHz f = 18.0 GHz	dB	8.0	22.5 10.5 7.5	
P_{SAT}[2]	Saturated Output Power (3 dB Compressed)	f = 14.0 GHz	dB		25.0	
—	Reverse Isolation	f = 14.0 GHz	dB		30.0	
I_d	Device Current		mA	100	150	200

Notes: 1. RF performance is determined by assembling and testing 10 devices per wafer.
2. Tuned Measurement.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	12.0 V
Total Power Dissipation[2]	2.0 W
CW RF Input Power	+25 dBm
Channel Temperature	175°C
Storage Temperature	–65°C to –175°C

Thermal Resistance: θ_{jc} = 33°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 µm spot size[3]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Derate linearly at 30 mW/°C for T_A > 109°C.
3. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

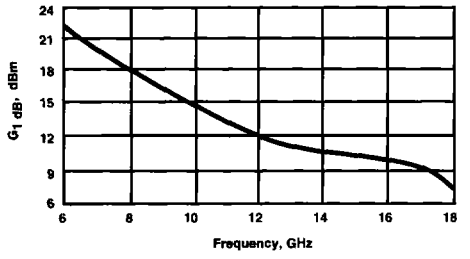
Part Number Ordering Information

Part Number	Devices Per Tray
MGA-63100-GP0	1
MGA-63100-GP2	10
MGA-63100-GP6	Up to 300

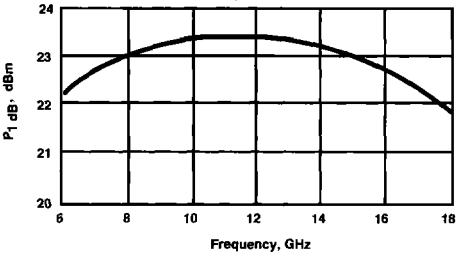
Typical Performance, T_A = 25°C

(unless otherwise noted)

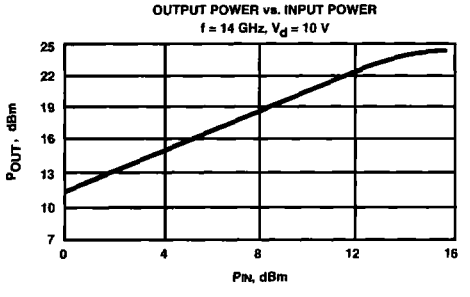
1 dB COMPRESSED GAIN vs. FREQUENCY
V_d = 10 V



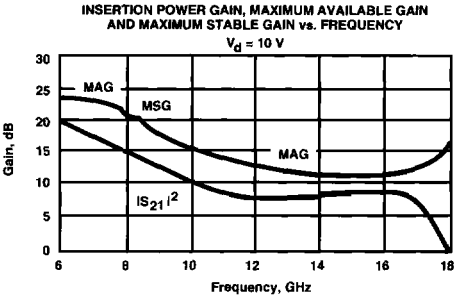
OUTPUT POWER @ 1 dB COMPRESSION
vs. FREQUENCY
V_d = 10 V



OUTPUT POWER vs. INPUT POWER
f = 14 GHz, V_d = 10 V



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN
AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_d = 10 V

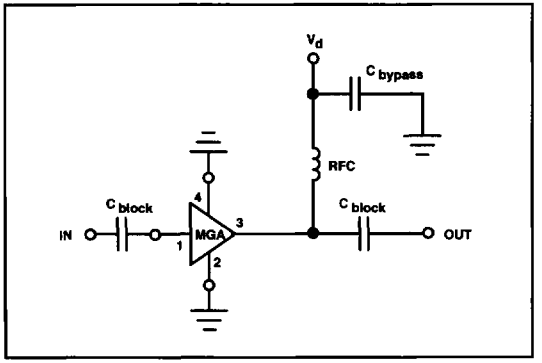


Typical Scattering Parameters: Z_O = 50 Ω

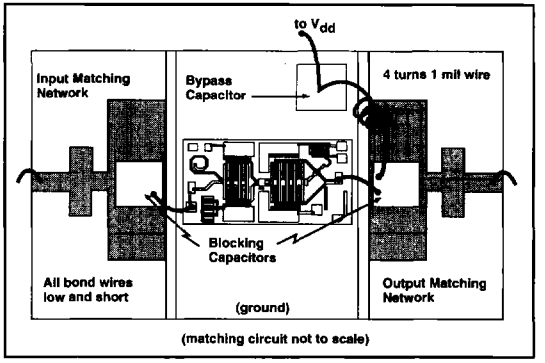
T_A = 25°C, V_d = 10 V

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
4.0	.89	130	8.6	2.14	92	37.7	.013	86	.44	–93	3.03
5.0	.93	106	13.2	4.56	5	95.0	.016	60	.58	–115	1.39
6.0	.63	40	19.9	9.85	–66	–37.1	.014	110	.59	–144	1.81
7.0	.60	–122	19.8	9.77	–155	–29.6	.033	108	.44	–168	1.08
8.0	.82	–178	15.2	5.74	156	–28.4	.038	94	.37	–169	0.92
9.0	.83	155	11.8	3.88	131	–27.5	.042	79	.39	–170	1.12
10.0	.83	138	10.0	3.17	106	–27.3	.043	65	.41	–177	1.31
11.0	.81	124	8.7	2.73	83	–27.3	.043	59	.42	–179	1.59
12.0	.80	109	8.1	2.53	61	–27.7	.041	48	.44	176	1.80
13.0	.74	89	7.8	2.45	36	–28.6	.037	35	.47	168	2.34
14.0	.61	68	7.7	2.42	10	–30.5	.030	18	.50	163	3.56
15.0	.33	48	7.5	2.37	–20	–34.9	.018	11	.56	157	7.34
16.0	.05	134	8.3	2.59	–63	–43.1	.007	13	.65	145	15.87
17.0	.32	–159	6.9	2.21	–106	–37.1	.014	65	.73	128	6.56
18.0	.71	168	–1.6	0.83	–149	–36.5	.015	49	.74	117	8.53

Typical Biasing Configuration



Substrate Bonding Diagram



EXTERNAL ELEMENTS REQUIRED:

- Input and Output DC Blocking Capacitors: 45pF typical
- RF Choke Network and Bypass Capacitor: 4 turns 1 mil wire; 45 pF capacitor typical

INPUT and OUTPUT IMPEDANCE MATCHING NETWORKS:

- This MMIC is not impedance matched. As with a discrete transistor, the S-parameter data provided should be used to design input and output impedance matching networks that will optimize device performance for the designer's application.
  All device guarantees and typical performance information represents performance of the MMIC in a tuned (optimally matched) environment.

RECOMMENDED DIE ATTACH PROCEDURE

1. Die attach should be performed under an inert atmosphere of either nitrogen or forming gas.
2. Set heater block temperature to 300 ± 10°C.
3. Place circuit on heater block and heat thoroughly; typically 5 - 15 seconds.
4. Place Au-Sn preform on circuit in die attach location, using sufficient quantity to ensure wetting and to produce a fillet around the die.
5. Using sharp tweezers, pickup the die and orient it properly on the circuit.
6. Scrub the die into the preform with a back-and-forth motion taking care not to scratch the top surface of the chip. Continue until wetting occurs; normally within 3 to 4 scrubs.
7. Wetting should occur on 100% of the chip perimeter to form a visible fillet around the die.
8. Remove the circuit from the heater block and allow it to cool in air. Total time for die attach should be less than 10 seconds.

RECOMMENDED WEDGE BONDING PROCEDURE

1. Set heater block temperature to 260 ± 10°C (If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact setting will need to be determined empirically, and will vary from machine to machine).
2. Use prestressed (annealed) gold wire of .0007 or .001 inches diameter.
3. Tip bonding pressure should be between 15 and 20 grams, and should not exceed 20 grams. The footprint left by the wire should be between 1.5 and 2.5 wire diameters across.
4. Proceed with bonding according to machine instructions. Bonds should be made from the circuit to the chip bonding pads to minimize the potential for pad damage. Bonds should be made to the source (common) and drain (output) pads of the MMIC before bonding to the gate (input) pad to minimize the potential for ESD damage.

CAUTION: This device makes use of GaAs FET devices with very small gate geometries. Such devices are subject to damage by electro-static discharge (ESD), and must only be handled by properly grounded personnel working at grounded assembly stations.