PERICOM

PI2C3000A

Token Ring Active Retiming Hub Interface Chip

Product Features:

- Complete physical layer interface for 4/16 Mbps Token Ring Concentrator
- Supports single-ended data mode for switch or MAC applications
- Dual PLLs with jitter attenuator for each lobe port and Ring-In/Ring-Out port for UTP/STP concentrator
- Pin selectable 4 Mbps or 16 Mbps data rates
- Receive adaptive equalizer to minimize data dependent correlated jitter and handle cable length variations
- Pin selectable Jitter Attenuator PLL for reduction of accumulated jitter at 16 Mbps
- Constant gain digital PLLs for data retiming
- Phantom voltage detection/generation for lobe port and Ring-In/Ring-Out port insertion
- Automatic speed detection during lobe test
- Speed/Energy detect circuit for valid received signals
- On-chip lobe bypass mechanism replaces relays
- LED drivers for diagnostic status display
- Advanced 0.8 µm BiCMOS technology
- Packages available:
  - 48-pin 240-mil wide plastic TSSOP (A48)
  - 48-pin 300-mil wide plastic SSOP (V48)

Product Description:

The Pericom PI2C3000A Token Ring Active Retiming Hub Interface Chip is designed for IEEE 802.5 compliant Token Ring Active Concentrators. It contains a line driver, speed/energy detect circuit, a receive adaptive equalizer, a phantom voltage detector/generator, a retiming PLL, a jitter attenuator PLL, and LED drivers for status display. Other features such as jitter attenuator bypass, lobe bypass, and lobe test are included in the control logic. The PI2C3000A provides a robust signal retiming and conditioning for Token Ring Shielded Twisted Pair (STP) and Unshielded Twisted Pair (UTP) networks.

Figure 1. PI2C3000A Block Diagram

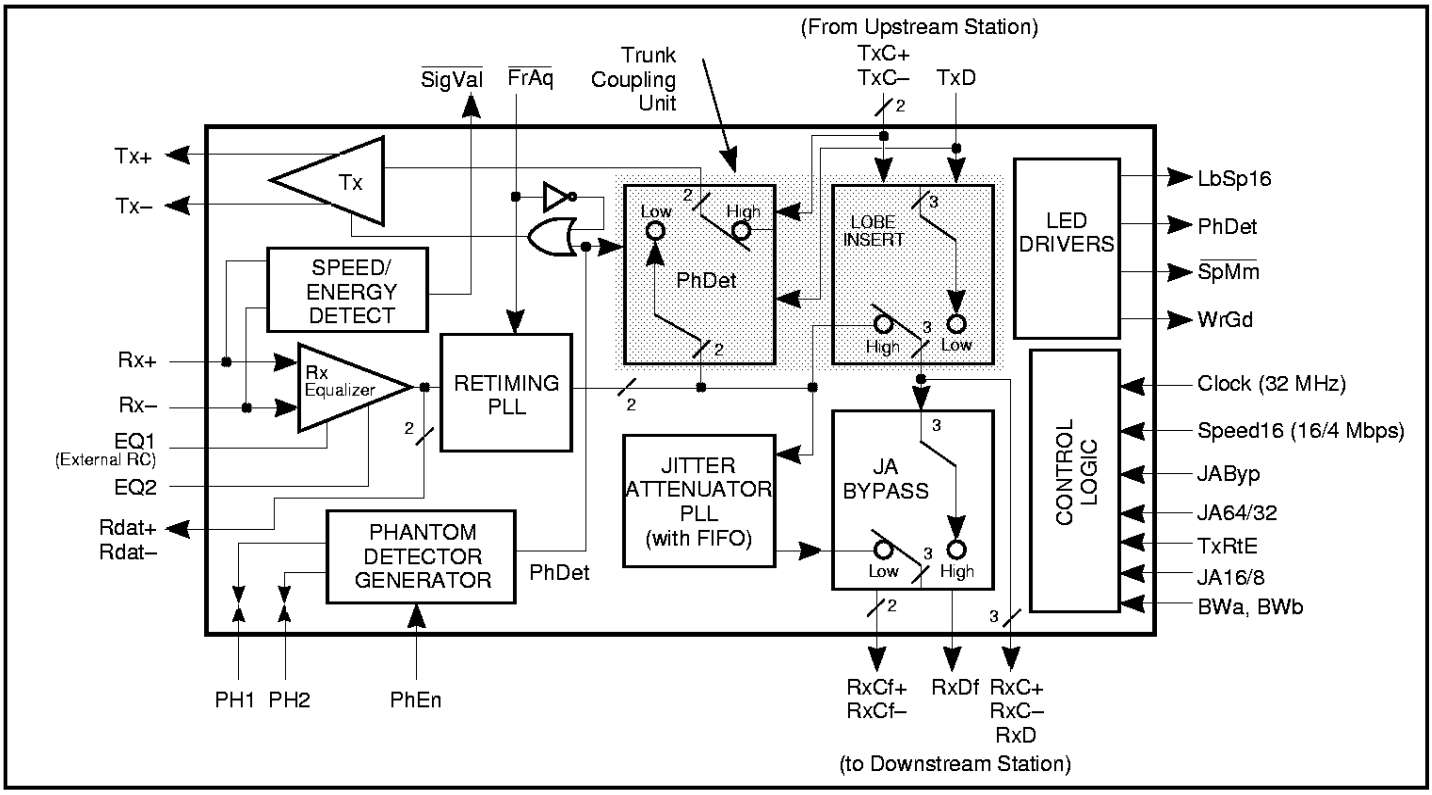
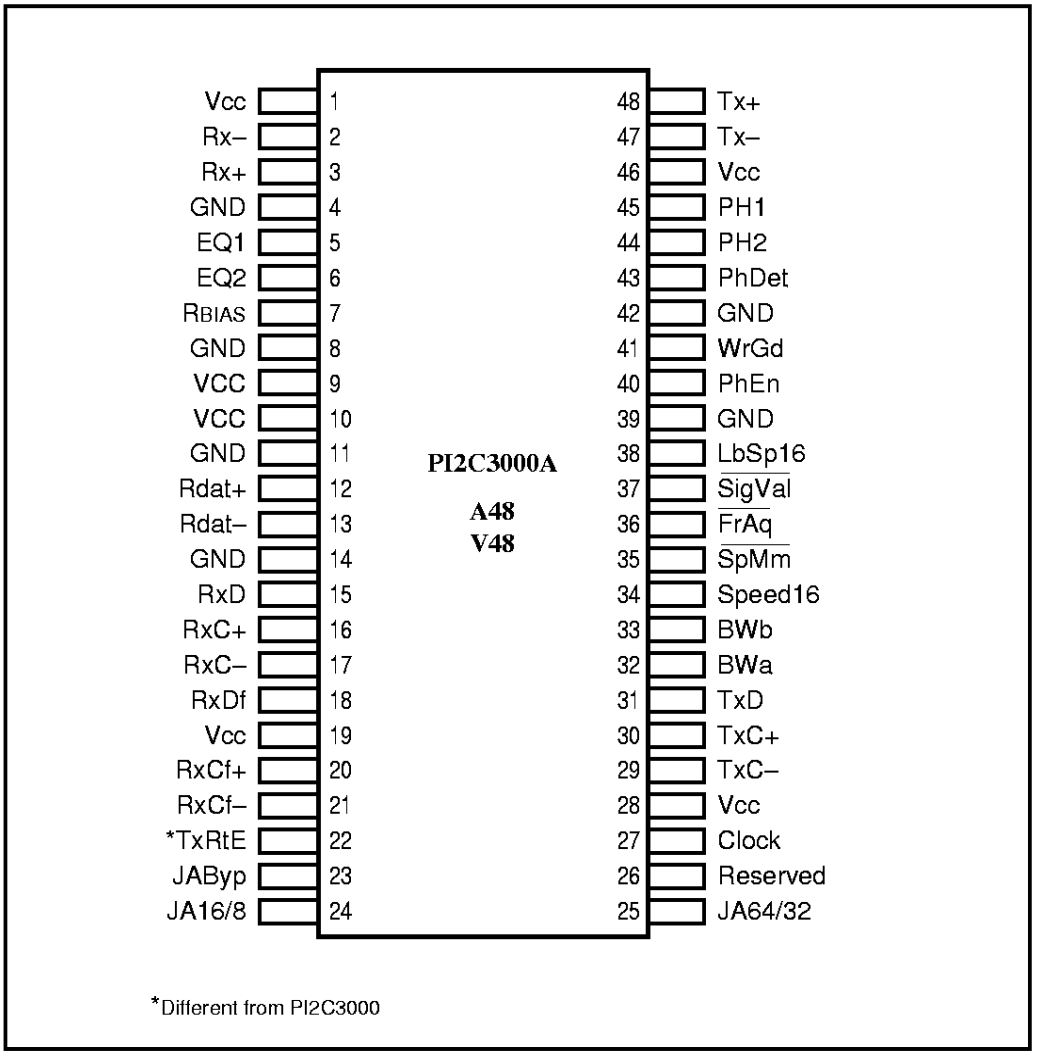


Figure 2. Product Pin Configuration



Product Pin Description

Pin No.	Symbol	I/O	Description
1	Vcc	—	**Receiver Power.**
2	Rx–	I	**Receiver Differential Negative Input.** Internally biased to 0.64 Vcc. Contact factory for single-ended implementations.
3	Rx+	I	**Receiver Differential Positive Input.** Internally biased to 0.64 Vcc.
4	GND	—	**Receiver Ground.**
5	EQ1	C	**Adaptive Equalizer First Terminal.** Connection for external components (see typical application circuit, page 15).
6	EQ2	C	**Adaptive Equalizer Second Terminal.** Connection for external components (see typical application circuit, page 15).
7	Rbias	C	**Bias Resistor** (6.04K, 1% resistor)**.** Sets the bias currents for internal circuits (see typical application circuit, page 15).
8	GND	—	**Bias Ground.**
9	Vcc	—	**Bias Power.**

I = input, O = output, C = component, - = N/A

Product Pin Description *(continued)*

Pin No.	Symbol	I/O	Description
10	Vcc	—	**Clock Generator Power.**
11	GND	—	**Clock Generator Ground.**
12	Rdat+	O	**Receiver Positive Digital Output.** Observation point for receiver output to fine tune the receive equalizer.
13	Rdat–	O	**Receiver Negative Digital Output.** Observation point for receiver output to fine tune the receive equalizer.
14	GND	—	**Digital PLL Ground.**
15	RxD(1)	O	**Received Data Output.** The signal on this pin is after the Retimer and before the jitter attenuator. 8mA drive.
16	RxC+(1)	O	**Received Clock Output.** The signal on this pin is after the Retimer and before the jitter attenuator. 8mA drive.
17	RxC–(1)	O	**Received Clock Inverse Output.** The signal on this pin is after the Retimer and before the jitter attenuator. 8mA drive.
18	RxDf	O	**Filtered Received Data Output.** This is the received data after the elastic buffer in the jitter attenuator. When JAByp is inactive (0), this pin will output jitter attenuated data (16 Mbps only). When JAByp is active (1), this pin will be the same as RxD. This pin will drive 8mA output.
19	Vcc	—	**Digital PLL Power.**
20	RxCf+	O	**Filtered Received Clock Output.** This is the dejittered received clock after the jitter attenuator. When JAByp is inactive (0), this pin will output the jitter attenuated clock. When JAByp is active (1), this pin will be the same as RxC+. 8mA driver output.
21	RxCf–	O	**Filtered Received Clock Inverse Output.** This is the received inverse clock after the jitter attenuator. When JAByp is inactive (0), this pin will output jitter attenuated data (16 Mbps only). When JAByp is active (1), this pin will be the same as RxC–. 8mA driver output.
22	TxRtE	I	**Tx Retime Enable.** When HIGH, TxD is clocked by the use of TxC+ and TxC– before being sent out to either Tx± or RxD. When LOW, TxC+ and TxC– are not needed. A buffered version of TxD will be sent to either Tx± or RxD.
23	JAByp	I	**Jitter Attenuator Bypass** (TTL-threshold CMOS Input). The jitter attenuator is bypassed when this pin is HIGH. When JAByp is HIGH (i.e., bypassed), RxCf+ output is the same as RxC+, RxCf– is the same as RxC– and RxDf output is the same as RxD. When JAByp is LOW, the jitter attenuator is enabled. In 4 Mbps mode, the jitter attenuator is always bypassed. **HIGH = Bypass, LOW = Enable Jitter Attenuation.**
24	JA16/8	I	**Jitter Attenuator Mode Select.** This pin selects a 16X or 8X attenuation rate. Normally, corrections to the dejittered data are applied once every 16 clocks when required. When set to 8X, corrections are applied every eight clocks. Recommended use at 16X setting. **HIGH = 16X, LOW = 8X.**

Note:
1. These pins are recommended to be NC for future compatibility purposes.

Product Pin Description *(continued)*

Pin No.	Symbol	I/O	Description
25	JA64/32	I	**Jitter Attenuator Elastic Buffer Size Select.** This pin sets the depth of the elastic buffer in the jitter attenuator. It can be either 64 clocks (peak-to-peak) deep or 32 clocks deep. Recommended use at 64X setting. **HIGH = 64 clocks, LOW = 32 clocks.**
26	Reserved	—	**This pin must be connected to digital ground.**
27	Clock	I	**32 MHz Input Clock** (TTL-threshold CMOS Input). Reference clock for the retiming VCO.
28	Vcc	—	**Digital Power.**
29	TxC–	I	**Transmitted Clock Inverse Input** (TTL-threshold CMOS Input).
30	TxC	I	**Transmitted Clock Input** (TTL-threshold CMOS Input).
31	TxD	I	**Transmitted Data Input** (TTL-threshold CMOS Input).
32	BWa	I	**Bandwidth Control pin.** Normally set HIGH (TTL-threshold CMOS Input).
33	BWb	I	**Bandwidth Control pin.** Normally set HIGH (TTL-threshold CMOS Input).
34	Speed16	I	**Speed Select Input** (TTL-threshold CMOS Input). Determines the hub speed. Lobe insertion (the physical breaking of the ring) is allowed only if the lobe speed matches Speed16. If the lobe speed does not match Speed16, lobe insertion is inhibited and a speed mismatch condition is indicated. **HIGH = 16 Mbps, LOW = 4 Mbps**
35	$\overline{\text{SpMm}}$	O	**Speed Mismatch Status Output.** CMOS output, when LOW, it indicates that the lobe speed does not match Speed16. When HIGH, it indicates that the lobe speed matches Speed16. The speed mismatch condition is latched and stays latched until the lobe station generates the right speed. 8mA Driver
36	$\overline{\text{FrAq}}$	I	**Frequency Acquisition Input** (TTL-threshold CMOS Input). When $\overline{\text{FrAq}}$ = HIGH, the Retiming PLL is locked to the local 32 MHz crystal. When $\overline{\text{FrAq}}$ = LOW, the Retiming PLL is locked to the incoming data.
37	$\overline{\text{SigVal}}$	O	**Signal Valid Status Output.** When LOW, it indicates a valid 4 Mbps or 16 Mbps data at the receiver inputs. $\overline{\text{SigVal}}$ is normally hard-wired to $\overline{\text{FrAq}}$ externally. 8mA output
38	LbSp16	O	**Lobe Speed Status Output.** This pin indicates the bit rate of the incoming signal at the receiver output. This signal is latched and indicates the lobe speed of the previous valid decision (either 4 or 16 Mbps). Lobe speed defaults to 16 Mbps at power-up. **HIGH = 16 Mbps** (16 MHz ≅ 4.8 MHz to 17.09 MHz), **LOW = 4 Mbps** (4 MHz ≅ 1.2 MHz to 4.2 MHz). 8mA output.
39	GND	—	**Digital Ground.**
40	PhEn	I	**Phantom Enable Input** (TTL-threshold CMOS Input). When HIGH, this pin is used to enable the phantom driver for Ring-In insertion (PH1 and PH2 source phantom drive). When LOW, this pin enables the phantom detector (inputs PH1 and PH2) for lobe port and Ring-Out port phantom detection. When HIGH, PhDet is also enabled. **Note:** WrGd (pin 41) is valid only if PhEn is HIGH.

Product Pin Description *(continued)*

Pin No.	Symbol	I/O	Description
41	WrGd	O	**Wire Good Status Output.** When HIGH, this pin indicates that the Ring-In insertion was successfully established in the phantom generate mode (see PhEn pin). When LOW, this pin indicates an open or short condition on PH1exists. 8mA output. **Note:** WrGd is valid only if PhEn is HIGH.
42	GND	—	**Transmitter Ground.**
43	PhDet	O	**Phantom Detect Status Output.** When HIGH, this pin indicates that the phantom voltage has been detected in the phantom detect mode (see PhEn pin). This pin is forced HIGH if PhEn is HIGH. 8mA output.
44, 45	PH2, PH1	I/O	**Phantom Input/Output**. When PhEn is HIGH, PH1 and PH2 become active HIGH output pins. They typically source 1 mA to the external loads at PH1 and PH2 and generate 4.1V. When PhEn is LOW, PH1 and PH2 are turned into active LOW input pins. The input receivers for these two pins are TTL-threshold CMOS buffers. When both PH1 and PH2 are LOW, PhDet will go HIGH. WrGd (Pin 41) indicates a valid load on PH1 when PhEn is HIGH.
46	Vcc	—	**Transmitter Power.**
47	Tx–	O	**Transmitter Negative Differential Output.** This output can drive 25 mA. (Balanced current drive outputs)
48	Tx+	O	**Transmitter Positive Differential Output.** This output can drive 25 mA. (Balanced current drive outputs)

Product Pin List by Name (in Alphabetical Order)

Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.
BWa	32	**JA16/8**	24	**Rx+**	3	**Tx–**	47
BWb	33	**JA64/32**	25	**Rx–**	2	**TxC+**	30
Clock	27	**JAByp**	23	**RxC+**(1)	16	**TxC–**	29
EQ1	5	**LbSp16**	38	**RxC–**(1)	17	**TxD**	31
EQ2	6	**PH1**	45	**RxCf+**	20	**TxRtE**	22
$\overline{\text{FrAq}}$	36	**PH2**	44	**RxCf–**	21	**Vcc**	1
GND	4	**PhDet**	43	**RxD**(1)	15	**Vcc**	9
GND	8	**PhEn**	40	**RxDf**	18	**Vcc**	10
GND	11	**Rbias**	7	**$\overline{\text{SigVal}}$**	37	**Vcc**	19
GND	14	**Rdat+**	12	**Speed16**	34	**Vcc**	28
GND	39	**Rdat–**	13	**$\overline{\text{SpMm}}$**	35	**Vcc**	46
GND	42	**Reserved**	26	**Tx+**	48	**WrGd**	41

Note:
1. These pins are recommended to be NC for future compatibility purposes.

Functional Description

Receiver

The receiver section consists of the receiver equalizer, the energy detect circuit and the retiming PLL. The receiver equalizer is a two-state amplitude adaptive equalizer. The same equalizer is used for both 4 or 16 Mbps operation. The equalizer operates in the nonlinear region for large signals (short cable) thereby effectively disabling the equalization, and it operates in the linear region for small signals (long cable) providing amplification for higher frequency signal components. External RC components are required to set the filtering characteristics of the equalizer (see Figures 8 and 9 for example). The Energy/ Speed Detect Circuit checks for the transition density of the incoming signal. When the required transition density is met in accordance with the speed configuration (4/16 Mbps) selected, a Signal Valid indication can be given to the retiming PLL so that the PLL can lock on to the incoming signal. The retiming PLL is frequency-locked to the 32 MHz reference clock input signal in the absence of valid received signal. The presence of valid received signal configures the retiming PLL to phase lock to the incoming signal (via the external connection from "$\overline{\text{SigVal}}$" to "$\overline{\text{FrAq}}$"). The retiming PLL is a constant gain PLL; no external loop filter is required.

Automatic Speed Detection

Lobe speed is checked constantly when a signal is present. A speed mismatch condition is indicated if the lobe speed does not match the hub speed through speed mismatch status output, "$\overline{\text{SpMm}}$." When the speeds are matched, the retiming PLL speed is configured appropriately upon receipt of a valid signal to allow the station to pass the lobe test (just as in a passive hub).

The retiming PLL speed is set by the hub speed (Speed 16 pin). Lobe insertion will be inhibited if the lobe speed does not match the hub speed; the speed mismatch indication is retained (from lobe test). Lobe insertion will be allowed only if the lobe speed matches the hub speed, phantom voltage is detected, and there is a valid signal.

If phantom is asserted during a speed mismatch condition, the Tx outputs will be enabled with the live hub data stream to allow auto speed detection in the NIC to map properly.

Speed Detection Table

Frequency (MHz)	$\overline{\text{SpMm}}$	$\overline{\text{SigVal}}$	LbSp16	Speed 16
4.80 t0 17.09	False	True	16	16
1.19 to 4.20	False	True	4	4

Speed Energy Detect

This section outputs the "$\overline{\text{SigVal}}$" signal when the incoming signal at "Rx±" meets the criteria for operation at 4 Mbps or 16 Mbps. "LbSp16" indicates the bit rate of the incoming signal and retains the value of the previous valid decision (4 or 16 Mbps). It defaults to 16 Mbps at power up. "$\overline{\text{SigVal}}$" is normally hard-wired to "$\overline{\text{FrAq}}$" externally.

Speed Energy Detect Criteria:

Voltage Hysteresis	±10 mV
Pulse Width	at least 10 ns
Transition Density	> 6 rising transitions but ≤ 16 rising transitions in 16BT

Lobe speed is declared after four consecutive passages of the transition density test (after a total of 64 bits, a running average rather than just average of a snapshot).

(16 MHz ≅ 4.8 MHz to 17.09 MHz and 4 MHz ≅ 1.2 MHz to 4.2 MHz)

Retiming PLL

"$\overline{\text{FrAq}}$" configures the retiming PLL to frequency lock ($\overline{\text{FrAq}}$ = 1) to the local 32 MHz crystal or to phase lock ($\overline{\text{FrAq}}$ = 0) to the incoming data from the receiver output. The retiming PLL speed is determined by lobe speed during lobe test and by hub speed when the lobe is inserted.

When there is no input, the retiming PLL locks on to the external 32 MHz reference clock. When there is a valid input, the PLL locks on to the phase and frequency of the input data.

Jitter Attenuator

The Jitter Attenuator is an extremely low bandwidth PLL used to attenuate the phase slope of the incoming signal. A 32-bit (64 clock) elastic buffer is provided to accommodate the accumulated phase jitter in the ring. The recovered clock (RxC) from the retiming PLL is used to clock the recovered data (RxD) into the elastic buffer, and the filtered recovered clock (RxCf) from the jitter attenuator PLL is used to clock the recovered data out of the elastic buffer.

The elastic buffer is auto-centering; it does not require a Token for recentering. The "fullness" and the "emptiness" of the elastic buffer are used as the error information in the feedback loop of the jitter attenuator PLL. When the jitter attenuator PLL is in the steady state condition (RxC is stable and its phase is constant and not varying), the elastic buffer is half full. The size of the buffer can be set via pin 25 "JA64/32." The 32-clock mode is useful to minimize latency in a relatively quiet network.

In a noisy environment (i.e., large networks), the 8X mode can be selected to apply phase corrections at a more frequent rate. In a quiet environment (i.e., small networks), the 16X mode can be selected to minimize unnecessary phase corrections. The jitter attenuator is enabled only when the Speed16 is HIGH (16 Mbps), JAByp is LOW (JA enabled), and the lobe is inserted.

Transmitter

The line driver takes the transmit clock and differential Manchester data of the upstream station and drives the cable in the normal lobe-inserted state. It takes the received clock and data from the retiming PLL during lobe test when bypassed (prior to lobe insertion). The line driver is idle (no data transitions) in the absence of a valid received signal or phantom voltage. The line driver is a current output typically used with a step down (2:1) isolation transformer. The drive current is 25 mA. The transmitter is also active if phantom is detected, but the speed of the incoming data is mismatched to the Speed16 input setting.

The PI2C3000A provides the capability of sending a buffered version of TxD to the differential line drivers Tx+ and Tx– or CMOS driver RxD when both TxC+ and TxC– are not available. In this case, TxRtE (pin 22) should be tied LOW. The unused TxC+, TxC– pins should be tied to either Vcc or Ground. This mode is provided for switched or MAC base applications where only data is available.

Phantom Detector/Generator and Lobe Bypass

The phantom detector senses (indirectly via optoisolators to PH1 and PH2 pins) the DC phantom voltage generated by the lobe station. The phantom voltage generated by the station is an indication to the concentrator that the station wants to be inserted in the ring. In the absence of phantom voltage, the PhDet is LOW, and the retiming PLL output is routed to the line driver for lobe test purposes. Upon receipt of the phantom voltage, transmit clock and data (TxC and TxD) of the upstream station are routed to the line driver, and the received clock and data (RxC and RxD) of the lobe station are routed to the downstream station.

When PhEn is enabled typically for a station or Ring-In configuration, the PH1 and PH2 pins will become outputs to generate the phantom voltage/current needed to request an insertion. In this state, the phantom detect pin (PhDet) will be asserted.

For hub interconnection, the Ring-In port of the second hub generates the phantom voltage and the Ring-Out port of the first hub detects the phantom voltage in a similar manner that a lobe station is inserted in the ring. A "wire-good" indication is provided in the Ring-In port of the second hub, and a "phantom detect" indication is provided in the Ring-Out port of the first hub to validate the integrity of the connection.

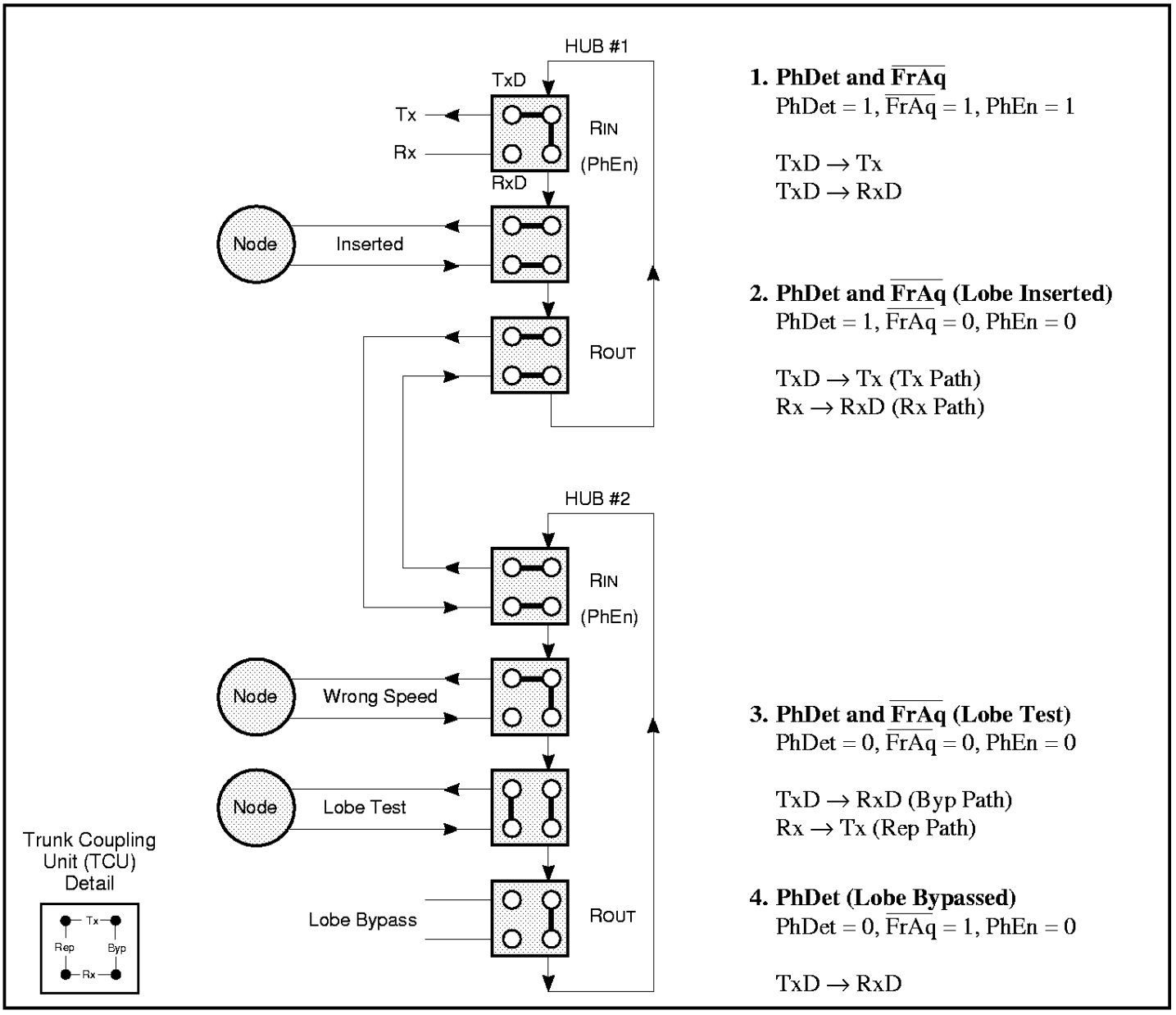
Examples of the data flow during the ring insertion are shown in Figures 3 and 4.

LED Drivers

The LED drivers provide status for the following signals: Phantom Detect for lobe port and Ring-Out (phantom detect mode, PhEn pin = LOW), Wire-Good for Ring-In (phantom generate mode, PhEn pin = HIGH), valid received signal, lobe speed, and speed mismatch.

RING INITIALIZATION PROCESS

Figure 3. Data Path Control



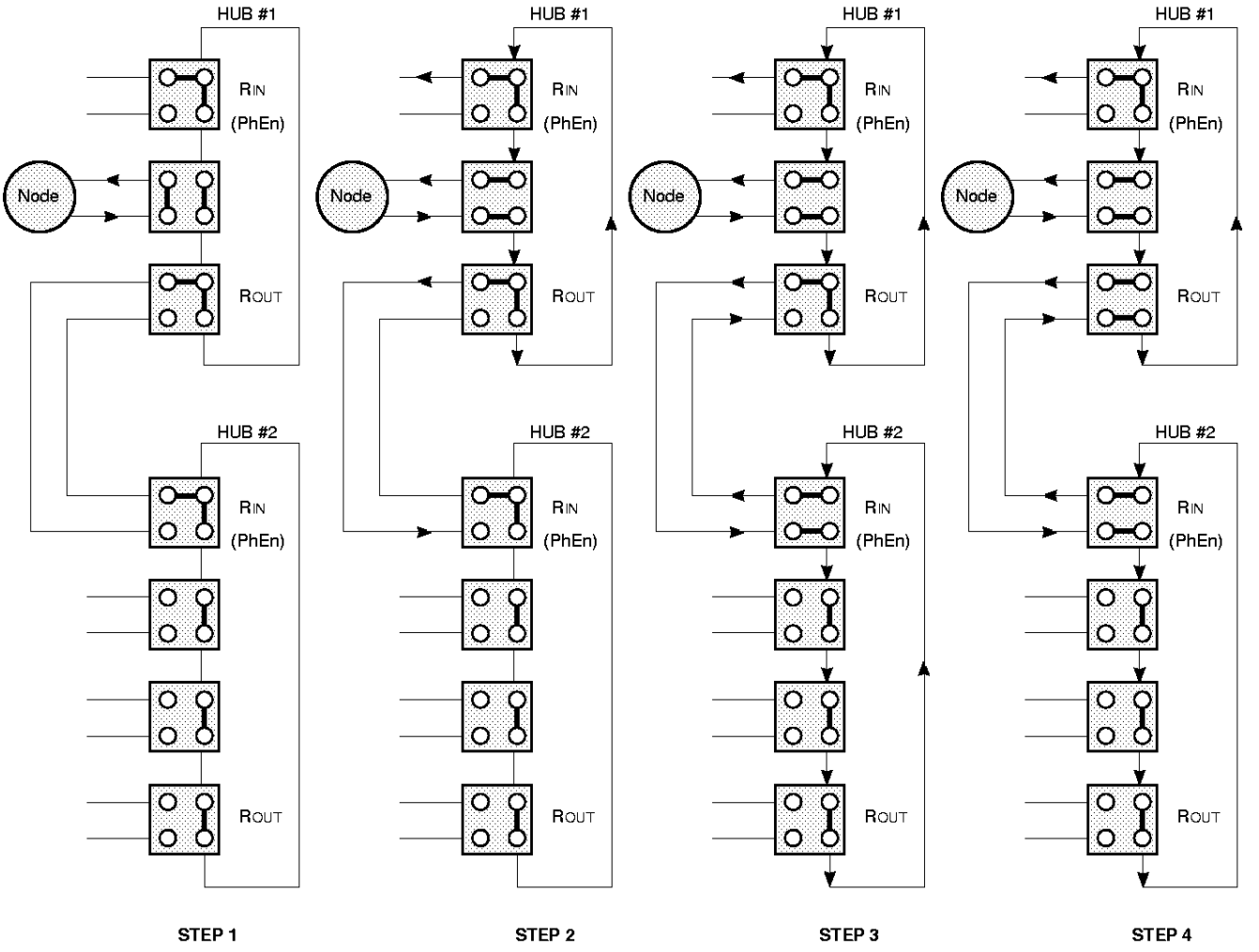
Normal Port Configuration (or Ring-Out Mode)

PhEn	PhDet	FrAq	Rep Path	Tx Path	Rx Path	Byp Path	Comments
0	0	1	Off	Off	Off	On	Lobe (No SigVal)
0	0	0	On	Off	Off	On	Lobe Test
0	1	0	Off	On	On	Off	Lobe Insert (LbSp16 = Speed16)
0	1	1	Off	On	Off	On	Unknown Signal or SpMm

Ring-In Configuration (Repeater or Station Mode)

PhEn	PhDet	FrAq	Rep Path	Tx Path	Rx Path	Byp Path	Comments
1	1	1	Off	On	Off	On	Ring-In – Ignores invalid signal or SpMm condition
1	1	0	Off	On	On	Off	Ring-In Active

Figure 4. Procedure For Ring Insertion



Step 1. The node is performing a lobe test.

Step 2. The node inserts and the data signal starts to flow in Hub#1.

Step 3. Ring-In of Hub#2 detects a valid signal and lets the data signal to flow in Hub#2.

Step 4. Ring-Out of Hub#1 detects a valid signal and connects Hub#2 to Hub#1.

Electrical and Timing Characteristics

Retiming PLL Characteristics

Description	4 Mbps Min	4 Mbps Typ	4 Mbps Max	16 Mbps Min	16 Mbps Typ	16 Mbps Max	Unit
PLL Bandwidth	—	90	—	—	360	—	KHz
Jitter Tolerance	±2.0	—	—	±0.56	—	—	ns/UI
Accu. Phase Slope	—	—	1.0	—	—	0.25	ns/UI
Static Alignment	—	—	—	—	—	1	ns

Phantom Detect/Generate Voltage

Condition	Min	Typ	Max	Unit
Phantom Voltage @ 1 mA	—	4.1	—	V

Line Driver Characteristics

Description	Min	Typ	Max	Unit
Output Voltage	3.00	3.75	4.50	V
Differential Twisted Pair Transit Skew	—	—	1	ns

LED Status

Description	Min	Typ	Max	Unit
Drive Current	—	8	—	mA

DC Electrical Characteristics

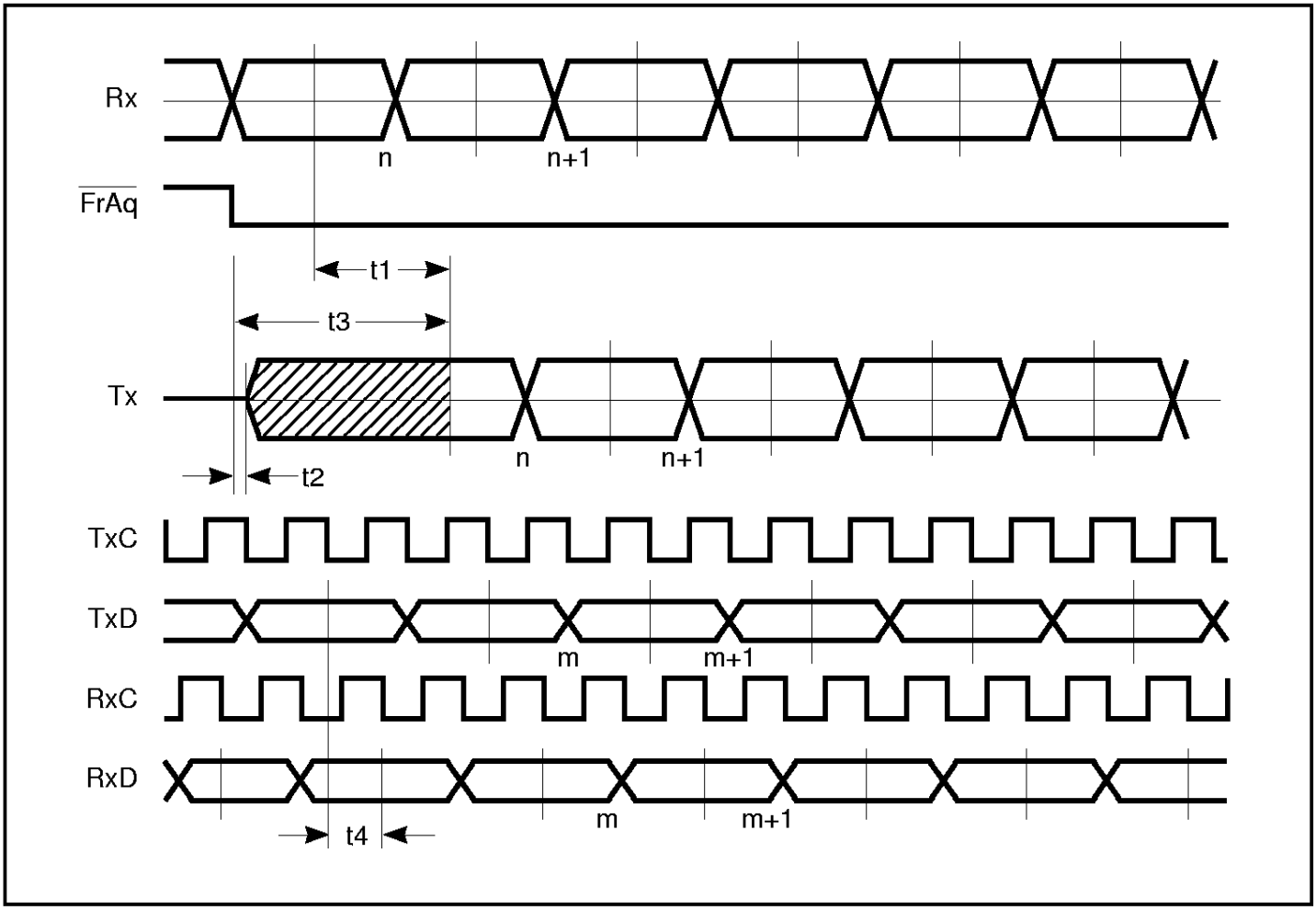
Description	Min	Typ	Max	Unit
Supply Voltage	4.75	5.0	5.25	V
Suppy Current	—	161	—	mA

Lobe Timing Characteristics (Lobe Bypassed State, PH1 or PH2 = HIGH)

Parameters	Description	Min.	Typ.	Max.	Units
t1	Line receiver to line driver propagation delay (with retime)	—	0.5BT + 15	—	ns
t2	Phase acquisition ($\overline{\text{FrAq}}$ = LOW) to line driver output enable delay	—	3	—	ns
t3	Phase acquisition ($\overline{\text{FrAq}}$ = LOW) to line driver output valid delay	—	2BT + 3	—	ns
t4	TxD to RxD delay	—	0.25BT + 9	—	ns

BT = Bit Time

Figure 5. Lobe Timing (Lobe Bypassed, Lobe Test, PH1 or PH2 = HIGH)

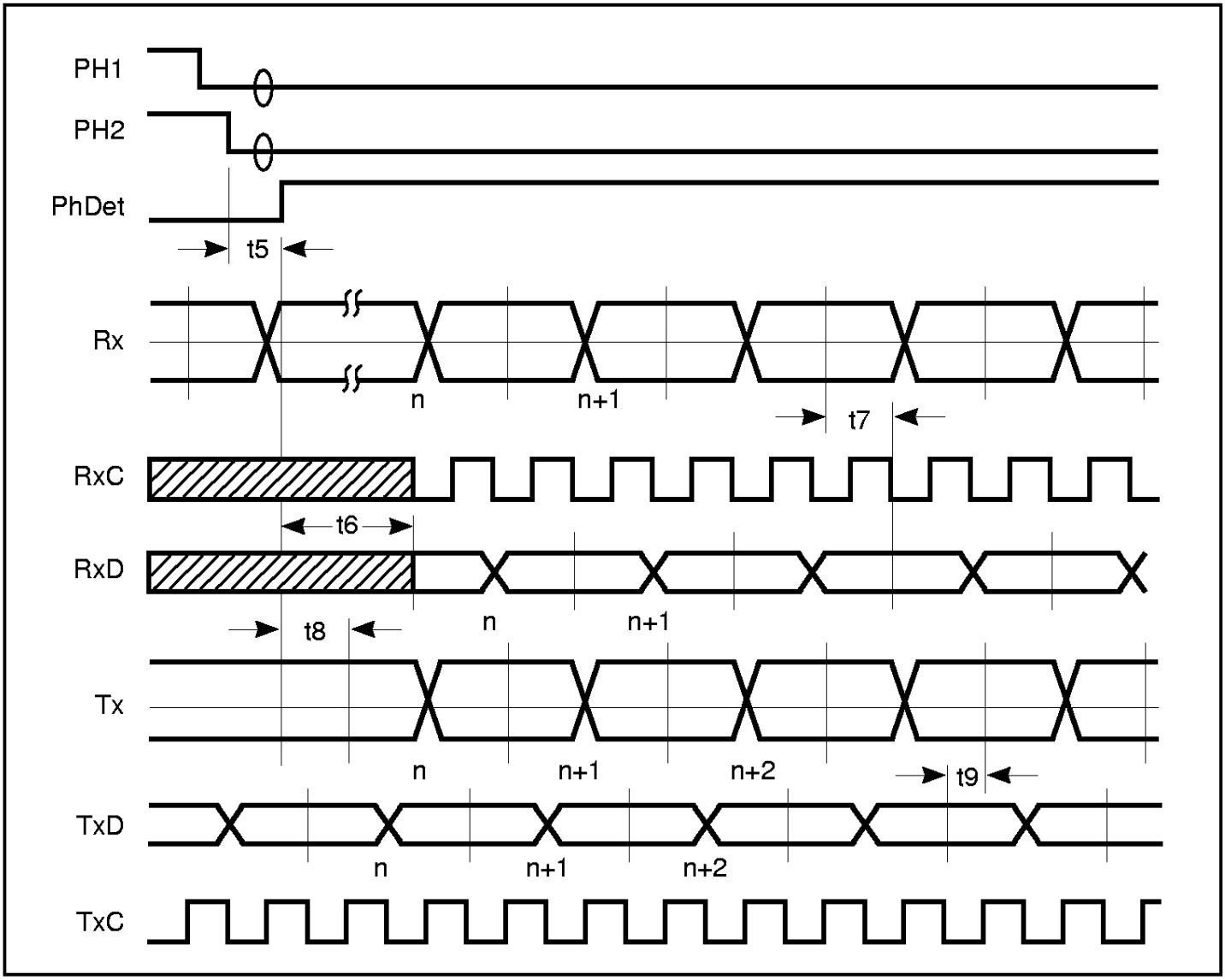


Lobe Timing Characteristics (Lobe Inserted State, PH1 = PH2 = LOW)

Parameters	Description	Min.	Typ.	Max.	Units
t5	Phantom detection delay	—	5	—	ns
t6	Phantom detection to RxD valid	—	0.25BT + 3	—	ns
t7	Line receiver to RxD propagation delay	—	0.25BT + 14	—	ns
t8	Phantom detection to line driver output valid	—	0.5BT + 5	—	ns
t9	TxD to line driver output delay	—	0.25BT + 8	—	ns

BT = Bit Time

Figure 6. Lobe Timing (Lobe Inserted, PH1 or PH2 = LOW)

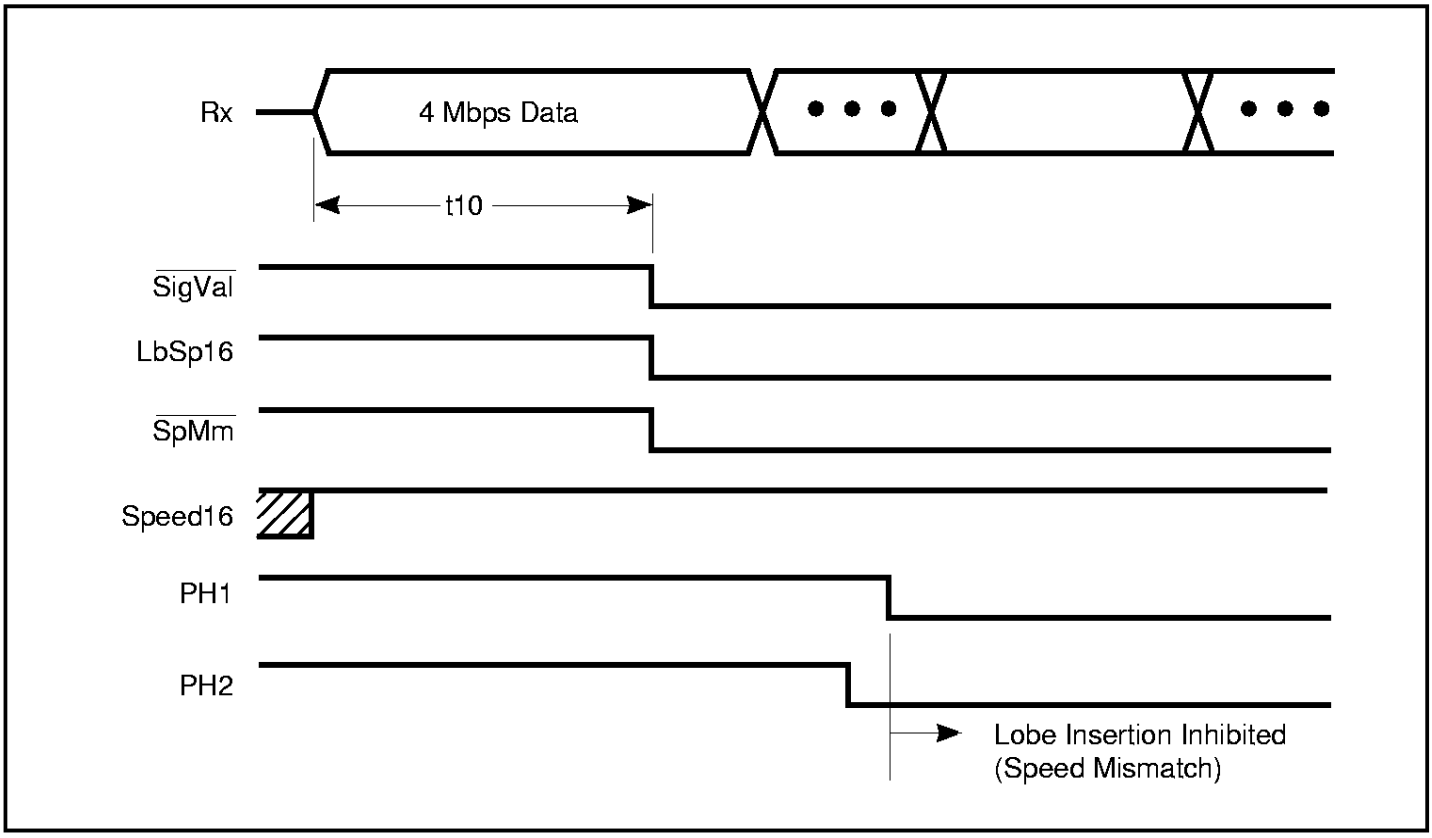


Signal Valid Timing Characteristics

Parameters	Description	Min.	Typ.	Max.	Units
t10	Line receiver to $\overline{\text{SigVal}}$, LbSp16, and $\overline{\text{SpMm}}$ delay	—	64BT + 75	—	ns

BT = Bit Time

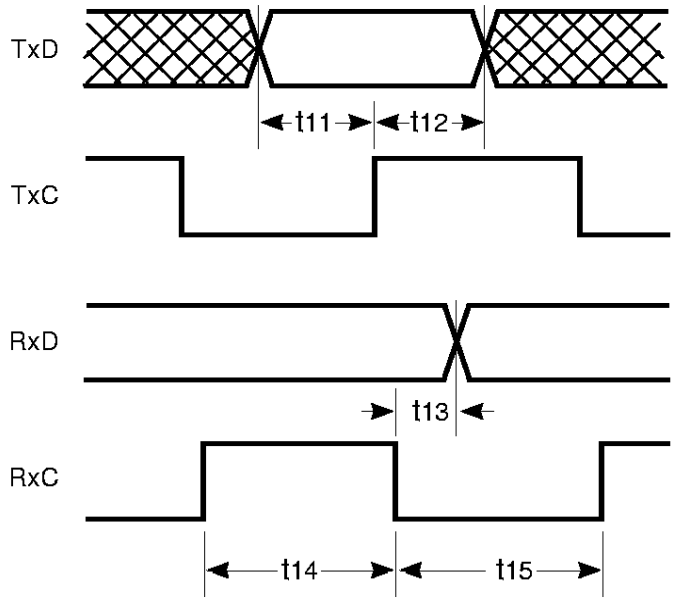
Figure 7. Signal Valid and Speed Mismatch Timing



Data Timing Characteristics

Parameters	Description	Min.	Typ.	Max.	Units
t11	TxD to TxC setup	3	—	—	ns
t12	TxD to TxC hold	2	—	—	ns
t13	RxD to RxC delay	—	2	4	ns
t14	RxC high	12	—	—	ns
t15	RxC low	12	—	—	ns

Figure 8. Data Timing



Transmit Output Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
t16	Tx± Rise/Fall Time (10% to 90%, 90% to 10%)	1	—	5	ns

Figure 9. Transmit Output

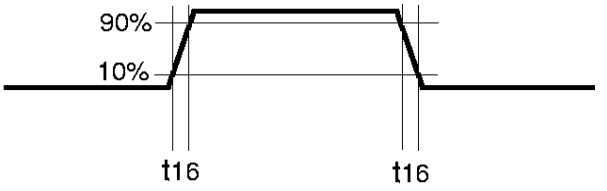
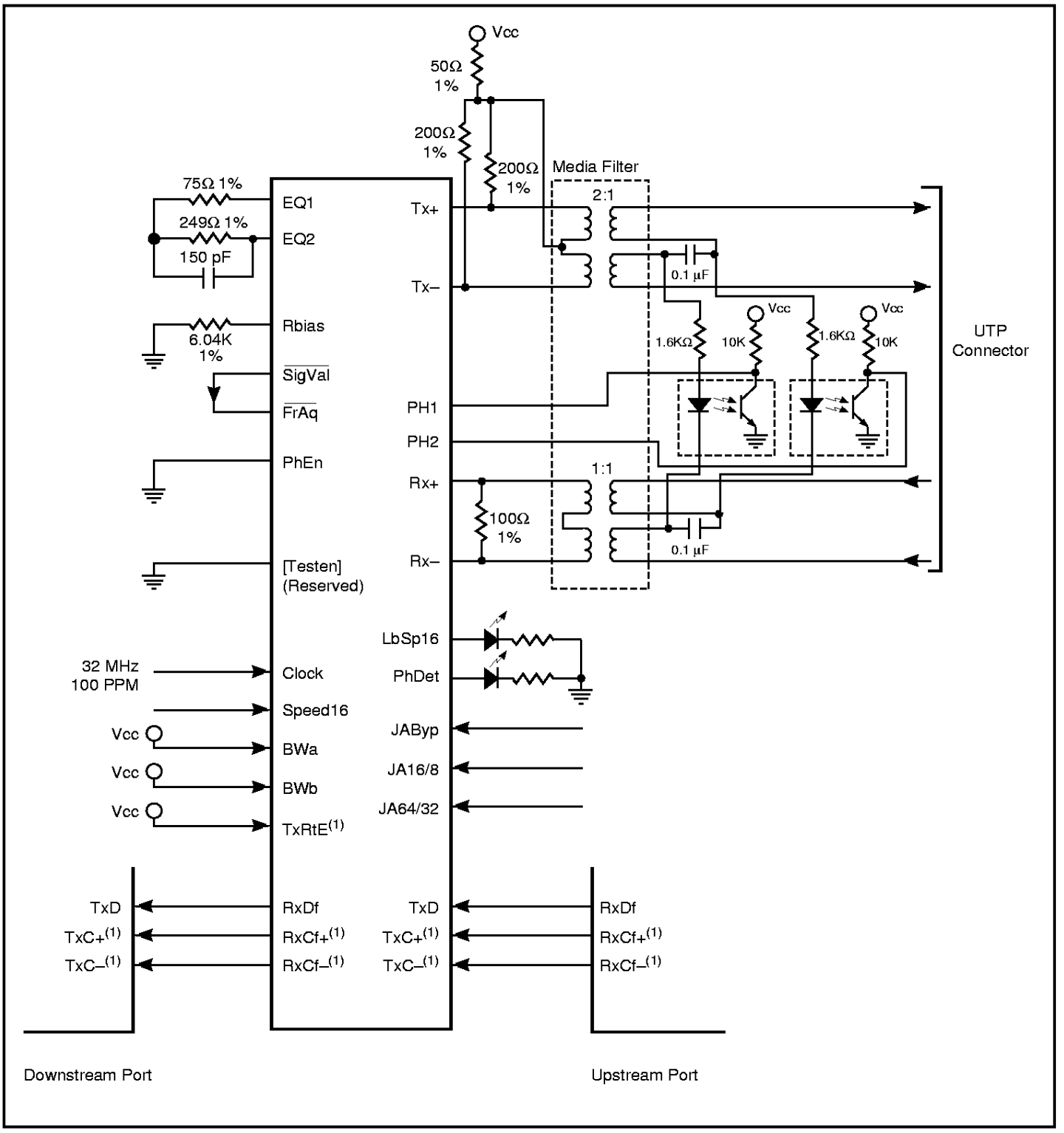
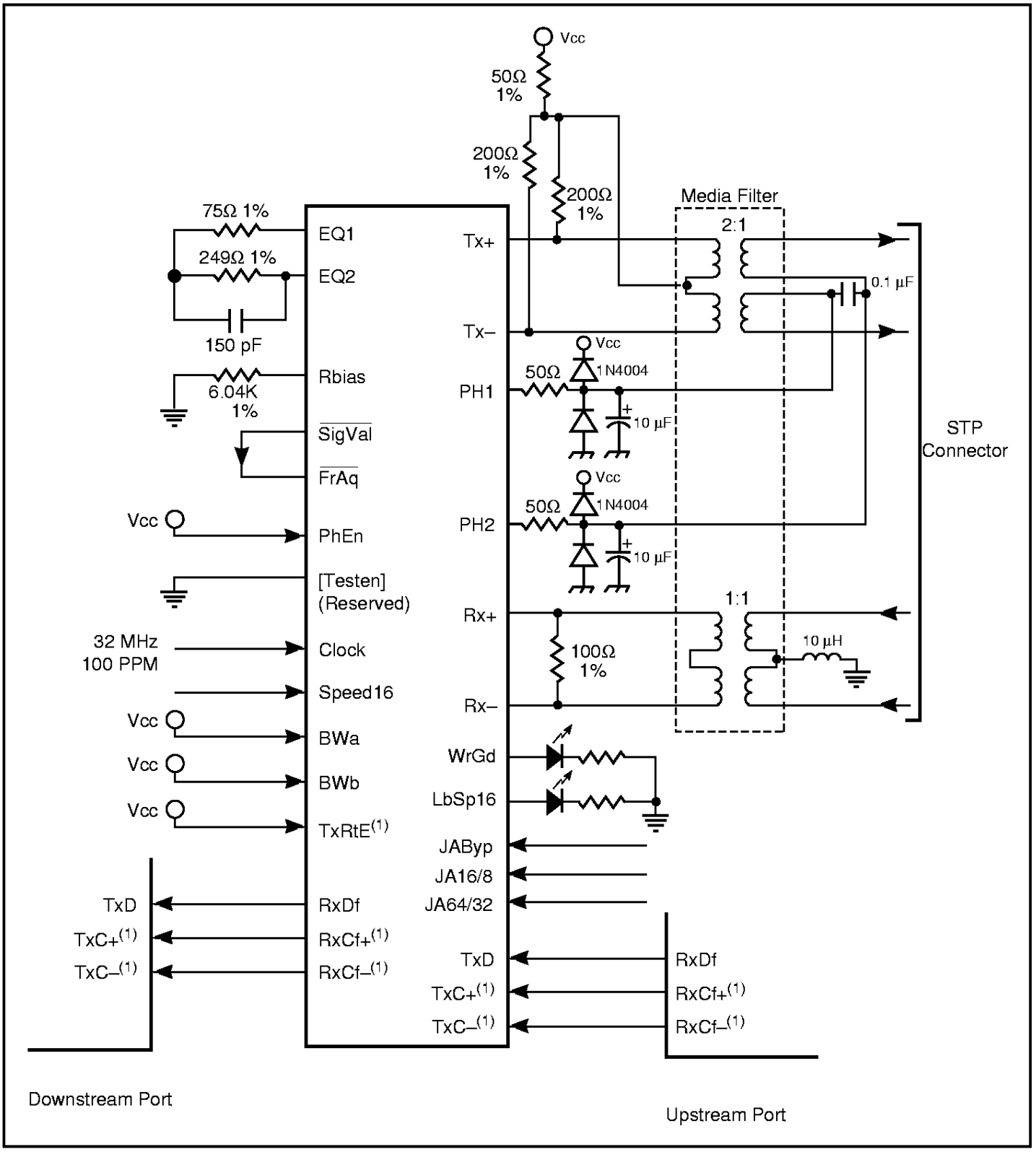


Figure 10. Typical Circuit Application (Lobe Port and Ring-Out Port)



Note:
1. If TxRtE = GND, TxC+ and TxC– are not required and should be connected to Vcc or GND.

Figure 11. Typical Circuit Application (Ring-In Port)



Note:
1. If TxRtE = GND, TxC+ and TxC– are not required and should be connected to Vcc or GND.

LIFE SUPPORT POLICY

Pericom Semiconductor Corporation's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of PSC.

1. Life support devices or systems are devices or systems which:
   (a) are intended for surgical implant into the body, or
   (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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