September 1990
Edition 1.0

FUJITSU

DATA SHEET

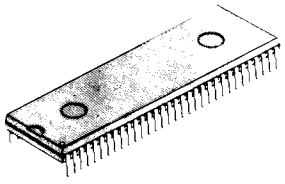
MB86151/MB86152
PICTURE IN PICTURE CONTROLLER

PICTURE IN PICTURE CONTROLLER FOR TV AND VCR (PAL MODE)

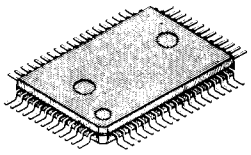
The MB86151/MB86152 are picture-in-picture controller which permit the incorporation of the picture-in-picture viewing mode into television sets and VCRs.

When combined with the MB81461 (256K-bit dual-port RAM), the MB40176 (A/D and D/A converters), and the MB3511 (PLL IC for PIP), a picture-in-picture system is formed.

- PAL mode
- Separate/Compress/Composite function of brightness signal and colour signal
- Memory control function
- Motion picture mode (all field)
- Selectable sub-picture position: Upper left, lower left upper right, or lower right
- Video signal input: PAL composite video signal (6Bit/4fsc)
- Sub picture video signal output:
  PAL composite video signal (6Bit/4fsc)
- Single supply voltage: +5V
- 64-pin plastic dual-in-line package: MB86152
  64-pin plastic flat package: MB86151



PLASTIC PACKAGE
DIP-64P-M01
(MB86152)



PLASTIC PACKAGE
FPT-64P-M01
(MB86151)

ABSOLUTE MAXIMUM RATINGS (see NOTE)

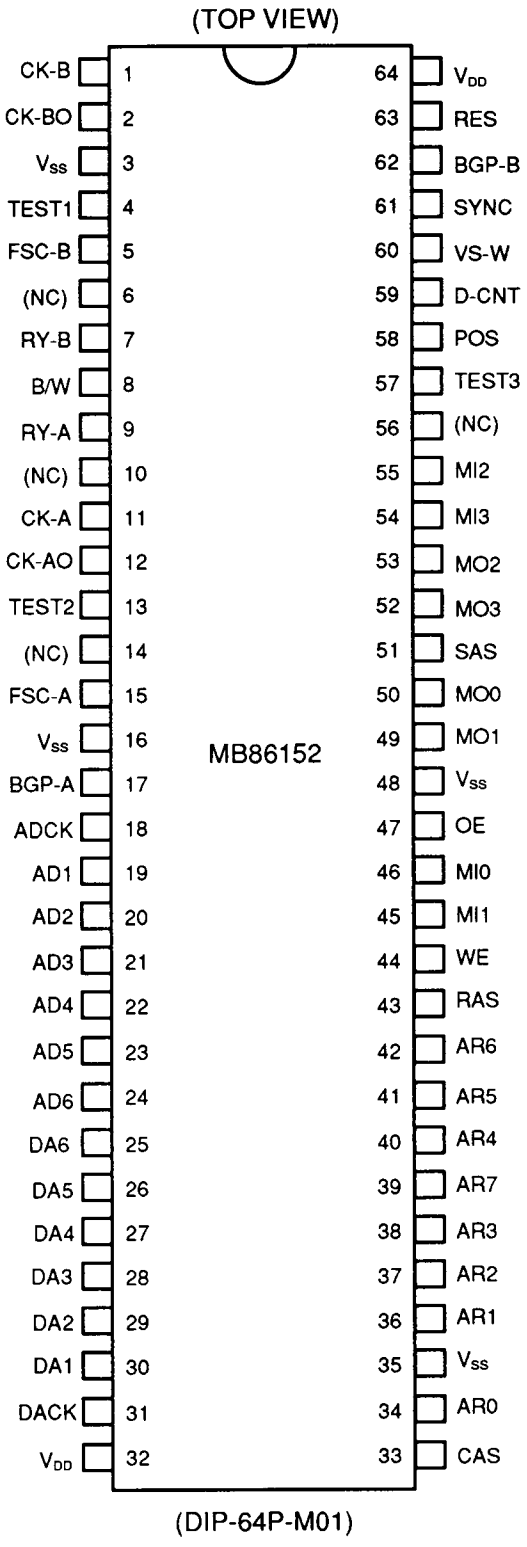
(V_{SS} = 0V)

Ratings		Symbol	Condition		Value	Unit
Supply Voltage		V_{DD}			V_{SS} –0.5 to 6.0	V
Input Voltage		V_I			V_{SS} –0.5 to V_{DD} +0.5	V
Output Voltage		V_O			V_{SS} –0.5 to V_{DD} +0.5	V
Operating Temperature		T_A			–25 to +85	°C
Storage Temperature		T_{STG}			–40 to +125	°C
Output Current	Except SAS pin	I_O	V_{DD} = Max. I_{OL} = 3.2mA	$V_O = V_{DD}$	+40	mA
				V_O = 0V	–40	
	SAS pin	I_O	V_{DD} = Max. I_{OL} = 8.0mA	$V_O = V_{DD}$	+80	mA
				V_O = 0V	–80	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

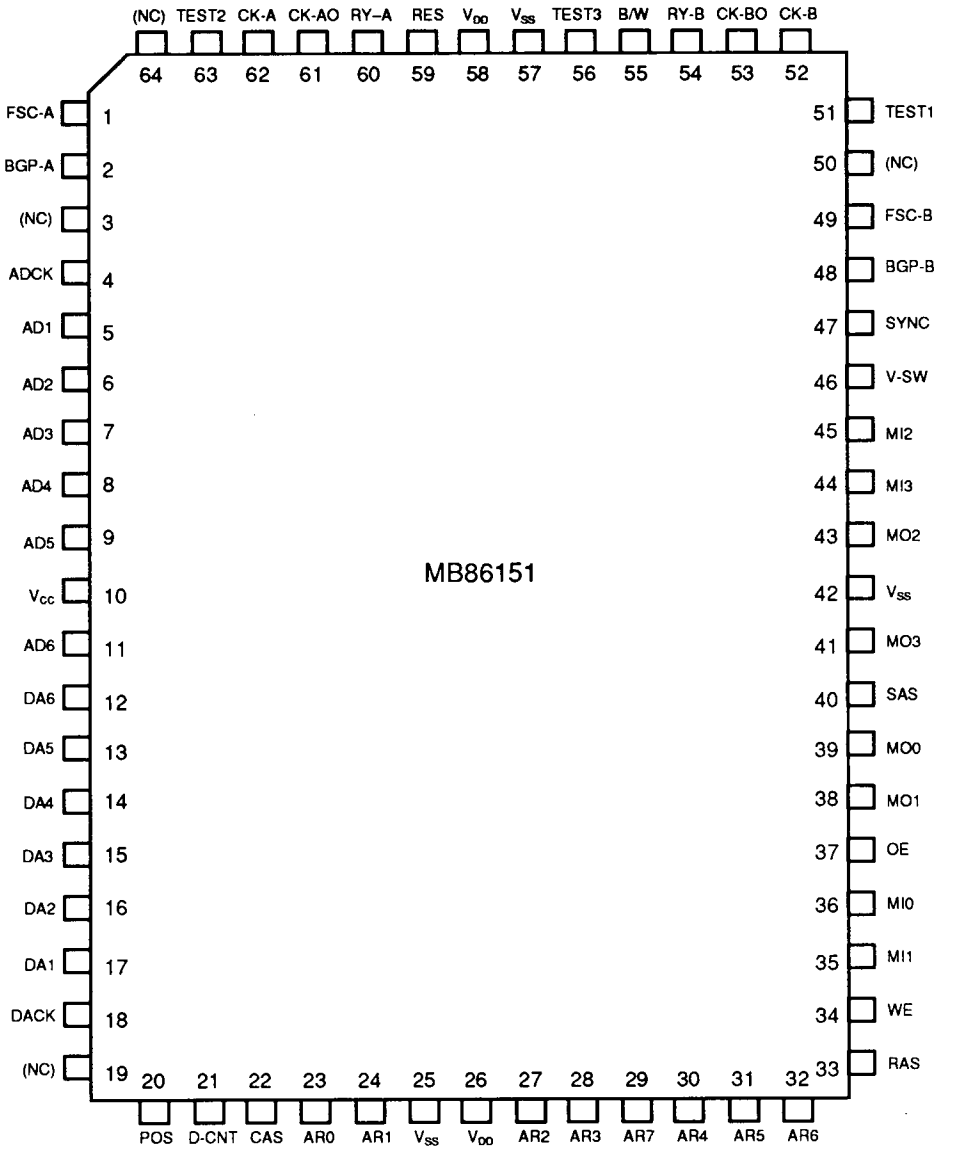
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT



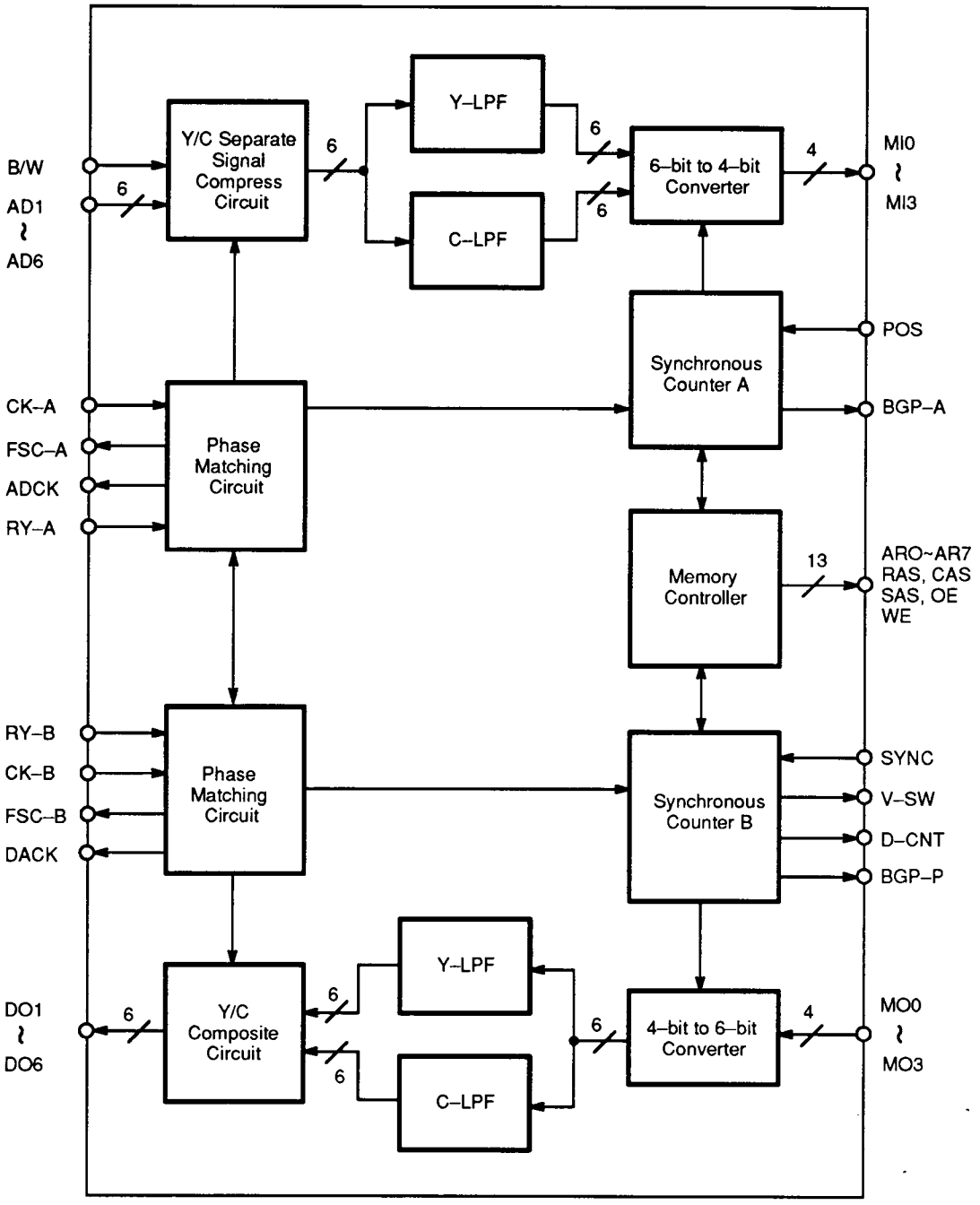
PIN ASSIGNMENT (Continued)

(TOP VIEW)



(FPT-64P-M01)

MB86151/MB86152 BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.		Symbol	I/O	Descriptions	Connection
MB86151	MB86152				
20	58	POS	I_{SM}	Picture in picture mode selection/sub picture position control pin ⎍ :Picture in picture mode/sub picture position control H level :Main picture mode	Controller
21	59	D-CNT	O	Picture in picture mode display output pin H level :Picture in picture mode display L level :Main picture mode display	
59	63	RES	I_T	Reset signal input pin H level :Normal operational mode L level :Reset mode	
46	60	V-SW	O	Video switch control signal output pin for picture in picture composition	MB3511
47	61	SYNC	I_T	Main picture composite sync input pin	
55	8	B/W	I_C	Sub picture colour/black and white sensing pin	
62	11	CK-A	I_C	Sub picture 4fsc input pin	
61	12	CK-AO	B_C	Sub picture 4fsc amp output pin	
60	9	RY-A	I_C	Sub picture colour phase input pin	
52	1	CK-B	I_C	Main picture 4fsc input pin	
53	2	CK-BO	B_C	Main picture 4fsc amp output pin	
54	7	RY-B	I_C	Main picture colour phase input pin	
1	15	FSC-A	O	Sub picture fsc output pin (PLL input signal)	
49	5	FSC-B	O	Main picture fsc output pin (PLL input signal)	
2	17	BGP-A	O	Sub picture burst gate pulse output pin	
48	62	BGP-B	O	Main picture burst gate pulse output pin	
5	19	AD1	I_T	Sub picture video signal input pin (MSB)	MB40176
6	20	AD2	I_T	Sub picture video signal input pin	
7	21	AD3	I_T	Sub picture video signal input pin	
8	22	AD4	I_T	Sub picture video signal input pin	
9	23	AD5	I_T	Sub picture video signal input pin	
11	24	AD6	I_T	Sub picture video signal input pin (LSB)	
12	25	DA6	O	Sub picture video signal output pin (LSB)	
13	26	DA5	O	Sub picture video signal output pin	
14	27	DA4	O	Sub picture video signal output pin	
15	28	DA3	O	Sub picture video signal output pin	
16	29	DA2	O	Sub picture video signal output pin	
17	30	DA1	O	Sub picture video signal output pin (MSB)	
4	18	ADCK	O	AD converter clock output pin	
18	31	DACK	O	DA converter clock output pin	

Note: I_T : TTL interface input pin
I_C : CMOS interface input pin
B_C : CMOS interface tri-state pin
I_{SM} : CMOS schmitt trigger input pin

PIN DESCRIPTIONS (Continued)

Pin No.		Symbol	I/O	Descriptions	Connection
MB86151	MB86152				
22	33	CAS	O	Memory CAS (Column address) control output pin	MB81461
23	34	AR0	O	Memory address output pin	
24	36	AR1	O	Memory address output pin	
27	37	AR2	O	Memory address output pin	
28	38	AR3	O	Memory address output pin	
29	39	AR7	O	Memory address output pin	
30	40	AR4	O	Memory address output pin	
31	41	AR5	O	Memory address output pin	
32	42	AR6	O	Memory address output pin	
33	43	RAS	O	Memory RAS (Row address) control output pin	
34	44	WE	O	Memory WE (Write enable) output pin	
35	45	MI1	O	Sub picture video signal output pin (Memory input)	
36	46	MI0	O	Sub picture video signal output pin (Memory input)	
37	47	OE	O	Memory OE (Output enable) output pin	
38	49	MO1	I_T	Sub picture video signal input pin (Memory output)	
39	50	MO0	I_T	Sub picture video signal input pin (Memory output)	
40	51	SAS	O	Memory SAS (Serial access) control output pin	
41	52	MO3	I_T	Sub picture video signal input pin (Memory output)	
42	53	MO2	I_T	Sub picture video signal input pin (Memory output)	
44	54	MI3	O	Sub picture video signal output pin (Memory input)	
45	55	MI2	O	Sub picture video signal output pin (Memory input)	
26	32	V_{DD}	–	Supply voltage input pin (+5V)	+5V
58	64	V_{DD}	–	Supply voltage input pin (+5V)	
10	3	V_{SS}	–	Ground (0V)	GND
25	16	V_{SS}	–	Ground (0V)	
42	35	V_{SS}	–	Ground (0V)	
57	48	V_{SS}	–	Ground (0V)	
51	4	TEST1	I_T	Test pin (This pin is grounded)	GND
63	13	TEST2	I_T	Test pin (This pin is grounded)	GND
56	57	TEST3	I_T	Test input pin (This pin is set to low in operation)	L level
3	6	(NC)	–	(No connection)	–
19	10	(NC)	–	(No connection)	–
50	14	(NC)	–	(No connection)	–
64	56	(NC)	–	(No connection)	–

Note: I_T : TTL interface input pin

FUNCTIONAL DESCRIPTIONS

PICTURE IN PICTURE MODE

The picture in picture mode and sub picture position are selected by POS pin input level. The input condition is shown below. Input timing is shown in Fig. 1 and sub picture position is shown in Fig.2.

PICTURE MODE SELECTION AND SUB PICTURE POSITION CONTROL PIN (POS)

POS Pin	Mode	Note
⎍	Picture in picture	The sub-picture shifts lower right, upper right, upper left, lower left by the each pulse.
5V	Main picture	Release picture in picture mode.

Fig. 1 – SUB PICTURE POSITION CONTROL PULSE TIMING

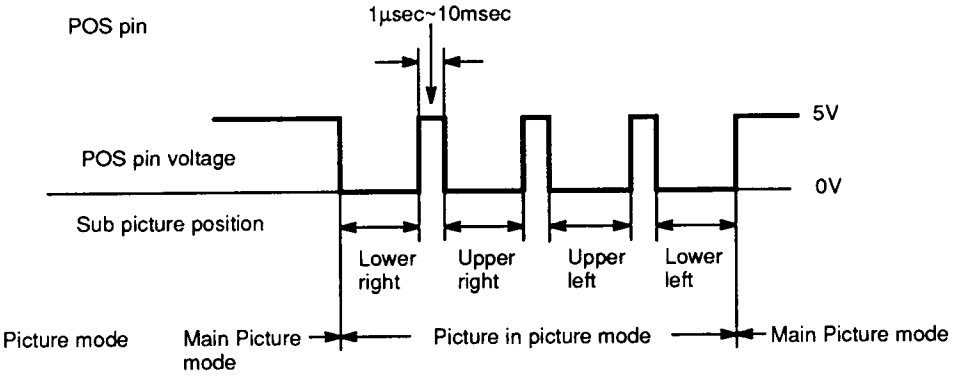


Fig. 2 – SUB PICTURE POSITION SEQUENCE IN PICTURE IN PICTURE MODE

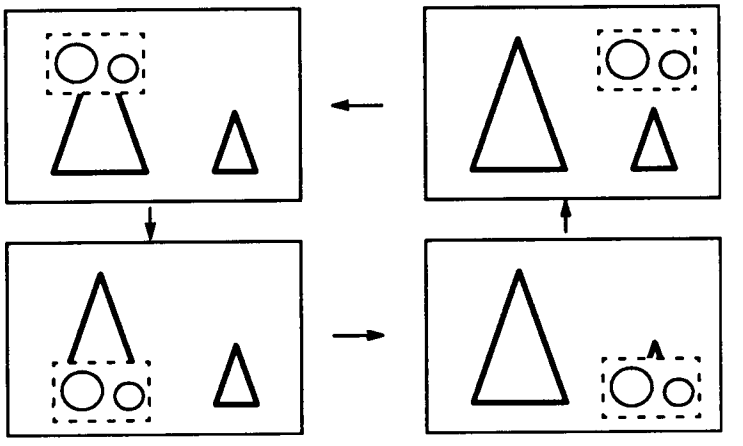
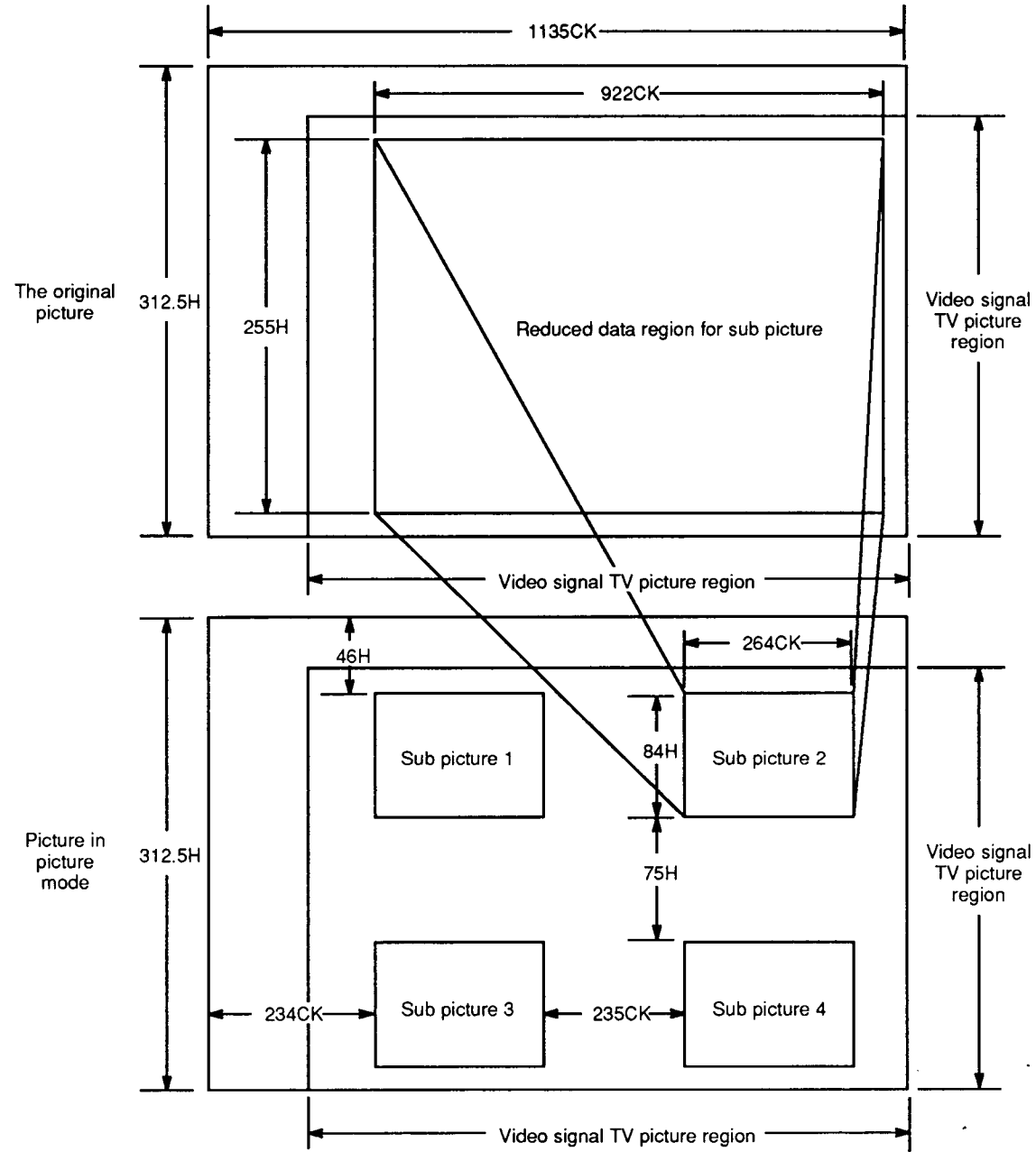


Fig. 4 – SUB PICTURE POSITION IN PIP MODE (CK=4fsc)



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Supply Voltage		V_{DD}	–	4.75	5.00	5.25	V
Operating Temperature		T_A	–	0	–	70	°C
High-level Output Voltage	TTL level	V_{IH}	–	2.2	–	V_{DD}	V
	CMOS level			V_{DD} x 0.7	–	V_{DD}	
Low-level Output Voltage	TTL level	V_{IL}	–	V_{SS}	–	0.8	V
	CMOS level			V_{SS}	–	V_{DD} x 0.3	

INPUT/OUTPUT CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Pin	C_I	f = 1MHz, V_I = V_O = 0V	–	16	–	pF
Output Pin	C_O	f = 1MHz, V_I = V_O = 0V	–	16	–	pF
Input/Output Pin	$C_{I/O}$	f = 1MHz, V_I = V_O = 0V	–	16	–	pF

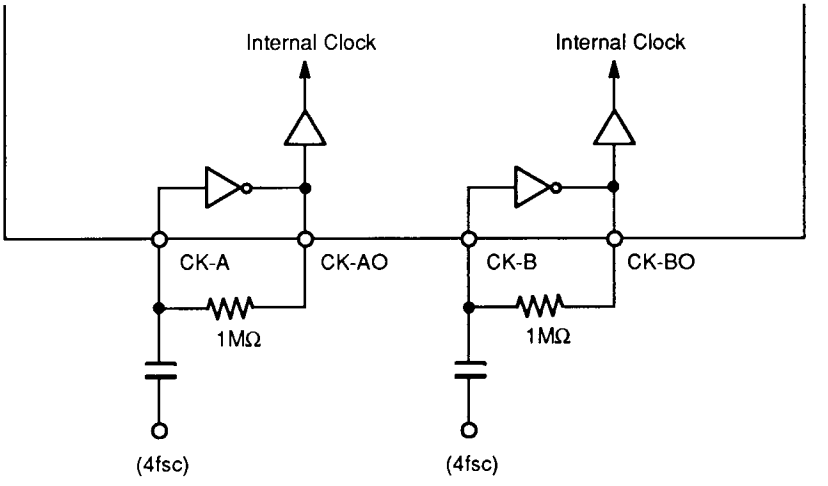
DC CHARACTERISTICS

(V_{DD} = 4.75V~5.25V, V_{SS} = 0V, T_A = 0~70°C)

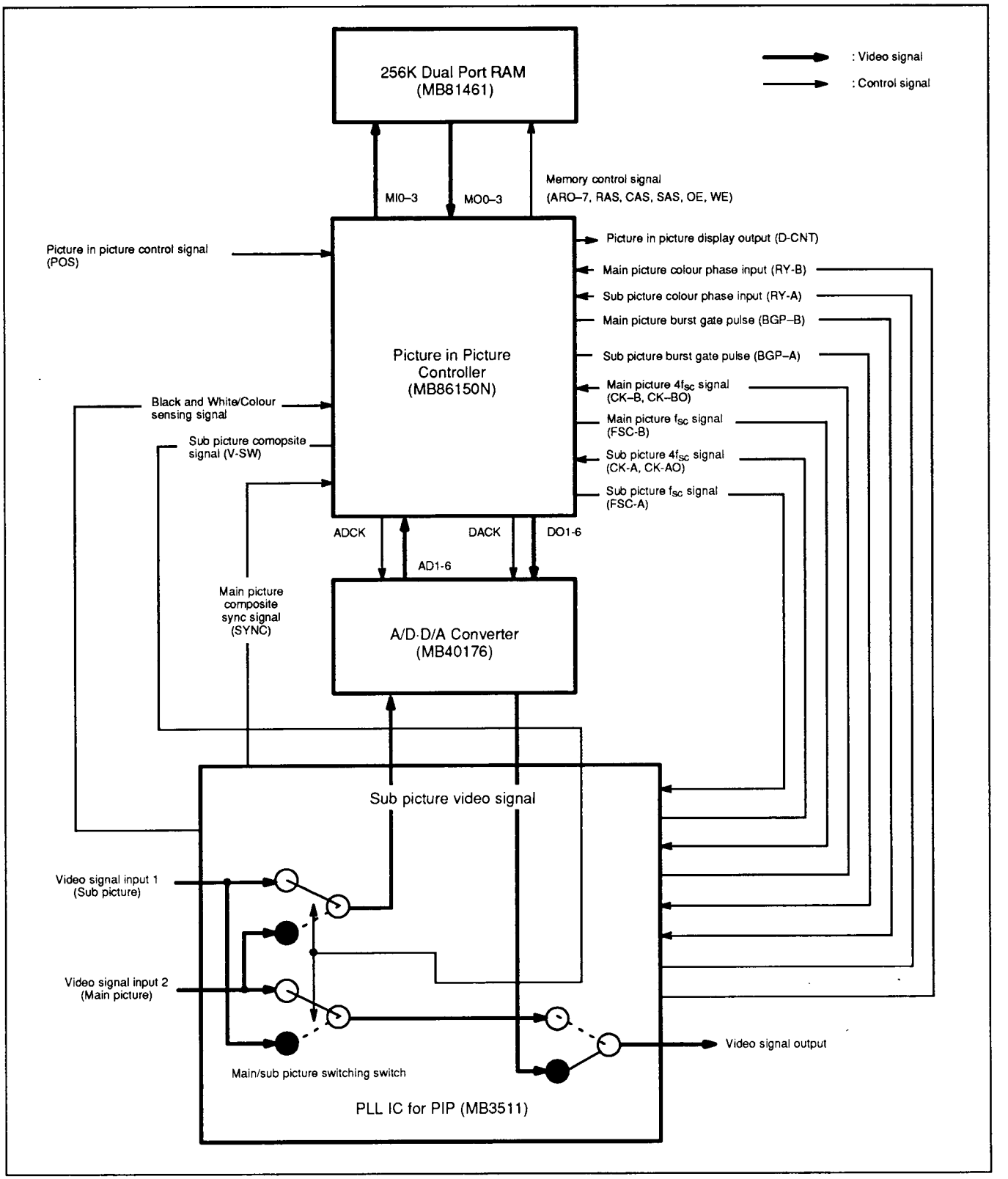
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Supply Current (Stand-by mode)	I_{DDS}	$V_{IH} = V_{DD}$ or $V_{IL} = V_{SS}$	–	–	0.1	mA
High-level Input Voltage	V_{IH}	TTL level	2.2	–	–	V
		CMOS level	V_{DD} x 0.7	–	–	
		Schmitt trigger level *	V_{DD} x 0.8	–	–	
Low-level Input Voltage	V_{IL}	TTL level	V_{SS}	–	0.8	V
		CMOS level	V_{SS}	–	V_{DD} x 0.3	
		Schmitt trigger level *	V_{SS}	–	0.6	
High-level Output Voltage	V_{OH}	I_{OH} = –2.0mA	4.0	–	V_{DD}	V
Low-level Output Voltage	V_{OL}	I_{OL} = 3.2mA (Except SAS pin)	V_{SS}	–	0.4	V
		I_{OL} = 8.0mA (Except pin)				
Input Leakage Current (For tri-state pin)	I_{LI}	V_I = 0V~V_{DD}	–10	–	10	µA
	I_{LZ}		–10	–	10	

Note: *POS pin input condition.

CLOCK INPUT SECTION EQUIVALENT CIRCUIT

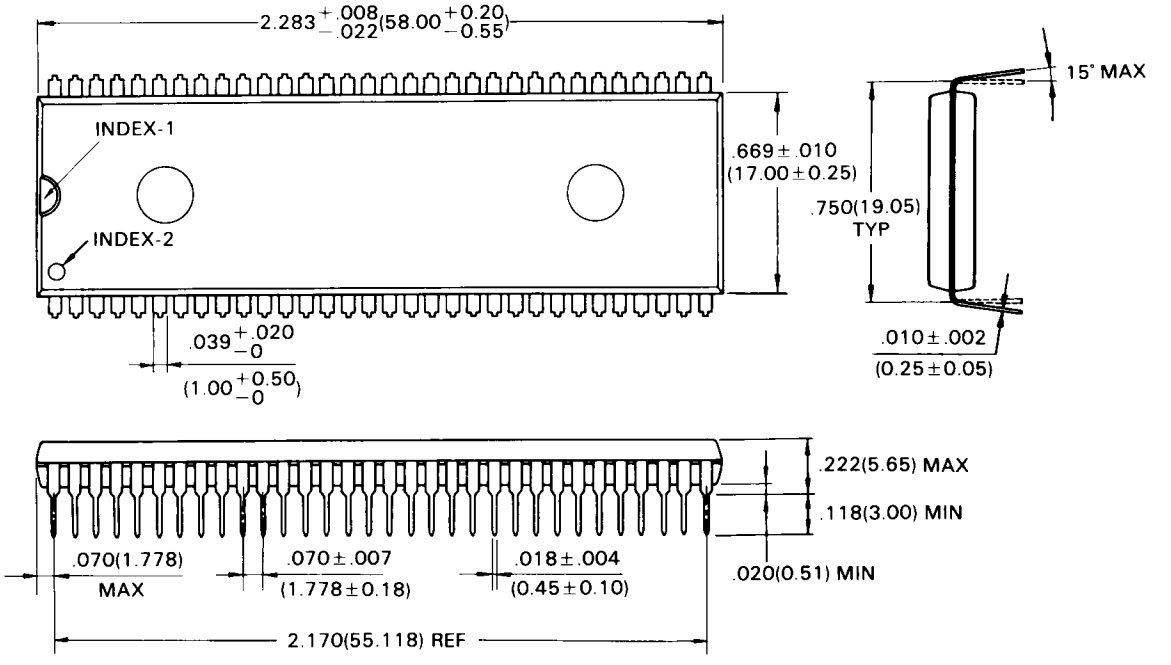


APPLICATION CIRCUIT



PACKAGE DIMENSIONS

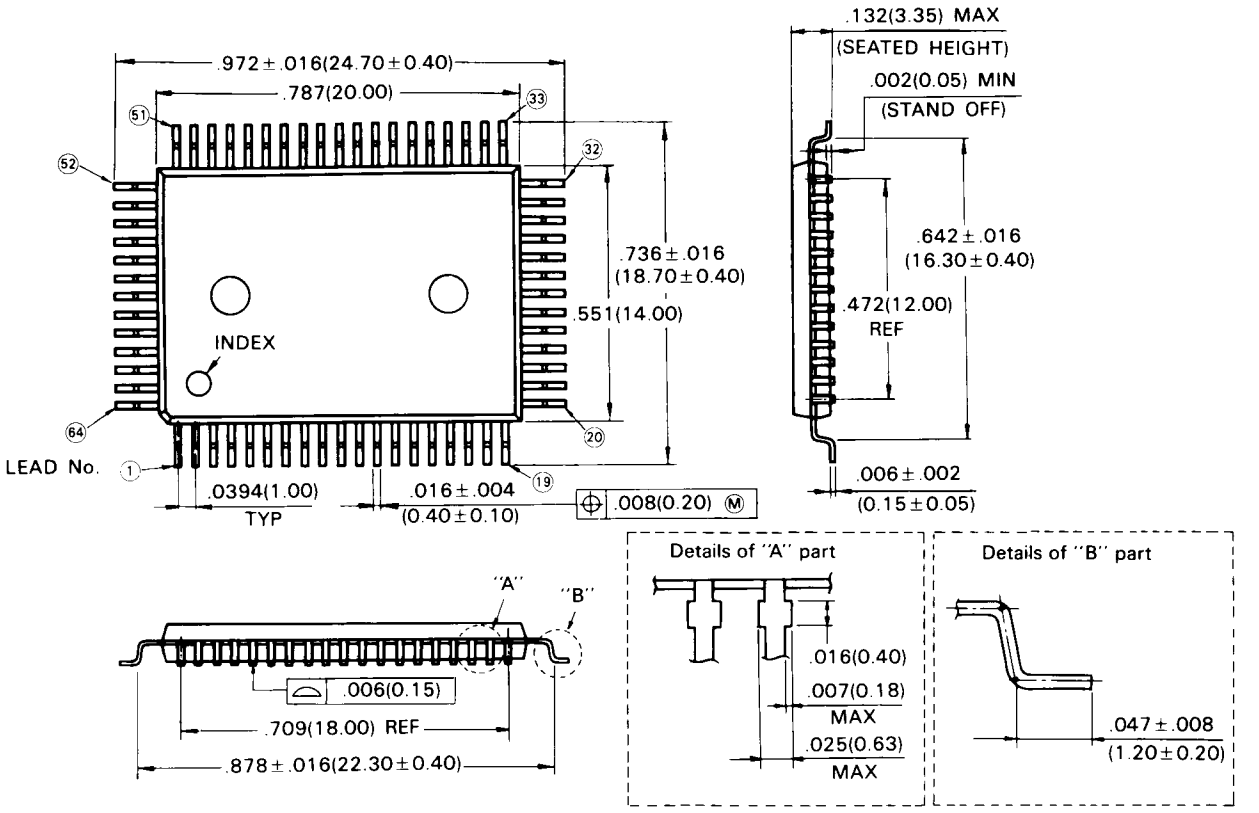
64-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-64P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

64-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-64P-M01)



Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete Information sufficient for construction purposes is not necessarily given.

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