

54F169 Counter

4-Bit Up/Down Binary Synchronous Counter

Military Logic Products

Product Specification

FEATURES

- Synchronous counting and loading
- Up/Down counting
- Modulo 16 binary counter
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Built-in lookahead carry capability
- Presettable for programmable operation

DESCRIPTION

The 54F169 is a synchronous, presettable Modulo 16 up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the Low-to-High transition of the clock.

ORDERING INFORMATION

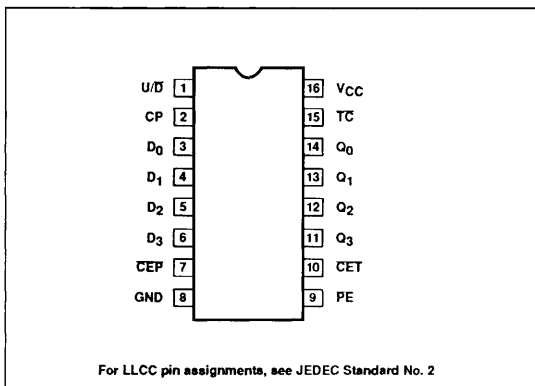
| DESCRIPTION | ORDER CODE |
|-------------------|------------|
| Ceramic DIP | 54F169/BEA |
| Ceramic Flat Pack | 54F169/BFA |
| Ceramic LLCC | 54F169/B2A |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

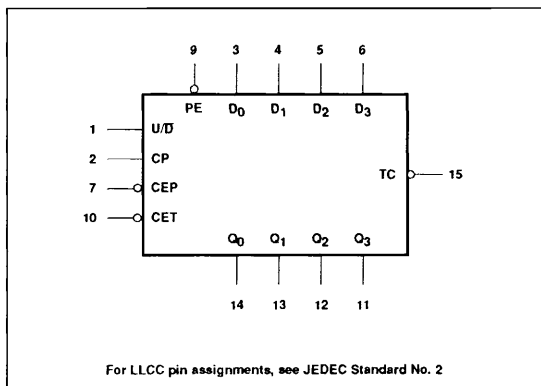
| PINS | DESCRIPTION | 54F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---------------------------------|--|-----------------------|------------------------|
| \overline{CEP} | Count enable parallel input (active Low) | 1.0/1.0 | 20 μ A/0.6mA |
| \overline{CET} | Count enable trickle input (active Low) | 1.0/2.0 | 20 μ A/1.2mA |
| CP | Clock pulse input (active rising edge) | 1.0/1.0 | 20 μ A/0.6mA |
| D ₀ - D ₃ | Parallel data inputs | 1.0/1.0 | 20 μ A/0.6mA |
| PE | Parallel enable input (active Low) | 1.0/1.0 | 20 μ A/0.6mA |
| U/ \overline{D} | Up/down count control input | 1.0/1.0 | 20 μ A/0.6mA |
| Q ₀ - Q ₃ | Flip-flop outputs | 50/33 | 1.0mA/20mA |
| TC | Terminal count output (active Low) | 50/33 | 1.0mA/20mA |

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



LOGIC SYMBOL



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The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable (PE) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

The direction of counting is controlled by the Up/Down (U/D) input; a High will cause the count to increase, a Low will cause the count to decrease.

The carry lookahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (CET·CEP) and a Terminal Count (TC) output. Both Count Enable inputs must be Low to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a Low output pulse with a duration approximately equal to the High level portion of the Q₀ output. This Low level TC pulse is used to enable successive cascaded stages.

See Figure 1 for the fast synchronous multi-stage counting connections.

FUNCTIONAL DESCRIPTION

The 54F169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the Clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When PE is Low, the data on the D₀ - D₃ inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both CEP and CET must be Low and PE must be High; the U/D input then determines the direction of counting. The Terminal Count (TC) output is normally High and goes Low, provided that CET is Low, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The TC output state is not a function of the Count Enable Parallel (CEP) input level. Since the TC signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes

on TC. For this reason the use of TC as a clock signal is not recommended (see logic equations below).

- 1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot PE$
- 2) Up: $TC = Q_0 \cdot Q_3 \cdot (U/D) \cdot \overline{CET}$
- 3) Down: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D) \cdot \overline{CET}$

MODE SELECT TABLE

| PE | CEP | CET | U/D | ACTION ON RISING CLOCK EDGE |
|----|-----|-----|-----|--|
| L | X | X | X | Load (D _n →Q _n) |
| H | L | L | H | Count Up (Increment) |
| H | L | L | L | Count Down (Decrement) |
| H | H | X | X | No Change (Hold) |
| H | X | H | X | No Change (Hold) |

H = High Voltage
 L = Low Voltage Level
 X = Don't care

MODE SELECT — FUNCTION TABLE

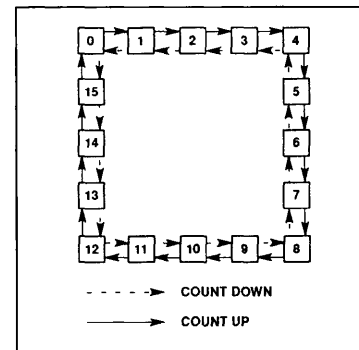
| OPERATING MODE | INPUTS | | | | | | OUTPUTS | |
|-------------------|--------|-----|-----|-----|----|----------------|----------------|-----|
| | CP | U/D | CEP | CET | PE | D _n | Q _n | TC |
| Parallel load | ↑ | X | X | X | l | l | L | (1) |
| | ↑ | X | X | X | l | h | H | (1) |
| Count Up | ↑ | h | l | l | h | X | Count Up | (1) |
| Count Down | ↑ | l | l | l | h | X | Count Down | (1) |
| Hold (do nothing) | ↑ | X | h | X | h | X | q _n | (1) |
| | ↑ | X | X | h | h | X | q _n | H |

H = High voltage level steady state
 h = High voltage level one setup time prior to the Low-to-High clock transition
 L = Low voltage level steady state
 l = Low voltage level one setup time prior to the Low-to-High clock transition
 X = Don't care
 q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
 ↑ = Low-to-High clock transition

NOTE:

1. The TC is Low when CET is Low and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL).

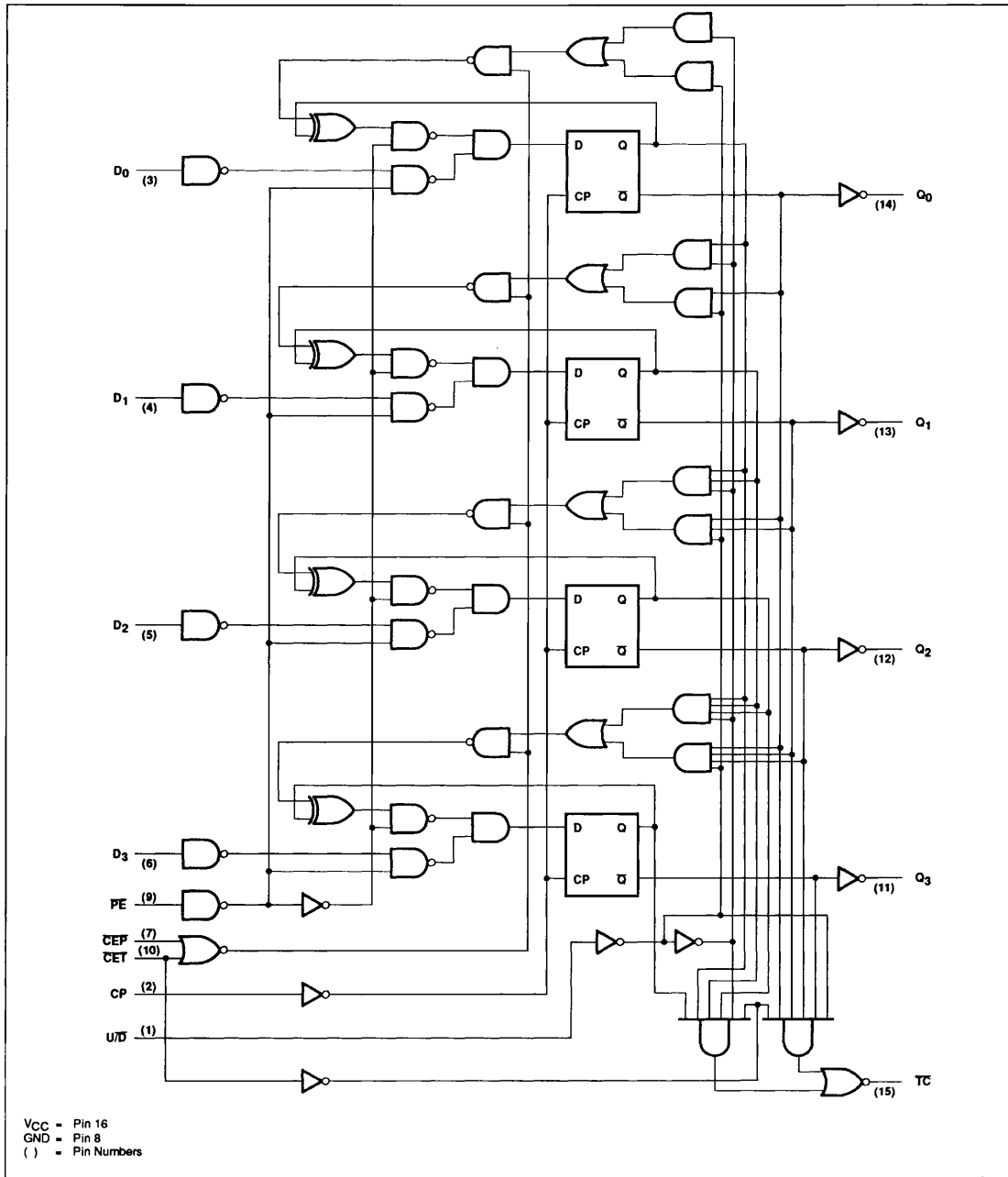
STATE DIAGRAM



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LOGIC DIAGRAM



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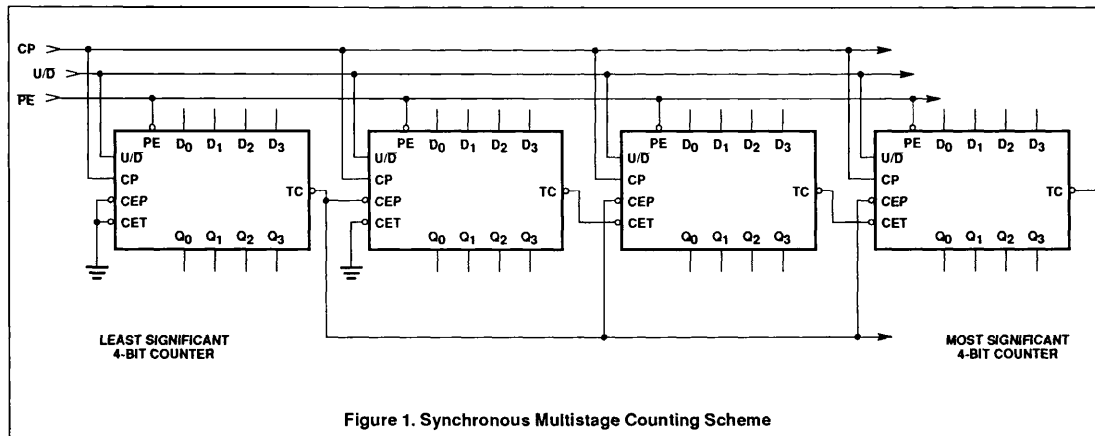


Figure 1. Synchronous Multistage Counting Scheme

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|--|--------------------------|------|
| V _{CC} | Supply voltage range | -0.5 to +7.0 | V |
| V _I | Input voltage range | -0.5 to +7.0 | V |
| I _I | Input current range | -30 to +5 | mA |
| V _O | Voltage applied to output in High output state range | -0.5 to +V _{CC} | V |
| I _O | Current applied to output in Low output state | 40 | mA |
| T _{STG} | Storage temperature range | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------------|--------------------------------------|--------|-----|------|------|
| | | Min | Nom | Max | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{IK} | Input clamp current | | | -18 | mA |
| I _{OH} | High-level output current | | | -1 | mA |
| I _{OL} | Low-level output current | | | 20 | mA |
| T _A | Operating free-air temperature range | -55 | | +125 | °C |

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | LIMITS | | | UNIT |
|------------------|---|---|--------------|------------------|------|------|
| | | | Min | Typ ² | Max | |
| V _{OH} | High-level output voltage | V _{CC} = Min, V _{IL} = Max, V _{IH} = Min, I _{OH} = Max | 2.4 | | | V |
| V _{OL} | Low-level output voltage | V _{CC} = Min, V _{IL} = Max, V _{IH} = Min, I _{OL} = Max | | 0.35 | 0.50 | V |
| V _{IK} | Input clamp voltage | V _{CC} = Min, I _I = I _{IK} | | -0.73 | -1.2 | V |
| I _{IH1} | Input current at maximum input voltage | V _{CC} = Max, V _I = 7.0V | | | 100 | μA |
| I _{IH2} | High-level input current | V _{CC} = Max, V _I = 2.7V | | | 20 | μA |
| I _{IL} | Low-level input current | V _{CC} = Max, V _I = 0.5V | CET input | | -1.2 | mA |
| | | | Other inputs | | -0.6 | mA |
| I _{OS} | Short-circuit output current ³ | V _{CC} = Max | -60 | | -150 | mA |
| I _{CC} | Supply current ⁴ (total) | V _{CC} = Max | | 35 | 52 | mA |

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | | UNIT |
|--------------------------------------|---|-----------------|--|------|------|--|------|----|------|
| | | | T _A = +25°C | | | T _A = -55°C to +125°C | | | |
| | | | V _{CC} = +5.0V | | | V _{CC} = +5.0V ± 10% | | | |
| | | | C _L = 50pF, R _L = 500Ω | | | C _L = 50pF, R _L = 500Ω | | | |
| | | | Min | Typ | Max | Min | Max | | |
| f _{MAX} | Maximum clock frequency | Waveform 1 | 90 | 115 | | 75 | | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CP to Q _n (PE, High or Low) | Waveform 1 | 3.0 | 6.5 | 8.5 | 3.0 | 9.5 | ns | |
| | | | 4.0 | 9.0 | 11.5 | 4.0 | 13.0 | | |
| t _{PLH} t _{PHL} | Propagation delay CP to TC | Waveform 1 | 5.5 | 12.0 | 15.5 | 5.5 | 18.0 | ns | |
| | | | 4.0 | 8.5 | 11.0 | 4.0 | 12.5 | | |
| t _{PLH} t _{PHL} | Propagation delay CET to TC | Waveform 2 | 2.5 | 4.5 | 6.0 | 2.5 | 7.0 | ns | |
| | | | 2.5 | 6.0 | 8.0 | 2.5 | 9.0 | | |
| t _{PLH} t _{PHL} | Propagation delay U/D to TC | Waveform 3 | 3.5 | 8.5 | 12.0 | 3.5 | 16.5 | ns | |
| | | | 4.0 | 8.0 | 10.5 | 4.0 | 13.0 | | |

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AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|------------------------------------|--|-----------------|--|-----|-----|--|-----|----------|
| | | | $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}, R_L = 500\Omega$ | | | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$ | | |
| | | | Min | Typ | Max | Min | Max | |
| $t_s(\text{H})$ $t_s(\text{L})$ | Setup time, High or Low D_n to CP | Waveform 4 | 4.0 4.0 | | | 4.5 4.5 | | ns ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, High or Low D_n to CP | Waveform 4 | 3.0 3.0 | | | 3.5 3.5 | | ns ns |
| $t_s(\text{H})$ $t_s(\text{L})$ | Set-up time, High or Low $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP | Waveform 5 | 5.0 5.0 | | | 5.5 5.5 | | ns ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, High or Low $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP | Waveform 5 | 0 0 | | | 0 0 | | ns ns |
| $t_s(\text{H})$ $t_s(\text{L})$ | Set-up time, High or Low PE to CP | Waveform 4 | 8.0 8.0 | | | 9.0 9.0 | | ns ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, High or Low PE to CP | Waveform 4 | 0 0 | | | 0 0 | | ns ns |
| $t_s(\text{H})$ $t_s(\text{L})$ | Set-up time, High or Low U/D to CP | Waveform 6 | 11.0 7.0 | | | 12.5 8.0 | | ns ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, High or Low U/D to CP | Waveform 6 | 0 0 | | | 0 0 | | ns ns |
| $t_w(\text{H})$ $t_w(\text{L})$ | CP pulse width High or Low | Waveform 1 | 5.0 5.0 | | | 5.5 5.5 | | ns ns |

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after applying a momentary $\geq 4.0\text{V}$, then ground to the clock input with all other inputs grounded and outputs open.

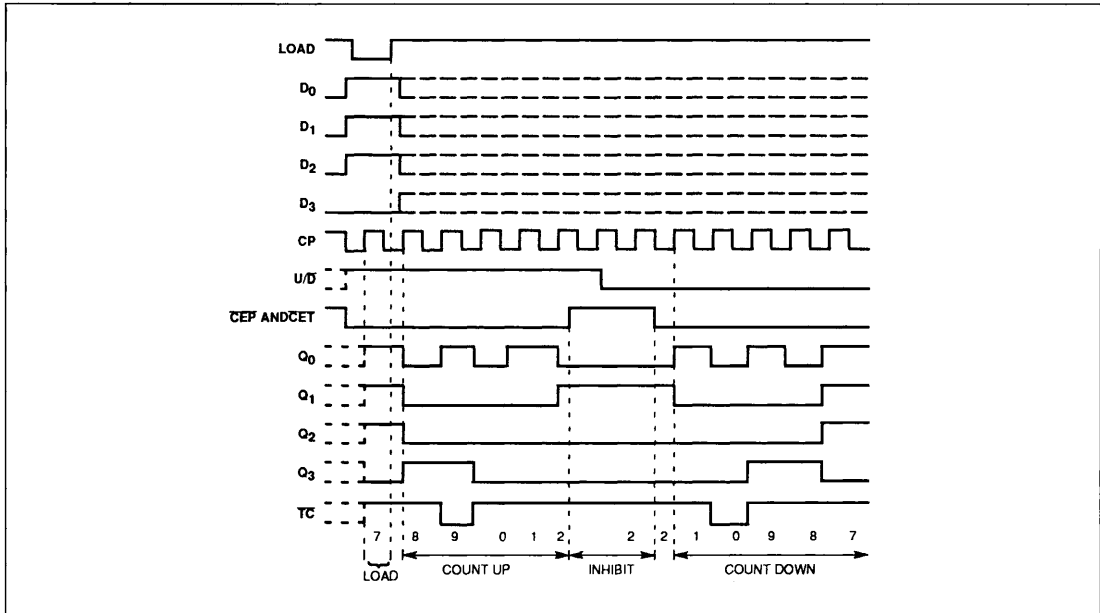
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WAVEFORM (Typical Load, Count, and Inhibit Sequences)

Illustrated below is the following sequence for the 54F168. The operation of the 54F169 is similar.

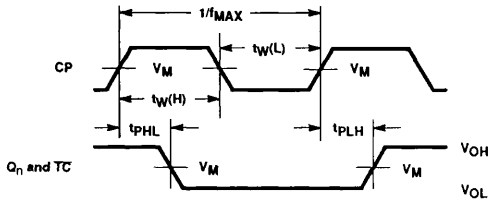
1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



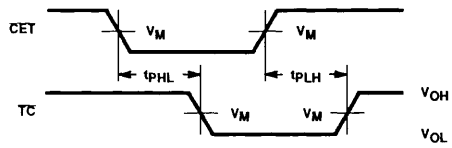
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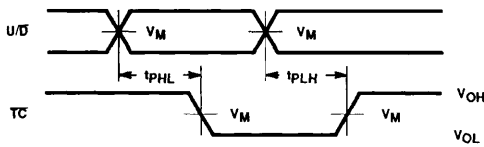
AC WAVEFORMS



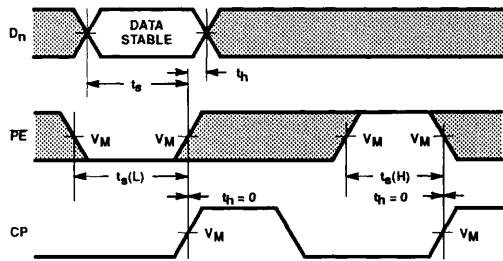
Waveform 1. Clock to Output Delays and Clock Pulse Width



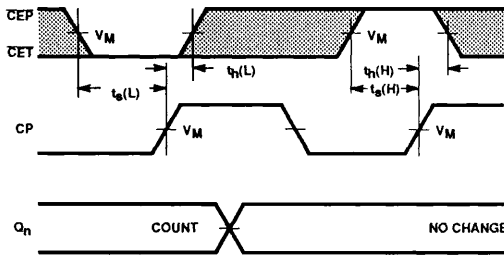
Waveform 2. Propagation Delays CET Input to Terminal Count Output



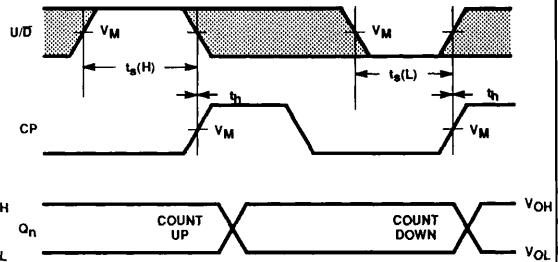
Waveform 3. Propagation Delays U/D Control to Terminal Count Output



Waveform 4. Parallel Data and Parallel Enable Set-up and Hold Times



Waveform 5. Count Enable Set-Up and Hold Times



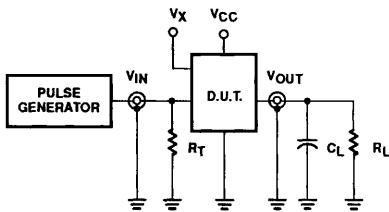
Waveform 6. Up/Down Control Set-Up and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance.

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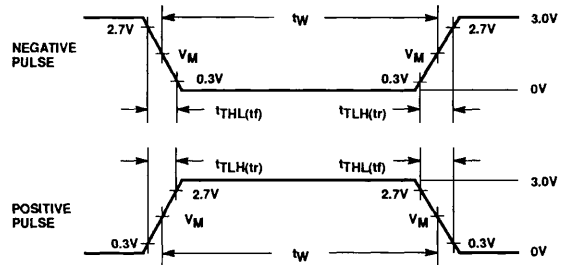
TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs

DEFINITIONS:

- R_L = Load Resistor; see AC Characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- V_X = Unlocked pins must be held at: $\leq 0.8V$; $\geq 2.7V$ or open per Function Table.



$V_M = 1.5V$

Input Pulse Definition

| INPUT PULSE CHARACTERISTICS | | | | |
|-----------------------------|-----------|-------------|--------------|--------------|
| Family | Rep. Rate | Pulse Width | t_{TLH} | t_{THL} |
| 54F | 1MHz | 500ns | $\leq 2.5ns$ | $\leq 2.5ns$ |