Overview

Features

- High Performance:

CAS latency = 2		-6	-7.5	-10	Units
f_{CK}	Clock Frequency	166	133	100	MHz
t_{CK2}	Clock Cycle	6	7.5	10	ns
t_{AC2}	Clock Access Time	4.3	4.5	5	ns

- 8Kbit SRAM Row Cache
- Supports Row Pipelining for Random Row Reads of 4:1:1:1:2:1:1:1:2:1:1:1 @ 133MHz
- Compatible with JEDEC Standard SDRAMs
- JEDEC Superset Standard ESDRAM
- Programmable Caching Policy
- Programmable CAS Latency: 1, 2, 3
- Dual Banks controlled by A11 (Bank Select)
- Programmable Burst Length: 1,2,4,8,full-page
- Programmable Wrap Sequence, Sequential or Interleaved
- Automatic and Controlled Precharge Command
- Hidden Precharge and Hidden Auto Refresh
- Self Refresh
- Suspend Mode and Power Down Mode
- 2048 refresh cycles / 64ms
- Single 3.3V ± 0.3V Power Supply
- LVTTL and 2.5V I/O Interface with Flexible V_{DDQ}
- Package: 44 pin 400 mil TSOP-Type II (x4,x8)
  50 pin 400 mil TSOP-Type II (x16)

Description

As a JEDEC superset standard, the Enhanced Synchronous DRAM is an evolutionary modification to a JEDEC standard 16Mbit Synchronous DRAM. The ESDRAM incorporates changes to a standard SDRAM which reduce the latency, increase the bandwidth, and allow for concurrent operations to the same bank. Even with these improvements in performance and functionality, the Enhanced SDRAM remains pin and command compatible with a JEDEC standard 16Mbit SDRAM. As a result, the ESDRAM is plug-compatible with an SDRAM and operates like a standard SDRAM when used in an SDRAM application.

The 16Mbit Enhanced Synchronous DRAM combines a fast DRAM array with an 8Kbit SRAM cache. The DRAM array is separated into two fully independent 8Mbit DRAM banks with 4Kbits of SRAM cache per bank. The SRAM cache is integrated into the DRAM array as tightly coupled row registers. The integrated cache provides several advantages. The first advantage is high speed random column accesses (<12ns). Another advantage is that through the use of auto-precharge, the cache allows the user to perform operations on the DRAM array concurrent with cache reads. These operations include new row activation, precharge, and refreshing the DRAM array. Since new row activations can occur during cache read cycles, it is possible for the ESDRAM to pipeline random row reads, thus reducing the page miss latency to that of a page hit.

This device is designed to comply with all JEDEC standards set for SDRAM products, both electrically and mechanically. All the control, address, and data input/output circuits are synchronized with the positive edge of an externally supplied clock.

Prior to any access operation, the CAS latency, burst length, burst sequence, and write caching policy must be programmed into the device by address inputs A0-A11 during a Mode Register Set command cycle. The write policy is set as either Write Transfer mode or No Write Transfer mode.

This device supports Self Refresh mode and operates with a single 3.3V ± 0.3V power supply. The device is available in a 400mil TSOP Type II package.

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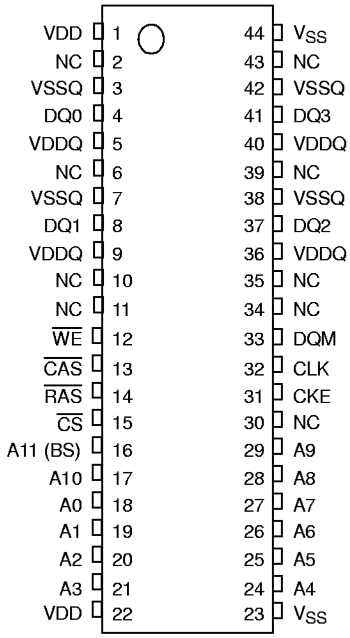
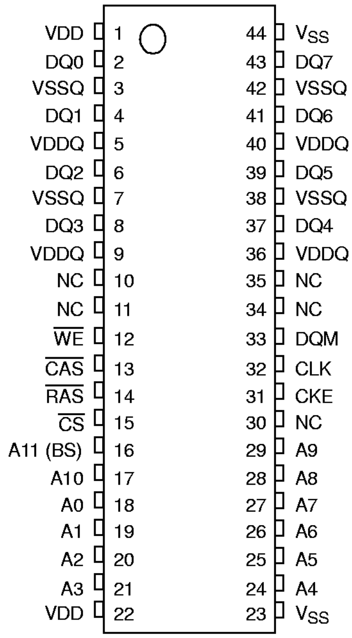
Pin Assignments (Top View)



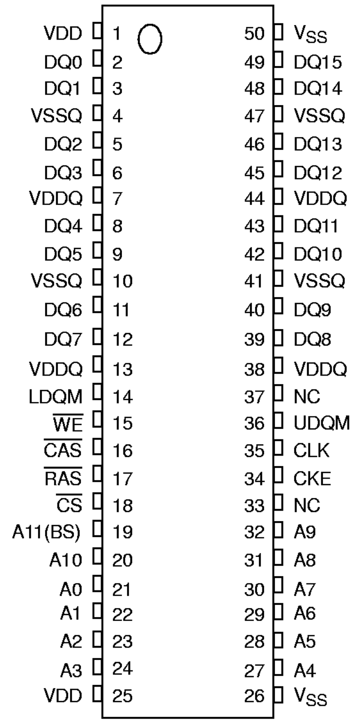
44-pin Plastic TSOP(II) 400 mil

2Mbit x 4 I/O x 2 Bank (4M x 4)



44-pin Plastic TSOP(II) 400 mil

1Mbit x 8 I/O x 2 Bank (2M x 8)



50-pin Plastic TSOP(II) 400 mil

512Kbit x 16 I/O x 2 Bank (1M x 16)

Pin Description

CLK	Clock Input	**DQ0-DQ15**	Data Input/Output
CKE	Clock Enable	**DQM, LDQM, UDQM**	Data Mask
$\overline{\text{CS}}$	Chip Select	**VDD**	Power (+3.3V)
$\overline{\text{RAS}}$	Row Address Strobe	**VSS ***	Ground
$\overline{\text{CAS}}$	Column Address Strobe	**VDDQ**	Power for DQ's (+3.3V or +2.5V)
$\overline{\text{WE}}$	Write Enable	**VSSQ ***	Ground for DQ's
A11 (BS)	Bank Select	—	—
A0 - A10	Address Inputs	**NC**	No Connection

* VSS and VSSQ are connected internally in the chip.

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Functional Pin Description

Symbol	Type	Function
CLK	Input	The system clock input. All of the ESDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	When sampled, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ define the operation executed by the SDRAM.
A11 (BS)	Input	Selects which bank is to be active. A11 low selects bank A and A11 high selects bank B.
A0 - A10	Input	During a Bank Activate command cycle, A0-A10 defines the row address (RA0-RA10). During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, A10 is used to invoke autoprecharge operation during a burst read cycle or at the end of a burst write cycle. If A10 is high, autoprecharge is selected and A11 defines the bank to precharge (low=bank A, high=bank B). If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 is used in conjunction with A11 to control which bank(s) to precharge. If A10 is high, both bank A and bank B are precharged regardless of the state of A11. If A10 is low, then A11 is used to define which bank to precharge.
DQ0 - DQ15	Input Output	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQM LDQM UDQM	Input	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing the write operation if DQM is low, but blocking the write operation if DQM is high.
VDD	Supply	Power for the input buffers and the core logic. Connect to 3.3V power supply.
VDDQ	Supply	Power for the output buffers. Connect to 3.3V or 2.5V power supply.
VSS, VSSQ	Supply	Ground for the chip. VSS and VSSQ are connected inside the chip.

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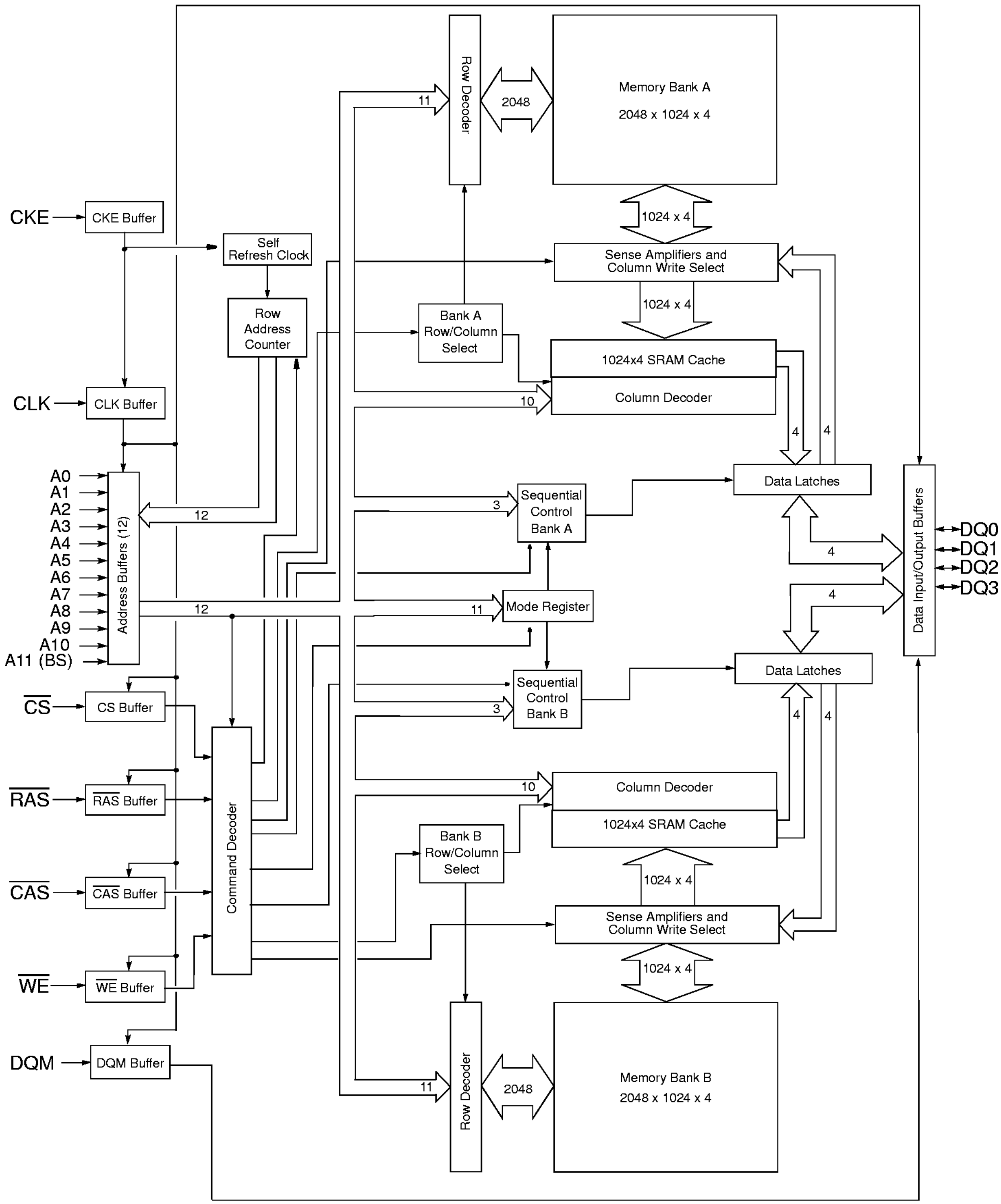
Block Diagram (2Mbit x 4 I/O x 2 Bank)



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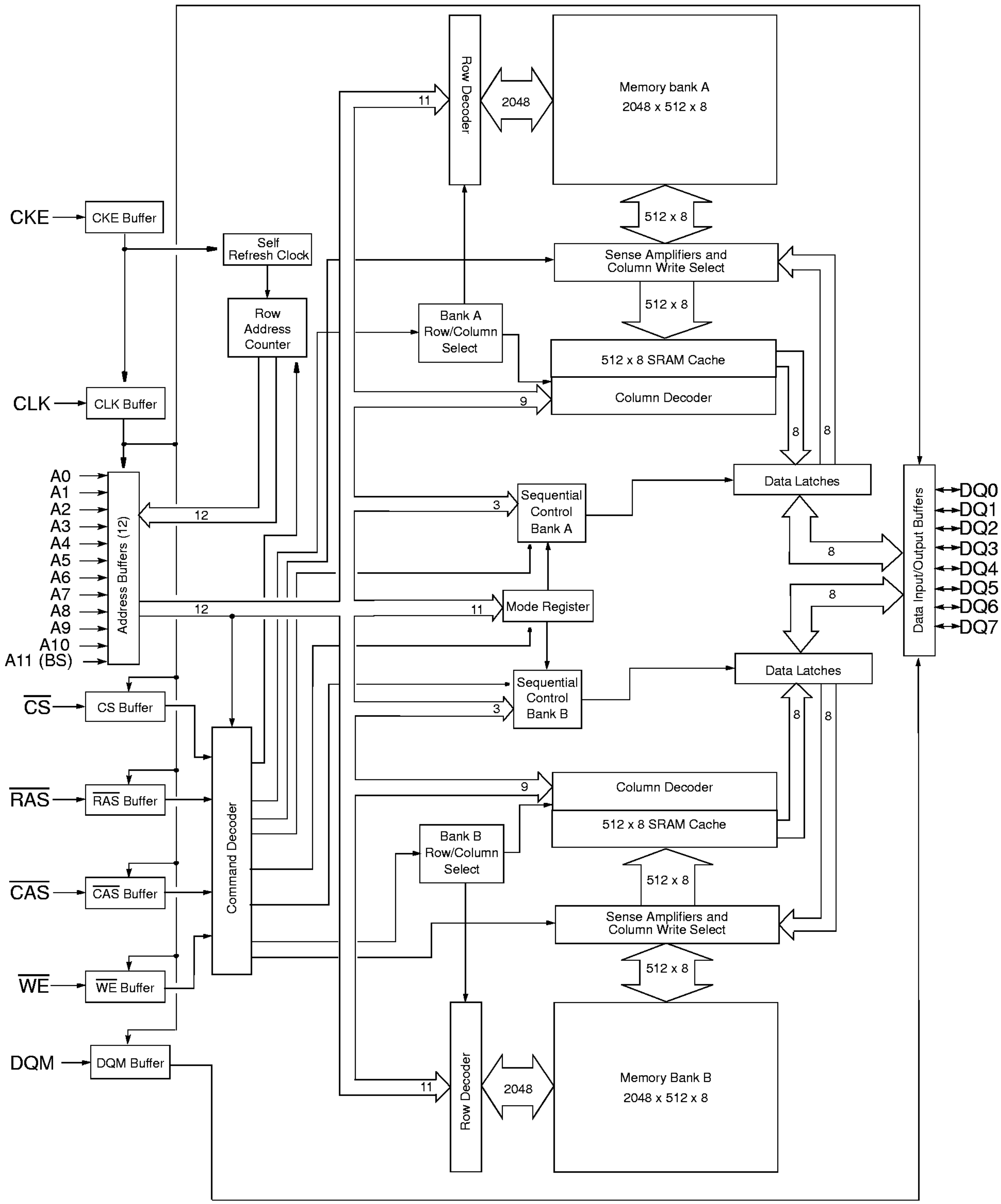
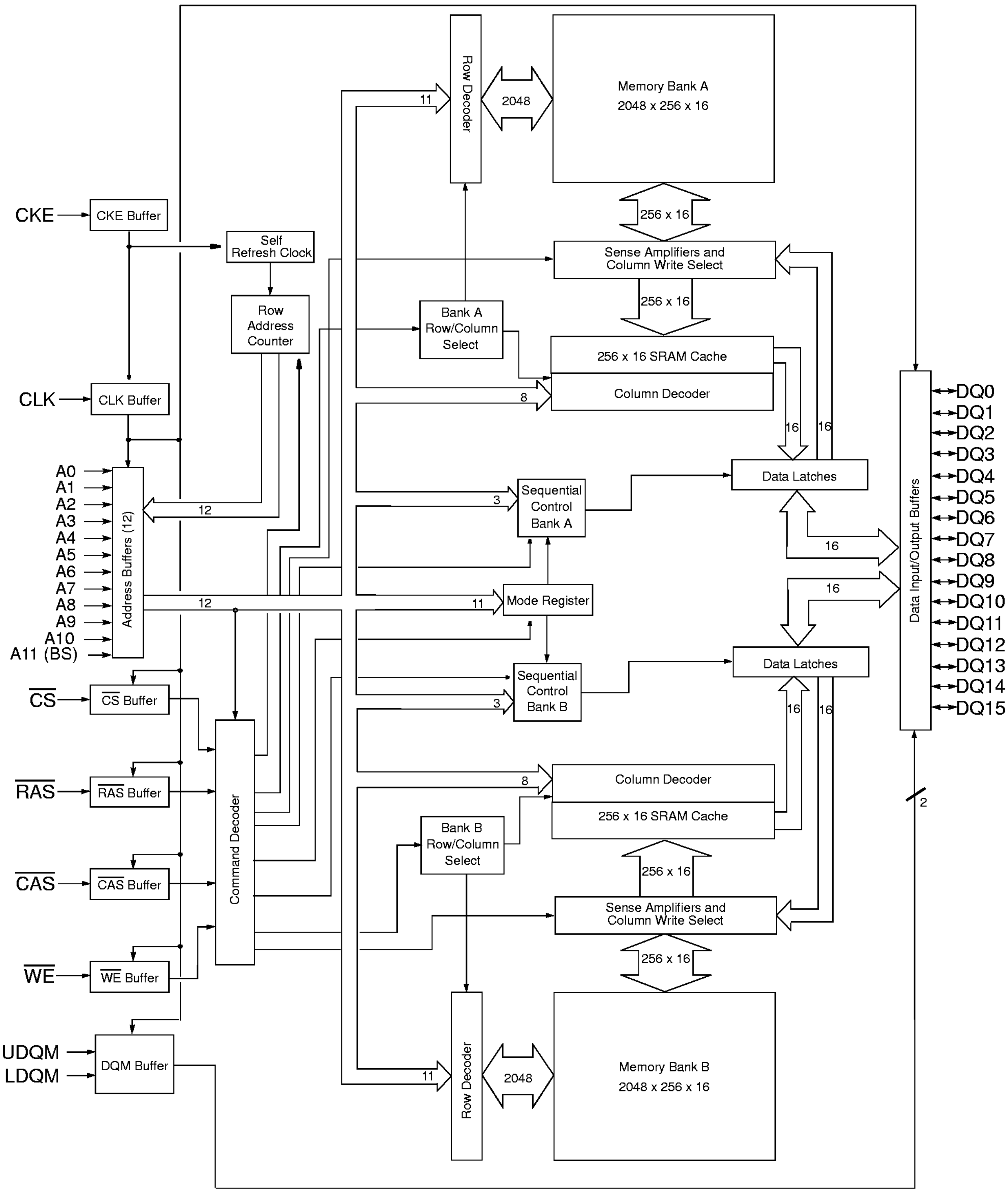
Block Diagram (1Mbit x 8 I/O x 2 Bank)



Block Diagram (512Kbit x 16 I/O x 2 Bank)



Device Operation

The 16Mbit Enhanced Synchronous DRAM is an evolutionary modification to a JEDEC standard 16Mbit Synchronous DRAM. Now ESDRAM is also a JEDEC superset of the SDRAM standard. The ESDRAM resolves some performance issues not addressed by standard SDRAMs. Standard Synchronous DRAMs are designed for flexibility through programmability and provide higher burst rates than asynchronous DRAMs. Unfortunately, a standard SDRAM does not improve the initial latency of a page hit or miss, and it does not reduce the penalties caused by the DRAM cycle time (t_{RC}) and the DRAM precharge time (t_{RP}). With two banks, a standard SDRAM does allow the user to perform simultaneous operations on both banks in order to hide some of the precharge and cycle time delays. However, this feature is useful only if the data being stored is orderly and can be organized such that the SDRAM can ping-pong between the two open banks without interruption. With today's multi-tasking computer operating systems, this is a formidable task.

The 16Mbit Enhanced SDRAM uses two architectural modifications to improve upon a standard SDRAM. The first of these changes is the design of a fast DRAM array (t_{RAC} = 22ns). The fast array reduces the initial latency of page misses, and the precharge and cycle times. The second modification consists of integrating a 4Kbit high speed SRAM cache into each bank of the DRAM array. This cache consists of tightly coupled row registers which hold one page (row) of data. The addition of the cache provides several performance advantages. The first of these advantages is a high speed (<12ns) random column access time. Secondly, since the row data is loaded into the cache, the DRAM array is available for auto-precharge and refresh or re-activate concurrent with page hit reads from the cache. Finally, because the DRAM can be re-activated during cache reads, the system has the ability to pipeline random row reads to the same bank. This allows the system to start the next row access on a page miss while bursting out data from the previous access, thus reducing the page miss latency to that of a page hit.

To summarize, the ESDRAM functions like a standard 16Mbit SDRAM while solving some of the performance limitations of a standard SDRAM. The ESDRAM improves the latency of a standard SDRAM by reducing RAS latency, CAS latency, and precharge and bank cycle times. In addition, the ESDRAM increases memory performance by supporting concurrent operations on the same bank, which allows the user to pipeline accesses and overlap commands. With these changes the ESDRAM can deliver more that twice the memory performance of standard SDRAM at the same clock frequency (See "SDRAM vs. ESDRAM" figure on page 15). In conclusion, the design of the ESDRAM enables the user to more fully utilize the memory bandwidth and eliminate system wait states for all memory accesses.

ESDRAM Cache Architecture

The 16Mbit Enhanced SDRAM uses two architectural modifications to improve upon a standard SDRAM. The first of these changes is the design of a fast DRAM array (t_{RAC} = 22ns). The fast array reduces the initial latency of page misses, and reduces the precharge and cycle times of the DRAM. The second modification consists of integrating an 8Kbit high speed SRAM cache into the DRAM array.

The 8Kbit integrated cache on the ESDRAM consists of a 4Kbit integrated row register for each DRAM bank. When a row in one of the DRAM banks is activated, the row data is latched by the sense amplifiers but does not get transferred into the cache. This allows refreshing the DRAM array, or initiating a new row access, without modifying the current contents of the cache. However, when a Read command occurs after a new row is activated, the entire row is automatically transferred into the cache where it is then read from the chip within the specified CAS latency. All Read commands retrieve data from the SRAM cache and do not access the DRAM array.

If a Write command occurs after a new row activate, the Mode register is used to determine whether or not the sense amplifiers are loaded into the cache. If the Mode register indicates that the part is in Write Transfer mode, the Write command transfers the sense amplifier data into the cache. If the Mode register indicates that the part is in No Write Transfer mode, the Write command does not transfer the sense amplifier data into the cache.

Note: If a write hit occurs (the write page is already in the cache) the ESDRAM automatically updates the cache when the data is written to the DRAM array, regardless of the Write Transfer mode setting.

The row data from the DRAM sense amplifiers is transferred into the cache only on the first Read or Write (Write Transfer mode) command occurring after a Bank Activate command. Any subsequent Read or Write commands to the same row do not load the cache.

Write Transfer Mode versus No Write Transfer Mode

For maximum flexibility, the ESDRAM incorporates a programmable caching policy. This feature allows the user to optimize the ESDRAM's cache for a particular application, to achieve increased memory performance and compatibility. The Mode register is used to select either Write Transfer mode or No Write Transfer mode.

Write Transfer Mode

If the ESDRAM is in Write Transfer (normal) mode, a write miss activates a new row which is transferred into the cache, overwriting any previous information stored there. Since read operations always load the cache, the row data in the DRAM sense amplifiers always equals the cache data after the Read or Write command is given. Therefore, in Write Transfer mode, only one DRAM/cache row per bank is available for reading or writing (not true in No Write Transfer mode). The following is a detailed discussion of Write Transfer mode which refers to the "Write Transfer Mode" figure below.

When a read miss occurs, a Bank Activate command must be issued for the new row. After a time t_{RCD}, a Read or Read with Auto Precharge command can be given to the ESDRAM in order to access data from the new row. When the Read command is issued at time T0, data from row X is transferred into the cache on the same clock cycle. If the auto precharge function is invoked, the DRAM precharge is started on the clock cycle following the Read command. Two clock cycles later, the DRAM bank is closed or precharged and a new row Y from the same bank can be activated (clock T3). When the Write command is issued at time T5, the ESDRAM transfers sense amplifier data (row Y) into the cache and the DRAM bank. At this point both the DRAM sense amplifiers and the cache are holding the same information (row Y). Any subsequent Read command reads row Y data from the cache (see T7-T9).

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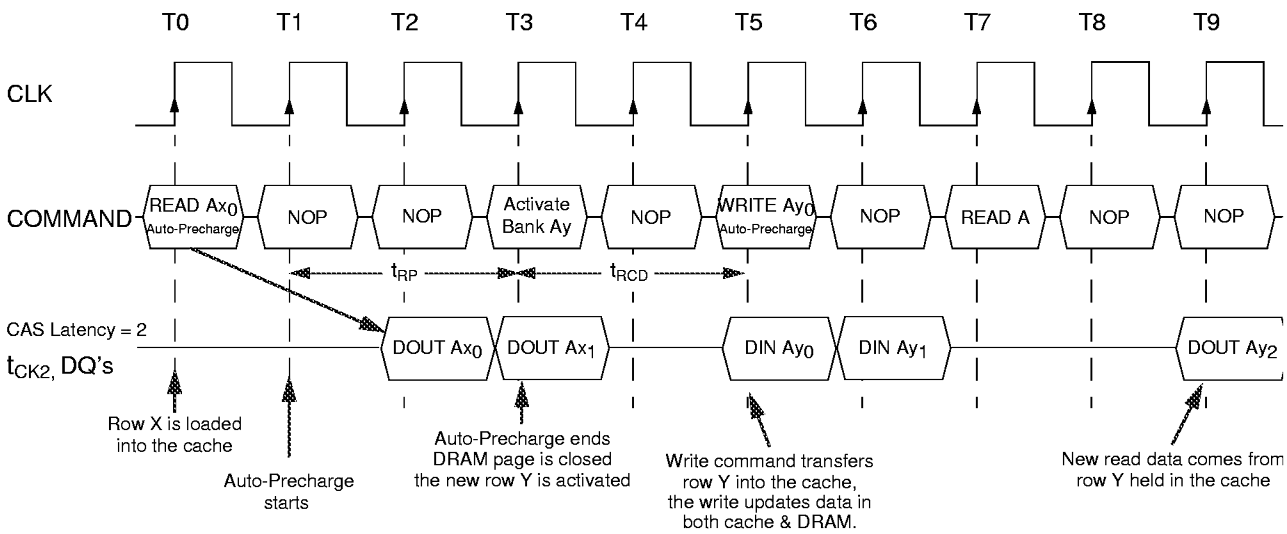
Write Transfer Mode (Burst Length = 2)



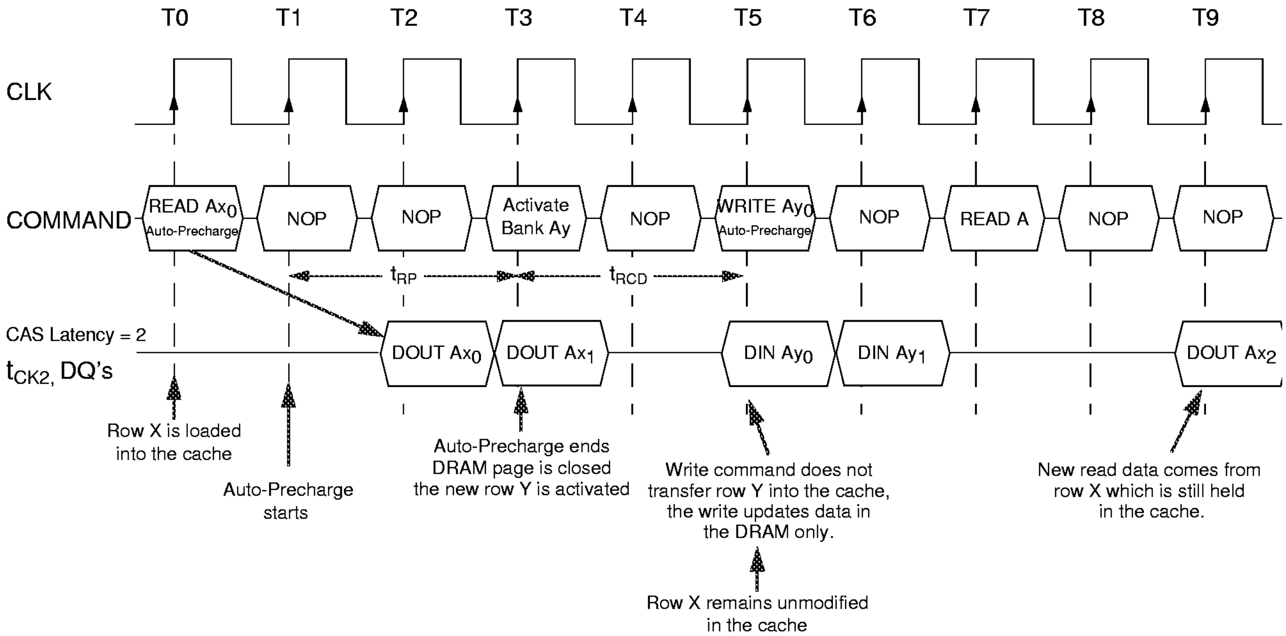
Since the DRAM sense amplifiers and the cache always hold the same row after a Read or Write command is issued, a memory controller requires only one page tag per bank of the ESDRAM. This is the same number of page tags per bank required for a standard SDRAM. In addition, the control of the DRAM/cache bank is identical to the control of a standard SDRAM's DRAM bank. For further compatibility with SDRAM, the binary code of the Write Transfer mode corresponds to the code for the normal operation mode of a standard SDRAM. These features help make the ESDRAM 100% compatible with an SDRAM, allowing the ESDRAM to replace a standard SDRAM without making any modifications to the memory controller and system.

No Write Transfer Mode

If the ESDRAM is placed in No Write Transfer mode, a write miss does not transfer the new row to the cache. Instead, the new row is updated in the DRAM sense amplifiers leaving the cache contents unaffected. This allows the ESDRAM to have a read page and a write page open simultaneously in the same bank. The following is a detailed discussion of No Write Transfer mode which refers to the "No Write Transfer Mode" figure below.

When a read miss occurs, a Bank Activate command must be issued to activate the new row. After a time t_{RCD}, a Read command can access data from the new row. When the Read command is issued at time T0, data from row X is transferred into the cache on the same clock cycle. If the auto precharge function is invoked, the DRAM precharge is started on the clock cycle following the Read command. Two clock cycles later, the DRAM bank is closed and the new row Y can be activated. When the Write command is issued at time T5, the ESDRAM does not load the row Y into the cache. Instead, the write data is used to update the DRAM sense amplifiers and the DRAM bank, but the cache remains unaffected. At this point there are two rows (row X and row Y) open from which column reads/writes can occur. Now any subsequent Read command reads column data from row X in the cache (see T7-T9) and any subsequent Write command writes data to row Y in the DRAM. Data cannot be read from row Y unless the DRAM is precharged and row Y is reactivated and followed by a Read command. Data cannot be written to row X unless the DRAM is precharged and row X is reactivated, followed by a Write command.

No Write Transfer Mode (Burst Length = 2)



This setup is ideal for a system that reads data from one page of memory, processes the data, and then writes the results back to a different page of the memory. In this case the ESDRAM can have both the read page and the write page open simultaneously in the same bank. Note that if fast read/write cycles are desired, the memory controller must issue Read (not Read with Auto-Precharge) commands. A Read AP command closes the write page in No Write Transfer mode. Additionally, any application in which data copy or data move operations occur frequently should see a performance benefit from using the No Write Transfer mode of the ESDRAM.

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ESDRAM Performance Advantages

The ESDRAM architecture improves system performance by reducing the latency of the memory in addition to allowing the system to perform concurrent operations on the same bank of DRAM memory.

Reduced Latency

The core of the ESDRAM consists of a high speed (t_{RAC} = 22ns) DRAM array. This fast array enables the ESDRAM to reduce the precharge time (t_{RP}) and the bank cycle time (t_{RC}). Since reads always access the cache and write data is buffered, the ESDRAM is able to perform random column accesses at SRAM speeds. The latency improvements over SDRAM resulting from these advantages are shown in the Table below.

ESDRAM (-7.5) and SDRAM (-8) Latency with a 133MHz Clock Frequency

Parameter	Description	ESDRAM	SDRAM	Units
t_{AC}	Access Time From Clock (Max)	4.5	6	ns
t_{AA}	Column Access Time (Max)	2	3	Clock Cycles
t_{RAC}	Row Access Time (Max)	4	6	Clock Cycles
t_{RP}	Row Precharge Time (Max)	2	3	Clock Cycles
t_{RAS}	Row Active Time (Min)	3	8	Clock Cycles
t_{RC}	Bank Cycle Time (Min)	5	11	Clock Cycles

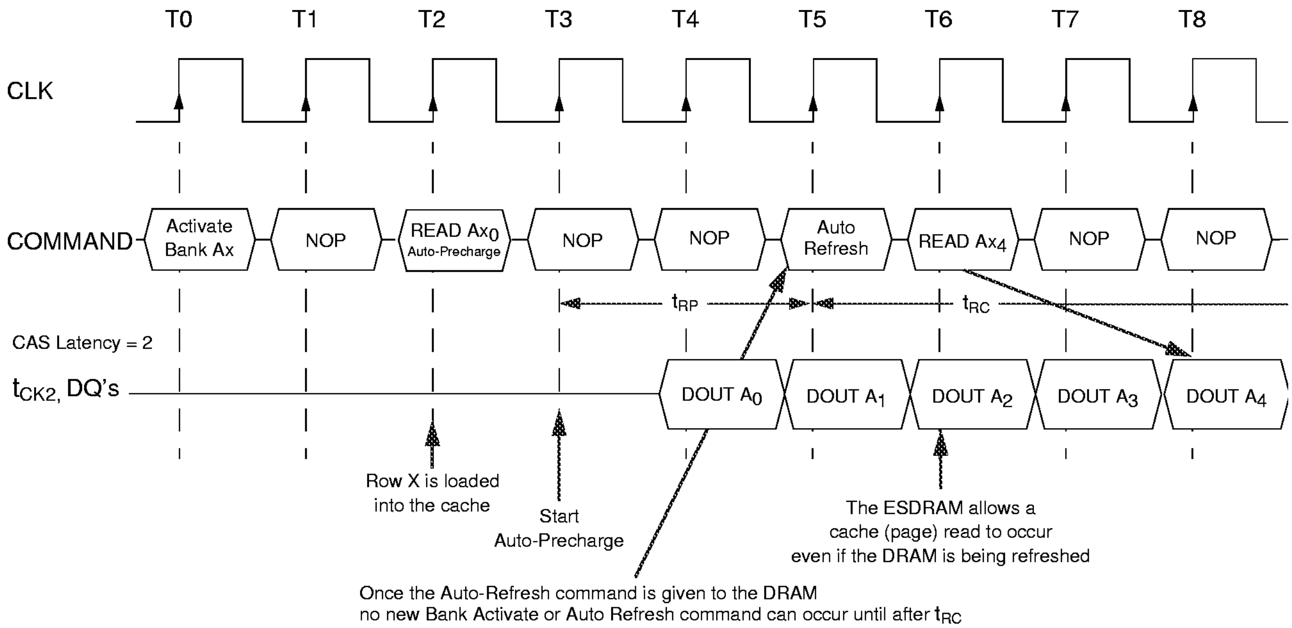
Concurrent Operations and Row Pipelining

Using the row cache, the ESDRAM is able to perform concurrent operations to the same bank, a feature that is unavailable on a standard SDRAM. This ability to perform concurrent operations provides a significant increase in the performance of the memory, in some instances it can effectively double the memory's bandwidth over that of a standard SDRAM. The following is a discussion on which concurrent operations are allowed and how they can be used to maximize memory performance and minimize system wait states.

When a Bank Activate command is given to the ESDRAM, the row is selected in memory and the data is latched by the sense amplifiers. At this point the contents of the cache remain unchanged. When a Read command is issued, the entire selected row is transferred into the cache within one clock cycle and the first read data appears on the outputs within one, two, or three clock cycles (as a function of CAS latency programmed).

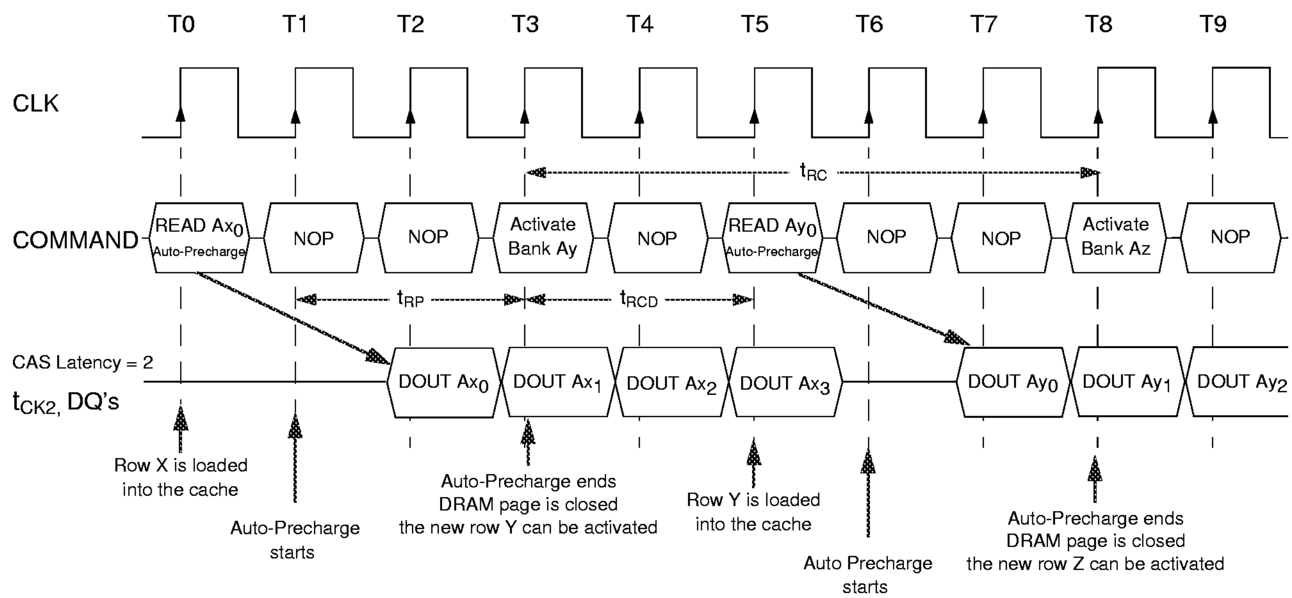
By the clock cycle following the Read command, the row data is present in both the cache and the sense amplifiers. Since all reads retrieve data from the cache and do not access the array, it is no longer necessary to hold the DRAM array open. As a result, the DRAM array can precharge on the clock cycle following the Read command using the auto-precharge function (Read with Auto-Precharge). The manual Precharge command cannot be used at this time because it would terminate the burst read. Manual precharge termination of a burst is still implemented in order to maintain backward compatibility with standard SDRAMs. To allow the burst to complete, the Precharge command can be given two clock cycles before the end of the read burst. Once the DRAM array is precharged the system can issue the Auto-Refresh command and/or another Bank Activate command during cache (page) read accesses.

DRAM Auto Refresh During Cache (Page) Reads (Burst Length = 4)



The ability of the ESDRAM to perform a bank activate during a cache (page) read gives the system the option to pipeline memory accesses to the same bank. Using pipelining, the precharge time and the t_{RCD} of a page miss can be completely hidden during a read burst. This is a very powerful feature of the ESDRAM, and in the case of random row reads, pipelining can double the bandwidth of the memory.

Read Followed by a Read Miss (Burst Length = 4)



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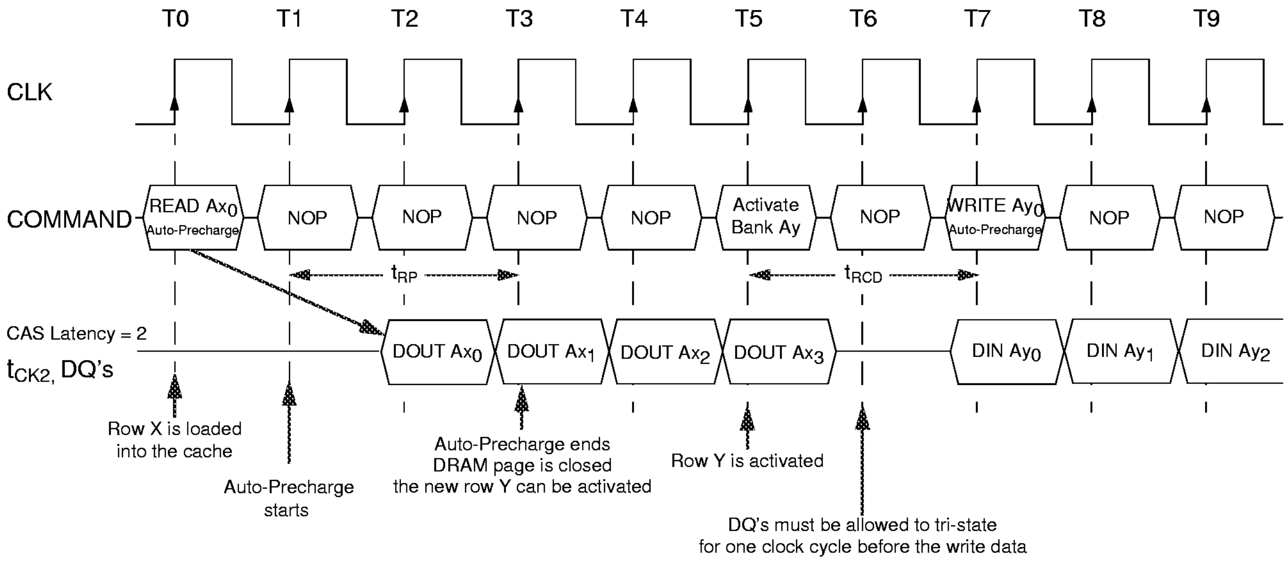
Read Miss Followed by a Write Miss (Burst Length = 4)



Combining the reduced latency of the ESDRAM with the capability of overlapping memory access cycles gives the ESDRAM a significant performance advantage over SDRAM (see the following "SDRAM vs. ESDRAM" figure). Note that write bursts cannot be pipelined due to the fact that the DRAM must be held open and cannot be precharged during a Write command execution.

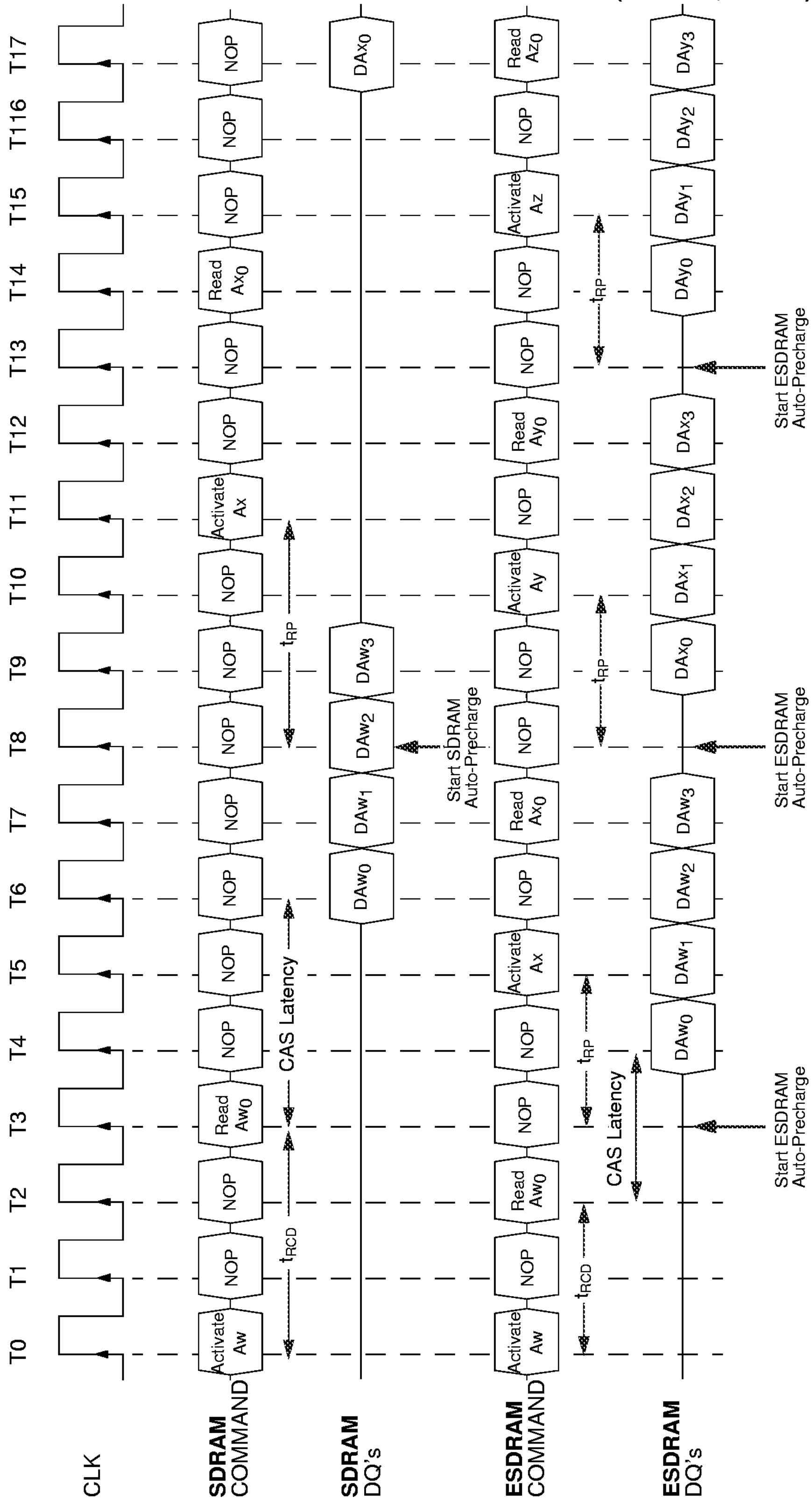
ESDRAM and SDRAM Compatibility

As a JEDEC superset standard, the ESDRAM represents an evolutionary improvement to a 16Mbit SDRAM. Consequently, the design of the ESDRAM is implemented in such a way as to maintain backward compatibility with JEDEC standard 16Mbit SDRAMs. The following is a list of some of the ESDRAM design points which maintain its compatibility with SDRAM:

1. Support for SDRAM command, address, and data setup/hold times
2. The same pinout and packages as JEDEC standard 16Mbit SDRAMs
3. The same command definitions and command sequence as an SDRAM
4. Support for CAS latency of 3 operation at all frequencies of operation

To elaborate on point 4, currently the ESDRAM is available with operating frequencies ranging from 100MHz to 166MHz with a CAS latency of 2. Standard SDRAMs require a CAS latency of 3 to operate at frequencies above 100 MHz. As a result, the ESDRAM supports CAS latencies of 2 or 3 at its operating frequencies. For example, a 100MHz CAS latency 2 ESDRAM part operates with 100MHz CAS latency 3 SDRAM controls. However, in this case, the performance of the ESDRAM is the same as an SDRAM because the SDRAM control is not taking advantage of the performance improvements of the ESDRAM. To summarize, from a functionality point of view, the ESDRAM is plug-compatible with an SDRAM, and it operates like a standard SDRAM when given SDRAM control signals.

SDRAM versus ESDRAM - Random Row Reads to the Same Bank (133MHz, BL = 4)



Commands

Commands Summary Table

Function	Page	CKE		Command Bus				DQM	A11	A10	A9 - A0	Notes
		Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$					
Mode Register Set	16	H	X	L	L	L	L	X	OP Code			
Bank Activate	19	H	X	L	L	H	H	X	BS	Row Address		2
Read	21	H	X	L	H	L	H	X	BS	L	Column	2
Read with Auto-Precharge	31	H	X	L	H	L	H	X	BS	H	Column	2
Write	21	H	X	L	H	L	L	X	BS	L	Column	2
Write with Auto-Precharge	31	H	X	L	H	L	L	X	BS	H	Column	2
Burst Stop	30	H	X	L	H	H	L	X	X	X	X	3
Single Bank Precharge	32	H	X	L	L	H	L	X	BS	L	X	2
Precharge all Banks	32	H	X	L	L	H	L	X	X	H	X	
Auto-Refresh (CBR)	36	H	H	L	L	L	H	X	X	X	X	
Self Refresh Entry	36	H	L	L	L	L	H	X	X	X	X	
Self Refresh Exit	36	L	H	NOP or DESEL				X	X	X	X	
No Operation (NOP)	36	H	X	L	H	H	H	X	X	X	X	
Device Deselect (DESEL)	36	H	X	H	X	X	X	X	X	X	X	
Clock Suspend Mode Entry	37	H	L	X	X	X	X	X	X	X	X	4
Clock Suspend Mode Exit	37	L	H	X	X	X	X	X	X	X	X	4
Power Down Mode Entry	36	H	L	NOP or DESEL				X	X	X	X	6
Power Down Mode Exit	36	L	H	NOP or DESEL				X	X	X	X	6
Data Write/Output Enable	22	H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable	22	H	X	X	X	X	X	H	X	X	X	5

1. All ESDRAM operations are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and DQM at the positive rising edge of the clock.
2. Bank Select (BS), if BS = 0 then bank A is selected, if BS = 1 then bank B is selected.
3. During a burst write cycle there is a zero clock delay, for a burst read cycle the delay is equal to the CAS latency.
4. During normal access mode, CKE is held high and CLK is enabled. When it is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ read and write operations. During a read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for write cycles. When it activates, the write operation at the clock is prohibited (zero clock latency).
6. All banks must be precharged before entering Power Down mode. The Power Down mode does not preform any refresh operations, therefore the device cannot remain in this mode longer than the refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.

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Mode Register Set Command

Power On and Initialization

The default power on state of the Mode register is undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs.

Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage no later than any of the input signal voltages. The power on voltage must not exceed VDD+0.3V on any of the input pins or power supplies. After power on, an initial pause of 100μs is required followed by a precharge of both banks using the Precharge command. In an attempt to reduce the possibility of data contention on the DQ bus during power on, it is recommended that the DQM pin(s) are held high during the initial pause period. Once both banks are precharged, a minimum of two auto refresh cycles (CBR) must occur before the Mode register is programmed. Prior to the Mode Register Set command, it is recommended that Deselect commands (instead of NOP commands) are issued. Failure to follow these steps may lead to unpredictable start-up modes.

Note: Once initialization is complete, a Bank Activate command must be issued prior to the first Read command. Otherwise, operation is unpredictable.

Programming the Mode Register

For application flexibility, CAS latency, burst length, burst sequence, and operation mode are user defined variables and must be programmed into the ESDRAM Mode register with a single Mode Register Set command. Any content of the Mode register can be altered by re-executing the Mode Register Set command. Even if the user chooses to modify only a subset of the Mode register variables, all four variables must be redefined when the Mode Register Set command is issued.

After initial power up, the Mode Register Set command must be issued before read or write cycles may begin. Both banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set command is issued. The Mode Register Set command is activated by the low signals of $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$ and $\overline{WE}$ at the positive edge of the clock. The address input data during this cycle defines the parameters set as shown in the following Mode Register Operation table. After the Mode Register Set command, two clocks are required before a new command is issued.

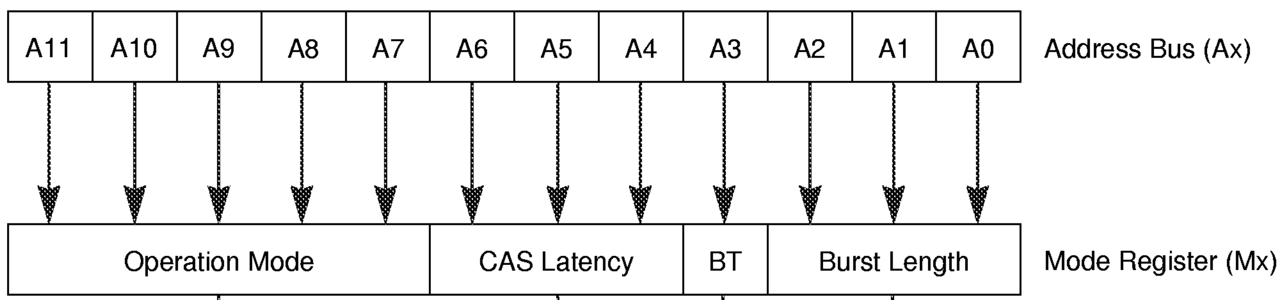
CAS Latency

The CAS latency is a parameter that is used to define the delay from when a Read command is registered on a rising clock edge to when the data from that Read command becomes available at the outputs. The CAS latency is expressed in terms of clock cycles and can have a value of 1, 2, or 3 cycles. The value of the CAS latency is determined by the speed grade of the device and the clock frequency that is used in the application. A table showing the relationship between the CAS latency, speed grade, and clock frequency appears in the Electrical Characteristics section of this document. Once the appropriate CAS latency is selected it must be programmed into the Mode register after power up. For an explanation of this procedure see Programming the Mode Register in the previous section.

Operation Mode

The ESDRAM has two operation modes which define how the cache is used on write cycles. If the operation mode is write transfer, then the Write command causes a previously activated row to load into the cache. In Write Transfer mode, the ESDRAM has two independent DRAM/cache banks which are controlled in the same manner as DRAM banks in standard SDRAMs. If the operation mode is no write transfer, the Write command does not transfer the activated row into the cache. In No Write Transfer mode, the ESDRAM has two independent cache read banks and two semi-independent DRAM write banks. This means that the system can have two different DRAM rows open for writing (one per DRAM bank) as well as two separate rows to read from in the cache (one per cache bank). While this is a potentially more powerful solution, the system must keep track of four open pages instead of two, leading to increased system complexity.

Mode Register Operation (Address Input For Mode Set)



Operation Mode

M11	M10	M9	M8	M7	Mode
0	0	0	0	0	Write Transfer
0	0	1	0	0	No Write Transfer
X	X	X	X	X	Reserved

Burst Type

M3	Type
0	Sequential
1	Interleaved

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

M2	M1	M0	Length	
			Sequential	Interleaved
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). There are two parameters that define how the Burst mode operates. These parameters are burst type and burst length. The burst type and burst length are programmable, and are determined by address bits A0 - A3 during the Mode Register Set command.

The burst type is used to define the order in which the burst data is delivered or stored to the SDRAM. Two types of burst are supported, sequential and interleaved. For more information, see the Burst Length and Type table below.

The burst length controls the number of bits output after a Read command, or the number of bits input after a Write command. The burst length is programmable to values of 1, 2, 4, 8 or full page (actual page length is dependent on organization: x4, x8, or x16). Full page burst operation is only possible using sequential addressing. A burst does not self terminate in full page mode, but continues even after the page length is satisfied.

Burst Length and Type

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleaved Addressing (decimal)
2	x x 0	0, 1	0, 1
	x x 1	1, 0	1, 0
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
Full Page (Note)	n n n	Cn, Cn+1, Cn+2,......	Not Supported

Note: Page length is a function of I/O organization and column addressing.

X4 organization (CA0-CA9); Page Length = 1024 bits per I/O

X8 organization (CA0-CA8); Page Length = 512 bits per I/O

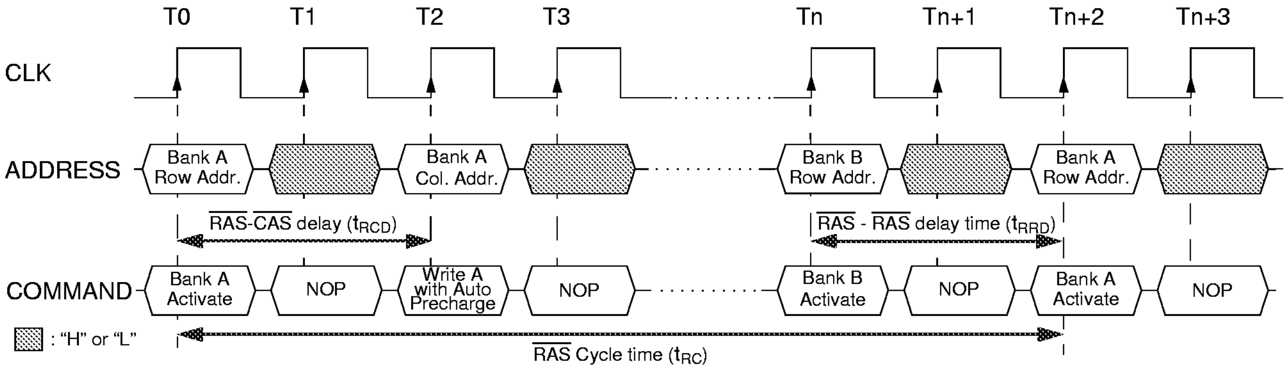
X16 organization (CA0-CA7); Page Length = 256 bits per I/O

Bank Activate Command

In relation to the operation of a fast page mode DRAM, the Bank Activate command corresponds to a falling $\overline{RAS}$ signal. The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank select address, A11 (sometimes referred to as BS), is used to select the desired bank. If BS is low bank A is activated, if BS is high bank B is activated. The row address A0 - A10 is used to determine which row to activate in the selected bank.

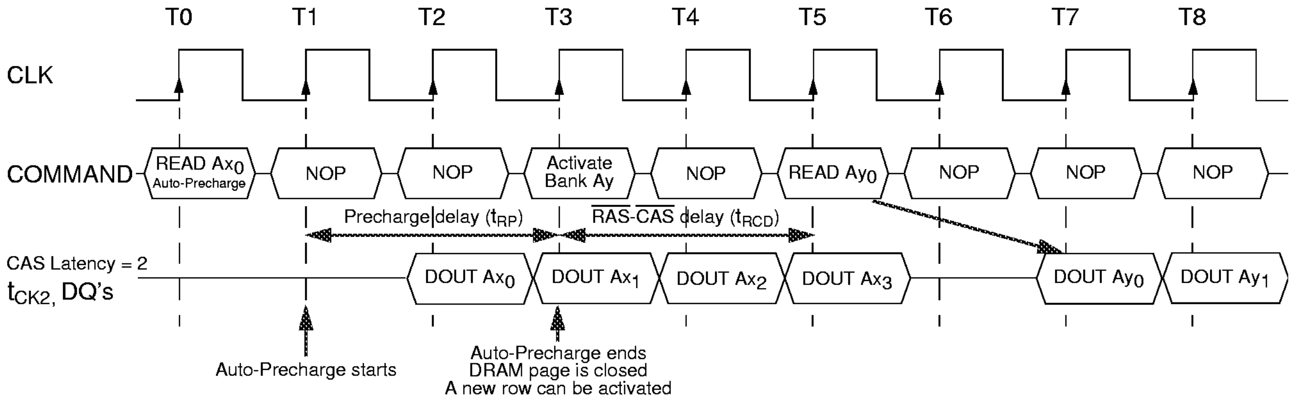
When accessing data that is not stored in either row cache the Bank Activate command must be applied before any read or write operation is executed. When a Bank Activate command is given, the row address is decoded and the selected row is latched by the sense amplifiers. However, the row is not loaded into the cache and the contents of the cache remain unchanged. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must meet or exceed the $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD}). Once a bank is activated it must be precharged before another Bank Activate command is applied to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the $\overline{RAS}$ cycle time of the device (t_{RC}). The minimum time interval between interleaved Bank Activate commands (bank A to bank B and vice versa) is the bank to bank delay time (t_{RRD}).

Bank Activate Command Cycle



Unlike a standard SDRAM, the ESDRAM allows the system to issue the Bank Activate command during a burst read cycle. This is because reads occur from the cache not the DRAM array. Therefore it is possible to issue Auto-Precharge and Bank Activate commands to the DRAM array without affecting the cache read. Writes, on the other hand, require that the page is open in the DRAM array. As a result, it is not possible to issue a Bank Activate command to the same bank during a burst write. Once a Bank Activate command is given, read or write operations cannot be initiated to the same bank until the $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD}) expires.

Bank Activate Command During a Burst Read Cycle (Burst Length = 4)



Read and Write Access Modes

Once a bank is activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high and $\overline{CAS}$ low at the clock's rising edge after the necessary $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}). $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low).

The first Read command issued after a Bank Activate command automatically transfers the data from the open DRAM page into the cache. This transfer is immediate and does not affect the latency of the first read cycle. If a Write command is given, the activated row may or may not be transferred into the cache. The operation mode in the Mode register is used to determine what occurs. If the operation mode is write transfer, then the Write command causes the activated row to load into the cache. If the operation mode is no write transfer, the Write command does not transfer the activated row into the cache and the contents of the cache remain unchanged.

The ESDRAM provides a wide variety of fast access modes. A single Read or Write command initiates a serial read or write operation on successive clock cycles. The number of serial data bits for each access is equal to the burst length, which is programmed into the Mode register. Although the burst length is user programmable, the boundary of the burst cycle is restricted to specific segments of the page length.

For example, the 2Mbit x 4 I/O x 2 bank device has a page length of 1024 bits per I/O (defined by CA0-CA9). If a burst length of 4 is programmed into the Mode register, then 256 boundary segments (4-bits each) are addressable. The first access begins at the column address (CA0-CA9) supplied to the device during the Read or Write command. However, the second access is not necessarily the next higher order column address. The second access is a function of the starting address, burst sequence, and burst boundary. Restated, the burst sequence is contained to four bits associated with one of the 256 possible boundary segments. The actual boundary segment (1 of 256) is determined by the eight higher order column addresses (CA2-CA9). The first access within this boundary segment is determined by the two low order column addresses (CA0-CA1) and the following three accesses are determined by the burst sequence.

The above discussion does not apply when full page burst is programmed into the Mode register. Full page burst length works only with the sequential burst sequence. The SDRAM device continues bursting data even after the entire page burst length is satisfied. The burst sequence starts at the column address defined during the read or write cycle and increments sequentially until the highest order column address is reached. At this point, the burst counter resets to address 0 and continues to perform burst read or burst write operations sequentially until either a Burst Stop command is issued, a Precharge command is issued to the bursting bank, or until a new Read or Write command is issued which interrupts the existing burst and begins a new burst at the new starting column address.

A new burst access can be started even before the previous burst ends. The ability to interrupt a burst operation at every clock cycle is supported. This is referred to as the 1-N rule. When the previous burst is interrupted by another Read or Write command, the remaining addresses are overridden by the new address once the CAS latency is satisfied.

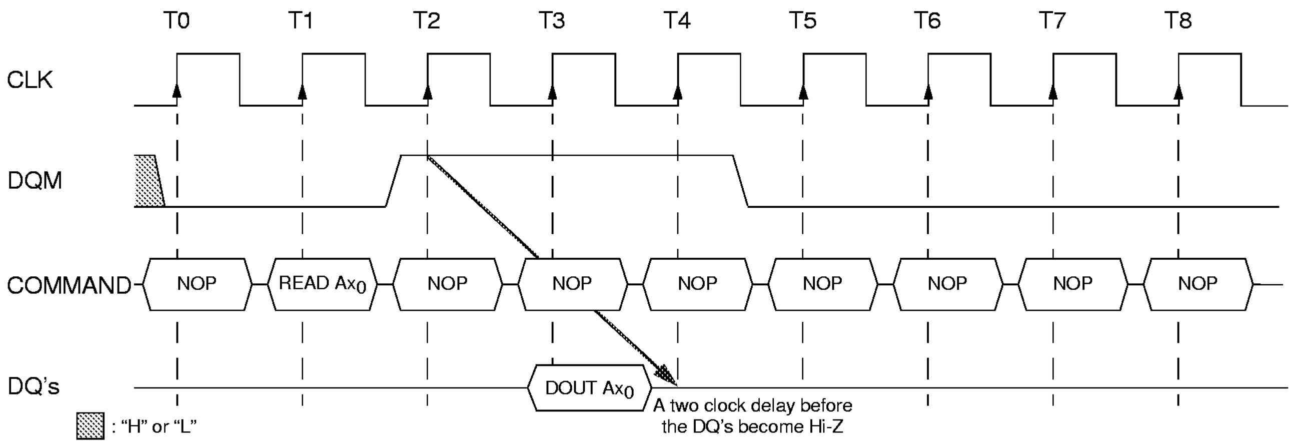
To perform a read or write cycle to a different row within an activated bank, the bank must be precharged and a new Bank Activate command issued. On a Burst Read command, all accesses occur from the cache. This allows the system to auto-precharge the DRAM array as soon as one clock cycle after the Read command is issued. Once the bank is precharged, it is also possible to activate a new row during a burst read from the cache. When the new Bank Activate command is given, any existing burst reads continue normally, but no new cache reads are allowed until time t_{RCD} after the Bank Activate command. After t_{RCD}, any new Read command causes the new row to load into the cache overwriting the previous row.

When both bank A and bank B are activated, interleaved (ping-pong) bank read or write operations are possible. By using the programmed burst length and alternating the access and precharge operations between the two banks, fast and seamless data access operation among many different pages are realized. When the two banks are activated, column to column interleave operation can be performed between two different pages. Finally, Read or Write commands can be issued to the same bank or between active banks on every clock cycle.

Data Mask

The ESDRAM has a data mask function that can be used in conjunction with data read and write cycles. When the data mask is activated (DQM high) during a write cycle, the write operation is prohibited immediately (zero clock latency). If the data mask is activated during a read cycle, the corresponding data outputs are disabled and become high impedance after a two clock delay, independent of CAS latency.

Data Mask Activated During a Read Cycle (Burst Length = 4, CAS Latency = 2)



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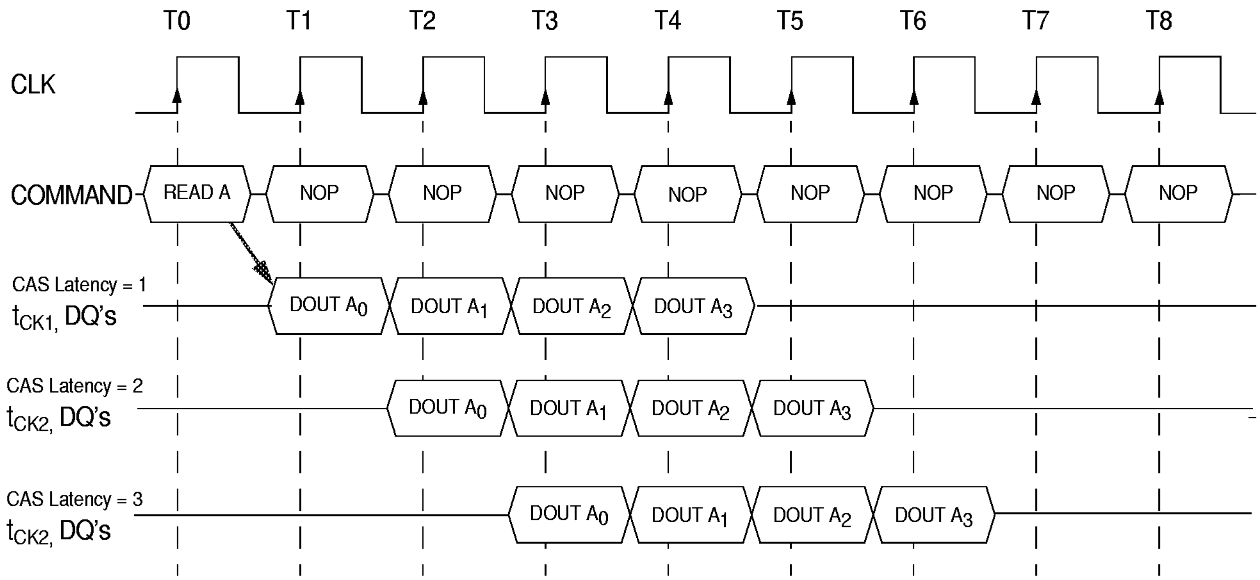
Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst, the Mode register settings determine burst type (sequential or interleaved) and burst length (1, 2, 4, 8, full page). The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the CAS latency that is set in the Mode register. The first Read command issued after a Bank Activate command automatically transfers the data from the open DRAM page into the cache.

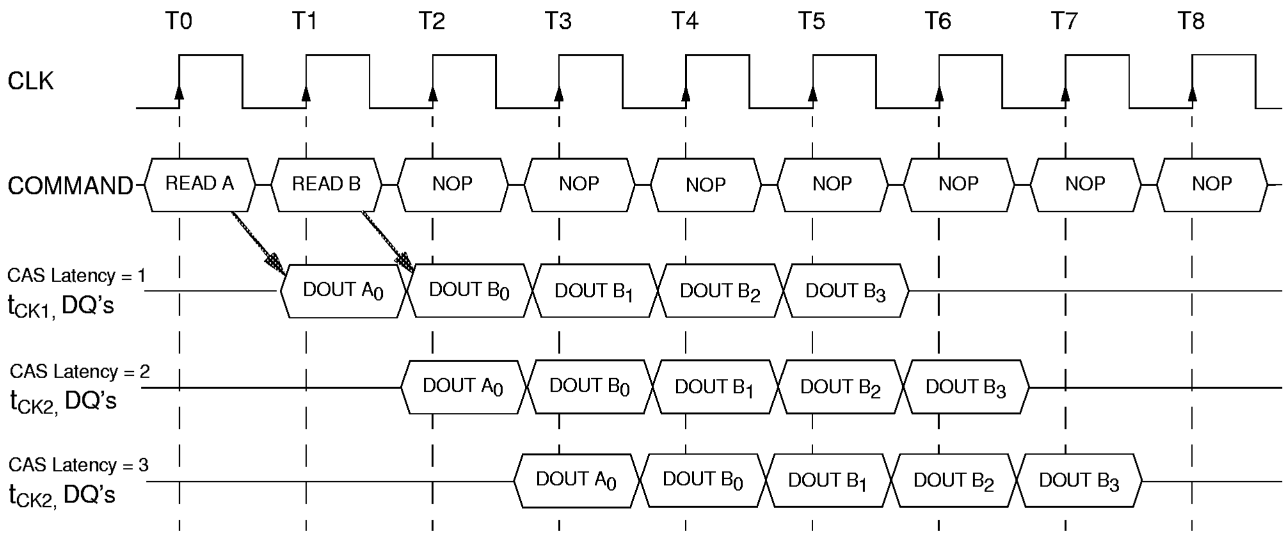
Burst Read Operation (Burst Length = 4)



Read Interrupted by a Read

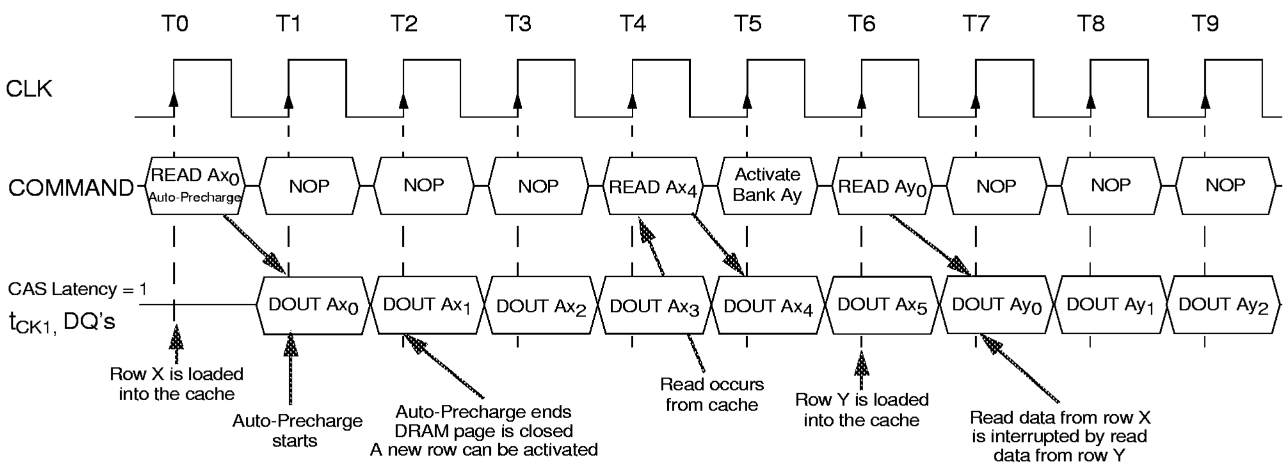
A Burst Read command may be interrupted before completion of the burst by another Read command, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the CAS latency from the interrupting Read command is satisfied, at this point the data from the interrupting Read command appears.

Read Interrupting a Read (Same Row, Burst Length = 4)

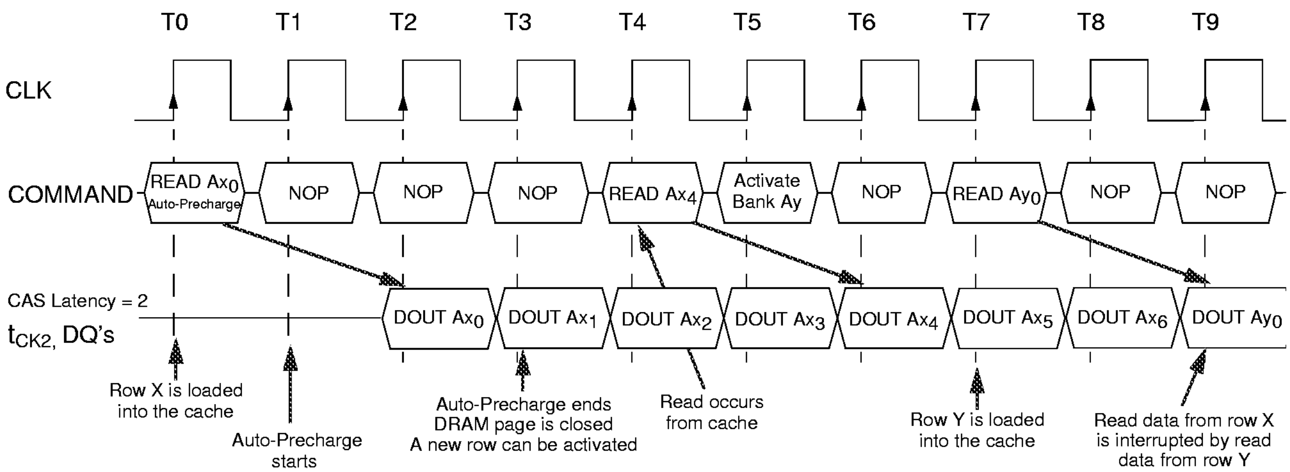


If the DRAM is auto-precharged and reactivated between the first Burst Read command and the interrupting Read command, then the interrupting read loads the new row into the cache and all subsequent read data comes from the new row.

Read Interrupting a Read (New Row, CAS Latency = 1, Burst Length = 4)



Read Interrupting a Read (New Row, CAS Latency = 2, Burst Length = 4)

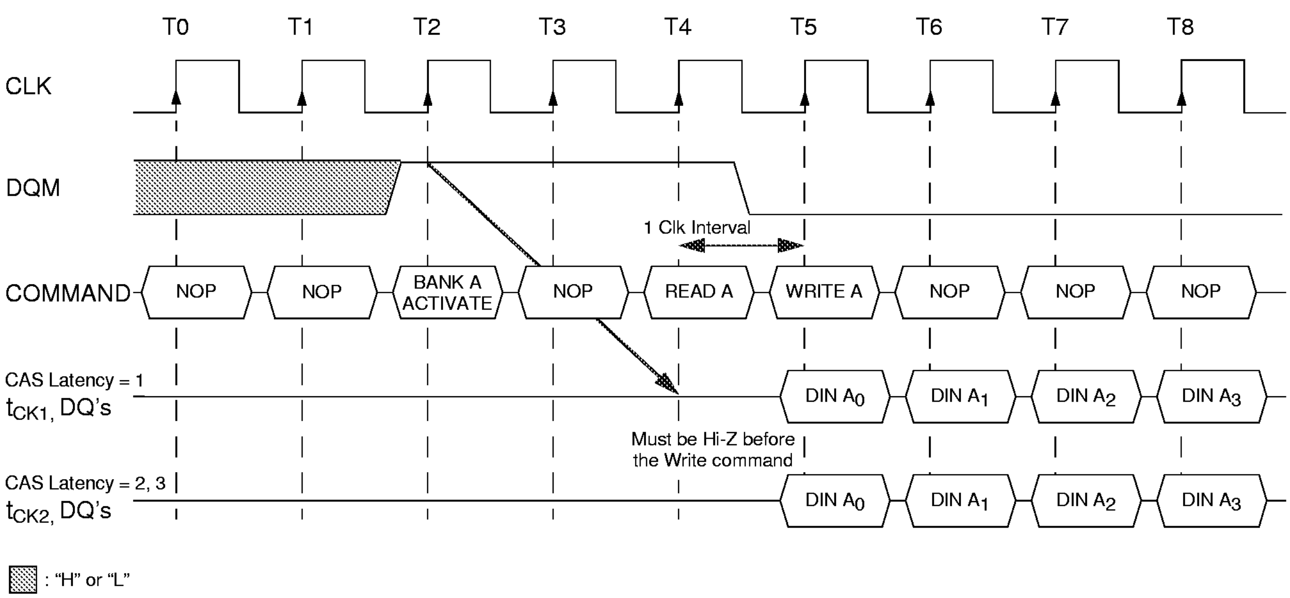


Read Interrupted by a Write

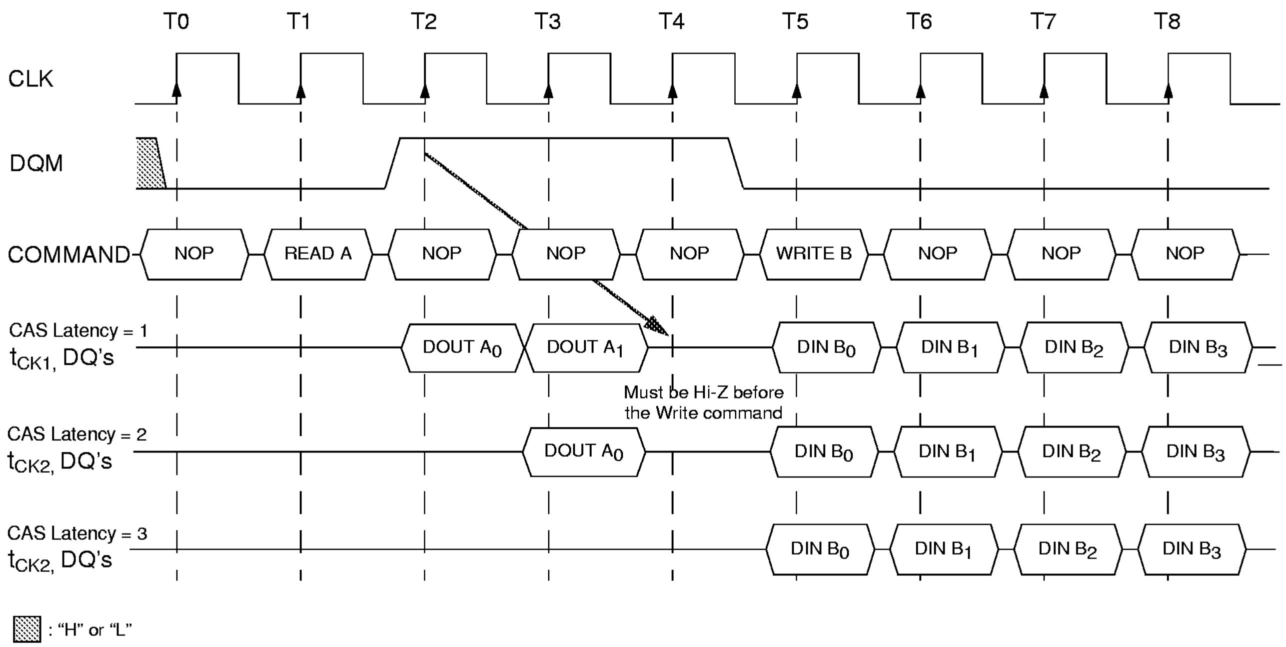
To interrupt a Burst Read command with a Write command, DQM must be used to avoid data contention on the I/O bus by placing the DQ's (output drivers) in a high impedance state at least one clock cycle before the Write command is initiated. To ensure the DQ's are tri-stated one cycle before the write operation begins, DQM must be activated at least 3 clock cycles before the Write command and be deactivated in the same clock cycle as the Write command.

When the CAS latency is 1, 2, or 3, the minimum interval between the Read and Write commands is one clock cycle.

Minimum Read to Write Interval: (DRAM Write Page Open, Burst Length = 4)

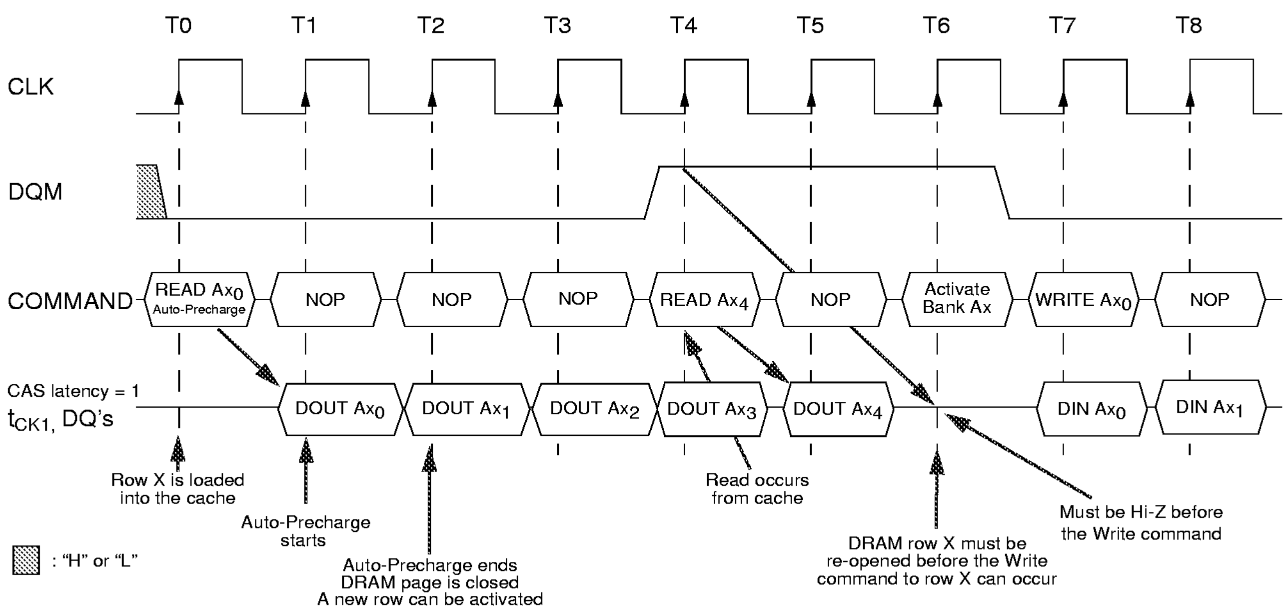


Non-minimum Read to Write Interval: DRAM Write (Page Open, Burst Length = 4)

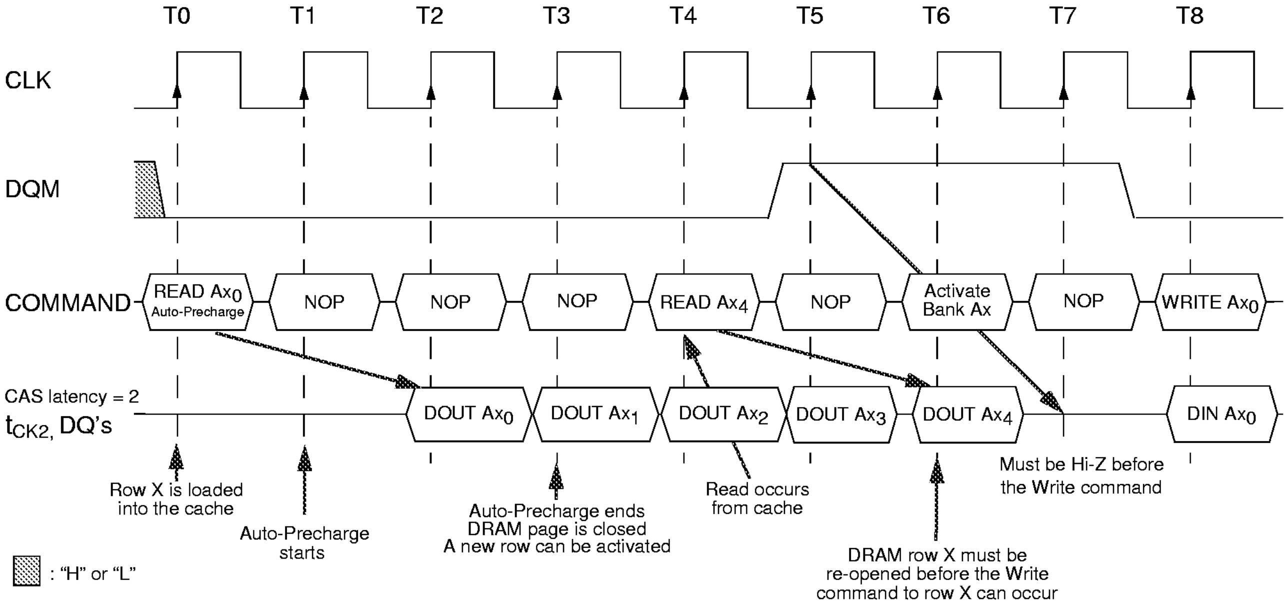


The ESDRAM allows the user to close the DRAM page and still read from the cache. Therefore, it is possible to interrupt a Read command with a Write command. The DRAM row must be open in order to write the incoming data. Consequently, the system must issue a Bank Activate command to the DRAM before the interrupting Write command can reopen the closed row.

Non-minimum Read to Write Interval (DRAM Precharged, CAS Latency = 1, Burst Length = 4)



Non-minimum Read to Write Interval (DRAM Precharged, CAS Latency = 2, Burst Length = 4)

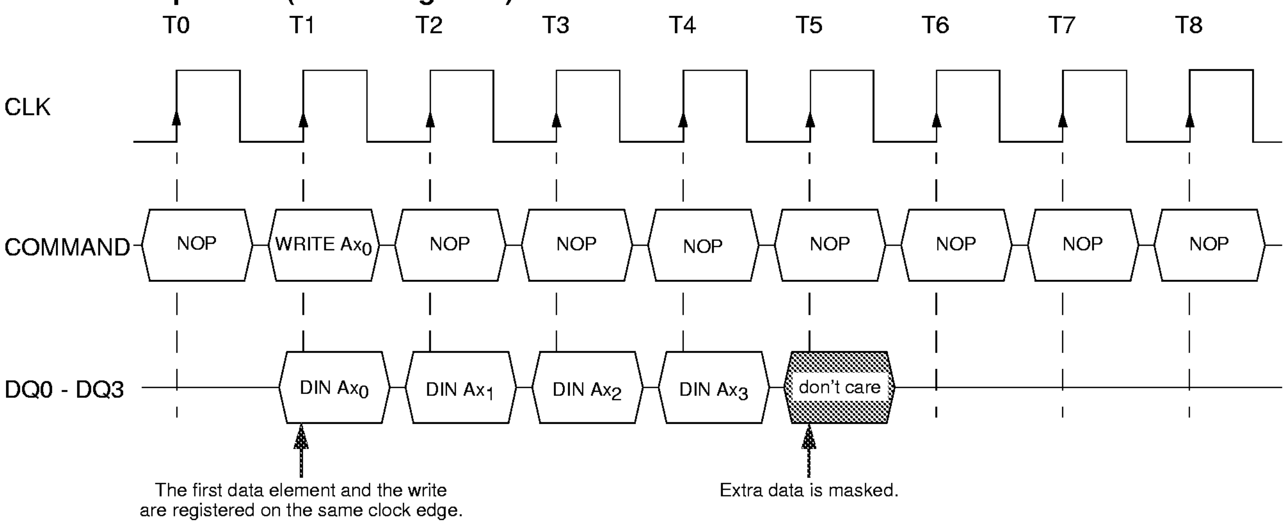


Burst Write Command

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. There is no CAS latency required for burst write cycles. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. When the burst completes, any additional data supplied to the DQ pins is ignored.

Unlike the Read command which allows the system to perform reads from the cache while the DRAM page is closed, the Write command requires that the DRAM page is open, even on a cache (page) hit. If a write hit occurs (the write row corresponds to the row currently in the cache), both the cache and DRAM array are updated simultaneously in order to maintain cache coherency. When a cache miss occurs the new row must be activated. This new row may or may not be transferred into the cache. The operation mode in the Mode register is used to determine what occurs. If the operation mode is write transfer, then the Write command causes the activated row to load into the cache. If the operation mode is no write transfer, the Write command does not transfer the activated row into the cache and the contents of the cache remain unchanged.

Burst Write Operation (Burst Length = 4)



Write Interrupted by a Write

A Burst Write command may be interrupted before completion of the burst by another Write command, with the single restriction that the interval separating the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are ignored, and data is written to the new addresses until the programmed burst length is satisfied.

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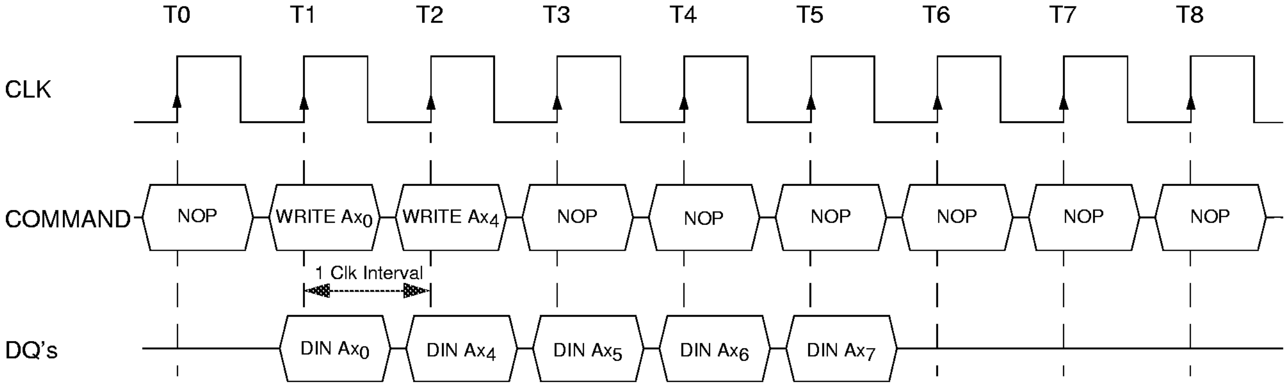
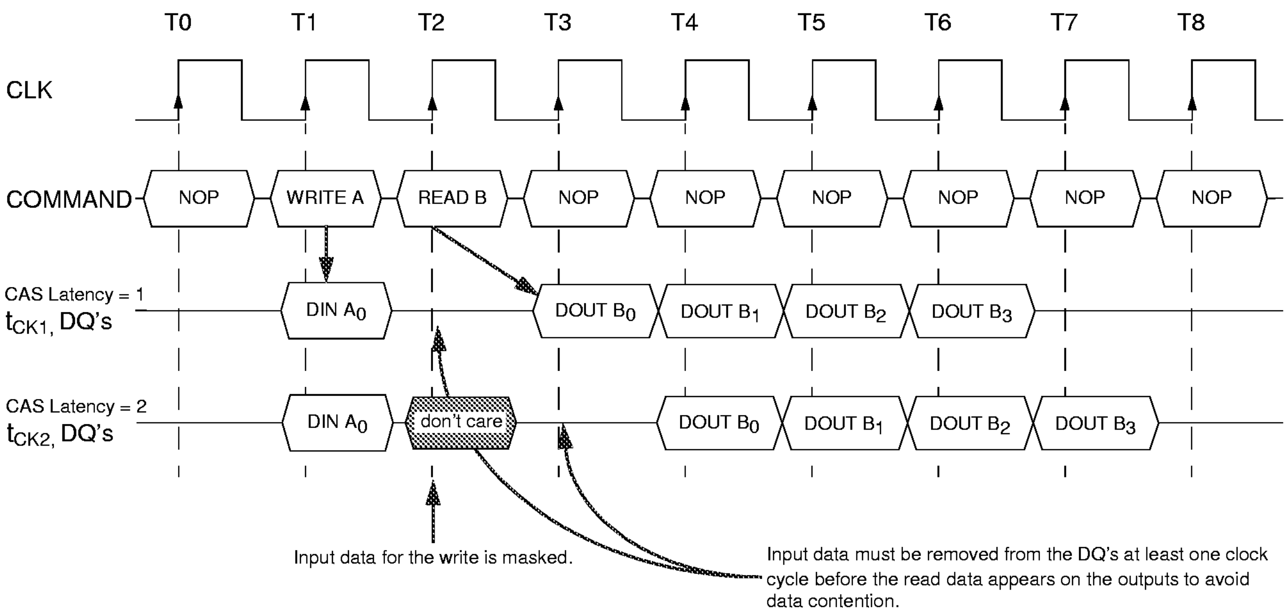
Write Interrupted by a Write (Burst Length = 4)



Write Interrupted by a Read

A Read command interrupts a Burst Write command on the same clock cycle that the Read command is registered. The data bus must be in the high impedance state at least one cycle before the interrupting read data appears on the outputs to avoid data contention. After the Read command is registered, any residual data from the burst write cycle is ignored. In addition, if the ESDRAM is in No Write Transfer mode, the Read command does not cause the open DRAM page to load into the cache. This makes it possible to read from the page in the cache, and write to a different page in the DRAM within the same ESDRAM bank. Data that is presented on the DQ pins before the Read command is initiated is actually written to the memory.

Write Interrupted by a Read (Burst Length = 4, CAS Latency = 1, 2)

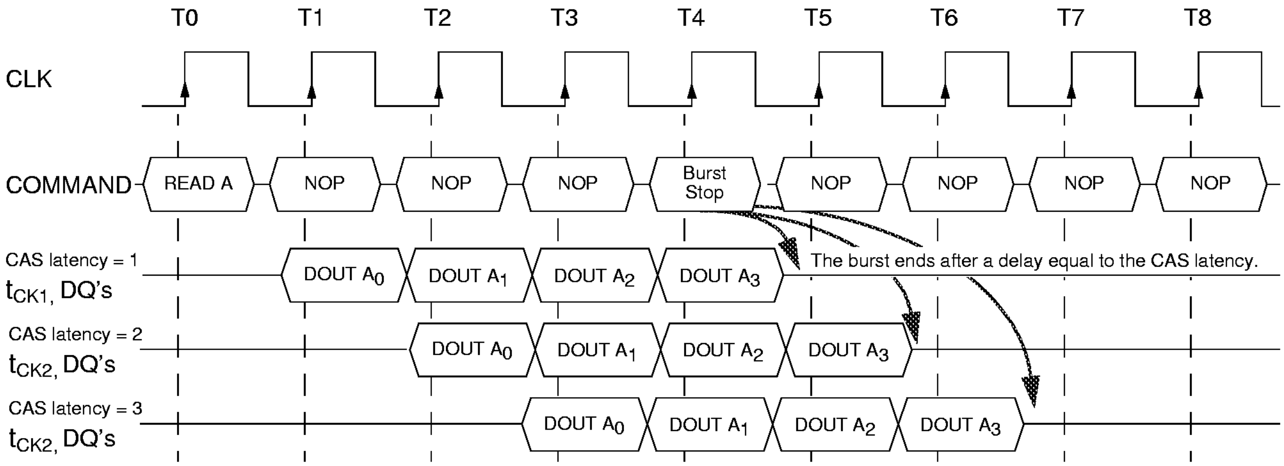


Burst Stop Command

Once a burst read or burst write is initiated, there are several ways to terminate the burst operation prematurely. These methods include using another Read or Write command to interrupt the existing burst, using a Precharge command to interrupt the burst and close the active bank, or using the Burst Stop command to terminate the existing burst but leave the bank open for future reads or writes to the same page of the active bank. When interrupting a burst with another Read or Write command care must be taken to avoid DQ contention. The Burst Stop command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it completes. The Burst Stop command is defined by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock.

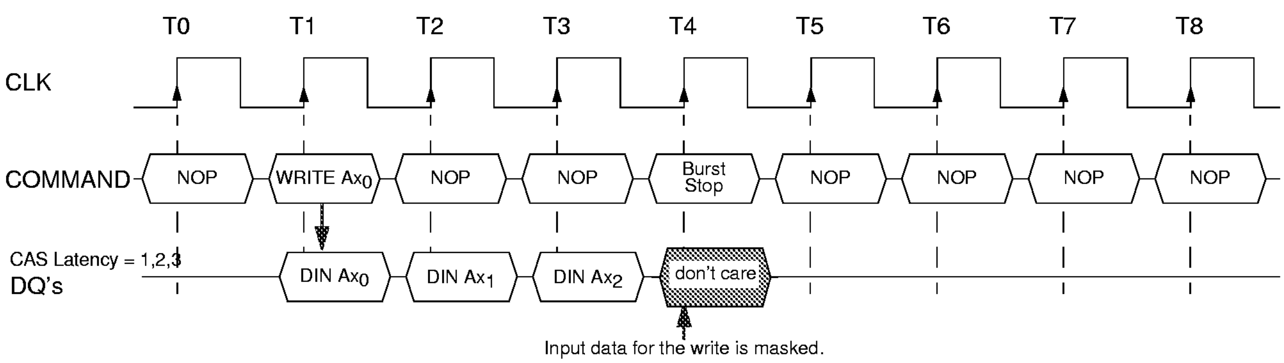
When using the Burst Stop command during a burst read cycle, the data DQ's go to a high impedance state after a delay which is equal to the CAS latency set in the Mode register.

Termination of a Burst Read Operation (Burst Length ≥ 4, CAS Latency = 1, 2, 3)



If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle is ignored. Data that is presented on the DQ pins before the Burst Stop command is registered is written to the memory.

Termination of a Burst Write Operation (Burst Length ≥ 4, CAS Latency = 1, 2, 3)



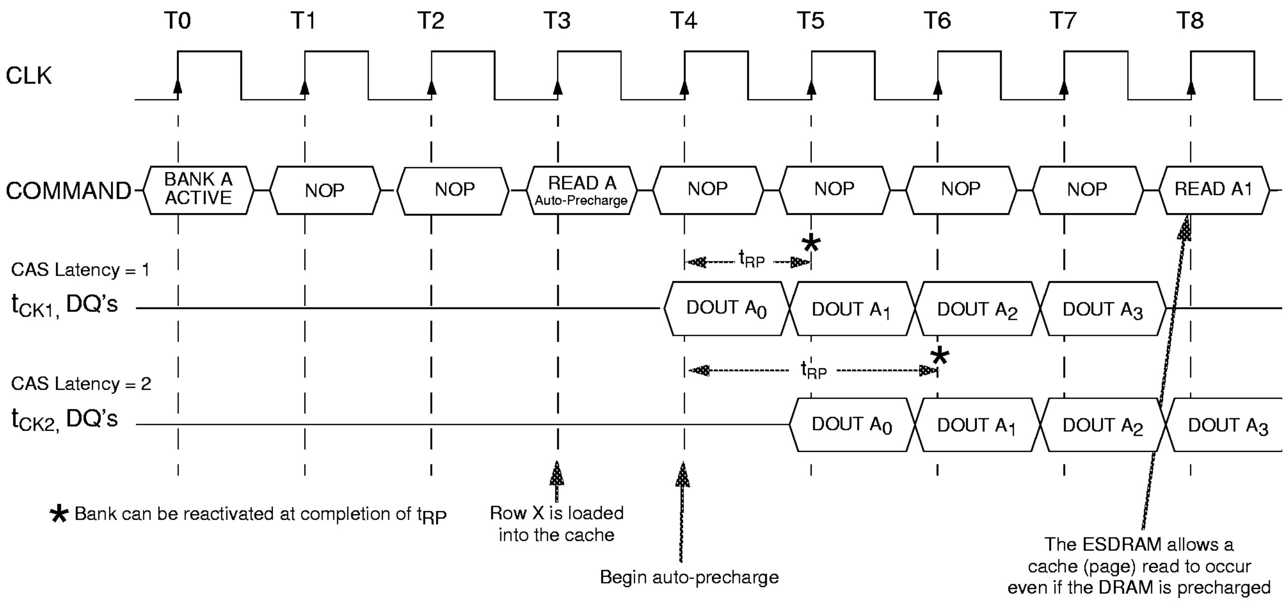
Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the ESDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read command executes normally with the exception that the active bank begins to precharge on the next clock cycle. This feature allows the precharge operation to be completely hidden during burst read cycles, improving system performance for random data access. Auto-precharge can also be implemented during Write commands although precharge cannot begin any sooner than is possible by issuing the Precharge command directly to the device.

Note that the ESDRAM, unlike a standard SDRAM, allows Read commands to execute even after the row is precharged. This can occur because the row data is loaded into the cache.

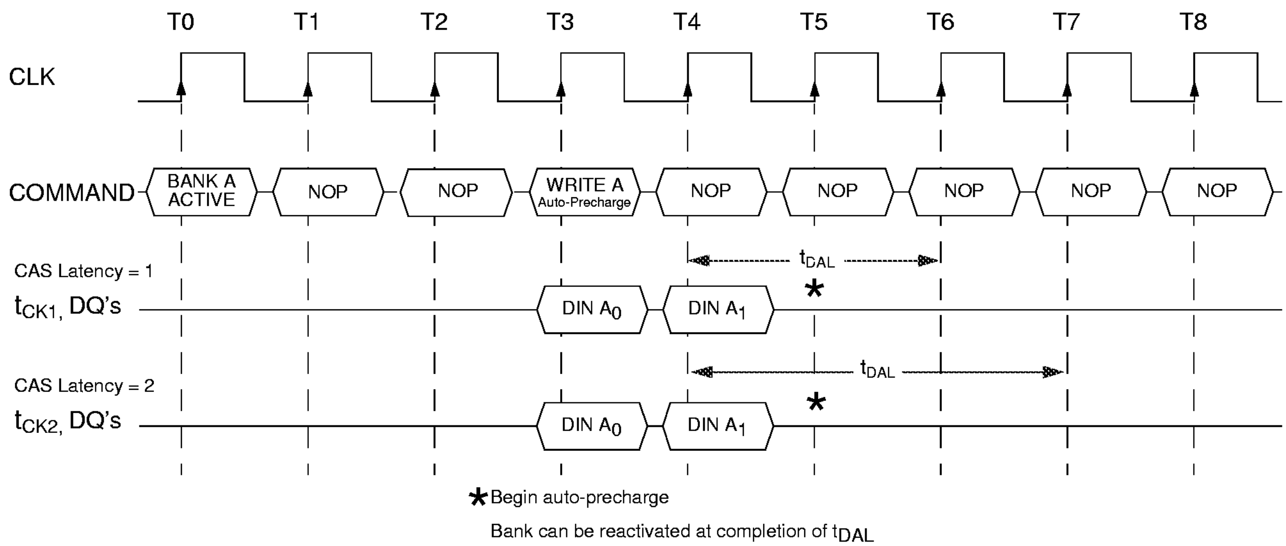
If A10 is high when a Read command is issued, a read with auto-precharge function is initiated. The ESDRAM automatically enters the precharge operation one clock after the Read command is registered. Once the precharge operation starts, the bank cannot be reactivated until the precharge time (t_{RP}) is satisfied.

Burst Read with Auto-Precharge (Burst Length = 4, CAS Latency = 1, 2)



If A10 is high when a Write command is issued, a write with auto-precharge function is initiated. The ESDRAM automatically enters the precharge operation a clock delay from the last burst write cycle. This delay is referred to as t_{DPL}. The bank undergoing auto-precharge cannot be reactivated until t_{DPL} and t_{RP} are satisfied. This is referred to as t_{DAL}, data-in to active delay ($t_{DAL} = t_{DPL} + t_{RP}$). For auto-precharged write cycles including full page, the device auto-precharges once any one of four commands are issued: Precharge, Burst Termination, Read to the other bank, or Write to the other bank.

Burst Write with Auto-Precharge (Burst Length = 2, CAS Latency = 1, 2)



Precharge Command

The Precharge command is used to precharge or close a bank that is activated. The Precharge command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge command can precharge each bank separately or both banks simultaneously. Two address bits A10 and A11 (BS) are used to define which bank(s) to precharge when the command is issued.

Bank Selection for Precharge by Address Bits

A10	BS(A11)	Precharged Bank(s)
LOW	LOW	Bank A only
LOW	HIGH	Bank B only
HIGH	DON'T CARE	Both Banks A and B

For read cycles when CAS latency = 1, the Precharge command may be applied coincident with the last clock of the burst read cycle. For read cycles when CAS latency = 2, the Precharge command may be applied coincident with the second to last clock of a burst read cycle. If a Precharge command is issued any sooner in the burst, it prematurely terminates the burst.

For write cycles, however, a delay must be satisfied from the start of the last burst write cycle until the Precharge command can be issued. This delay is known as t_{DPL}, data-in to precharge delay.

After the Precharge command is issued, the precharged bank must be reactivated before a new Write command can be executed. The delay between the Precharge command and the Activate command must be greater than or equal to the precharge time (t_{RP}).

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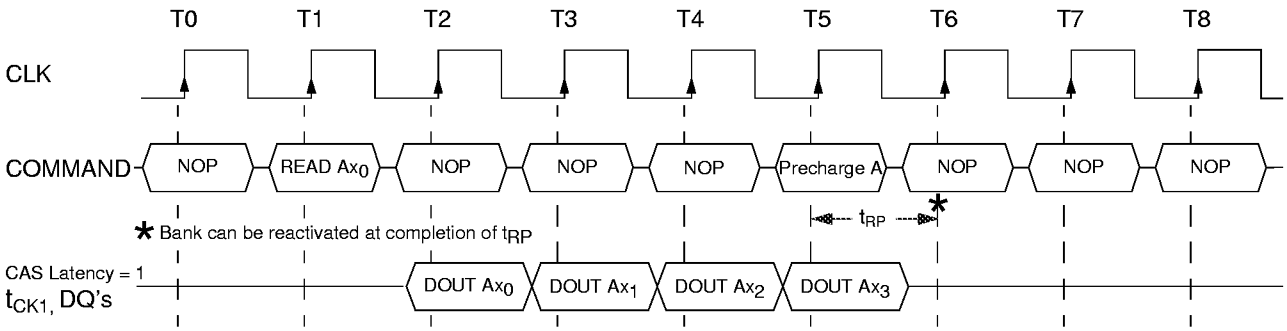
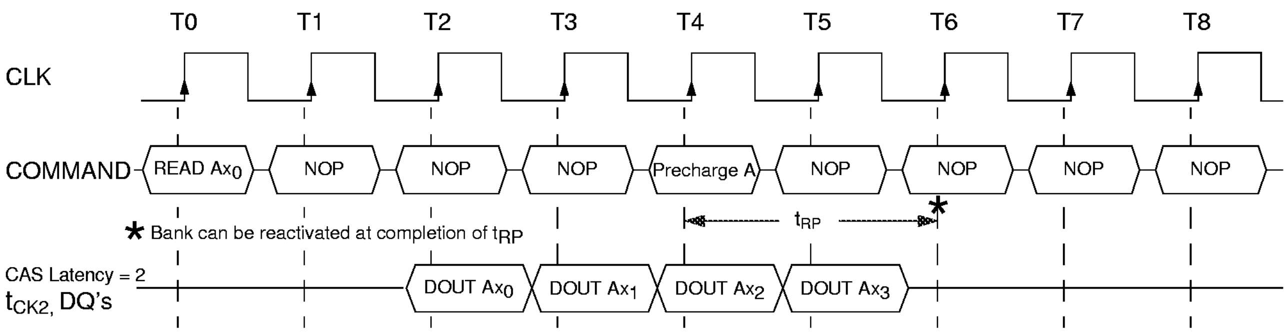
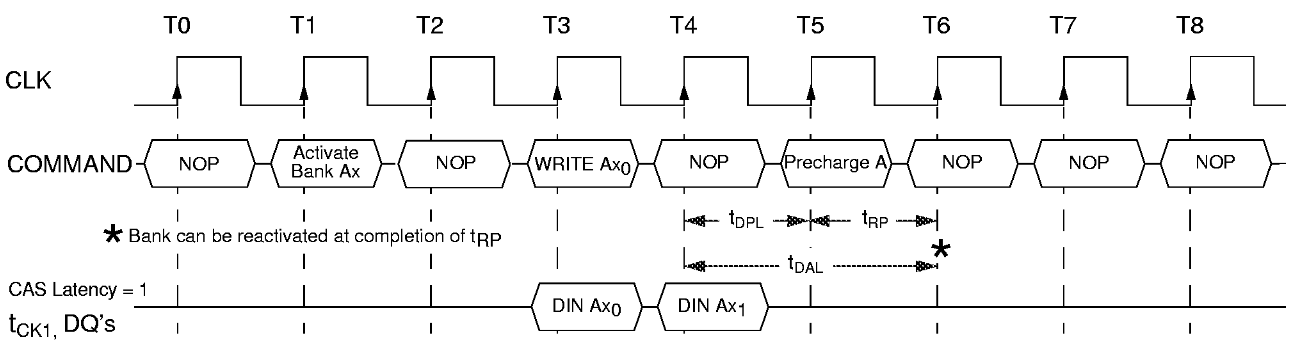
Burst Read followed by the Precharge Command (Burst Length = 4, CAS Latency = 1)



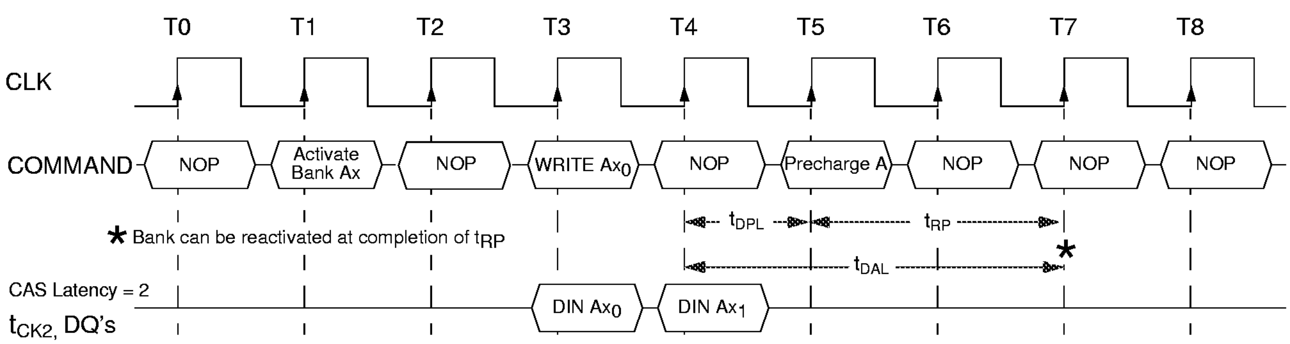
Burst Read followed by the Precharge Command (Burst Length = 4, CAS Latency = 2)



Burst Write followed by the Precharge Command (Burst Length = 2, CAS Latency = 1)



Burst Write followed by the Precharge Command (Burst Length = 2, CAS Latency = 2)

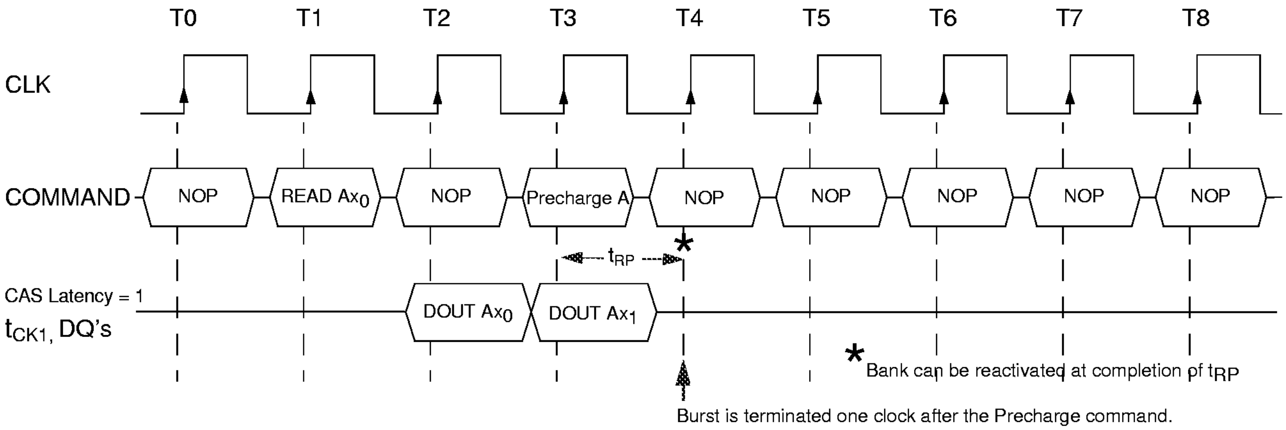


Precharge Termination

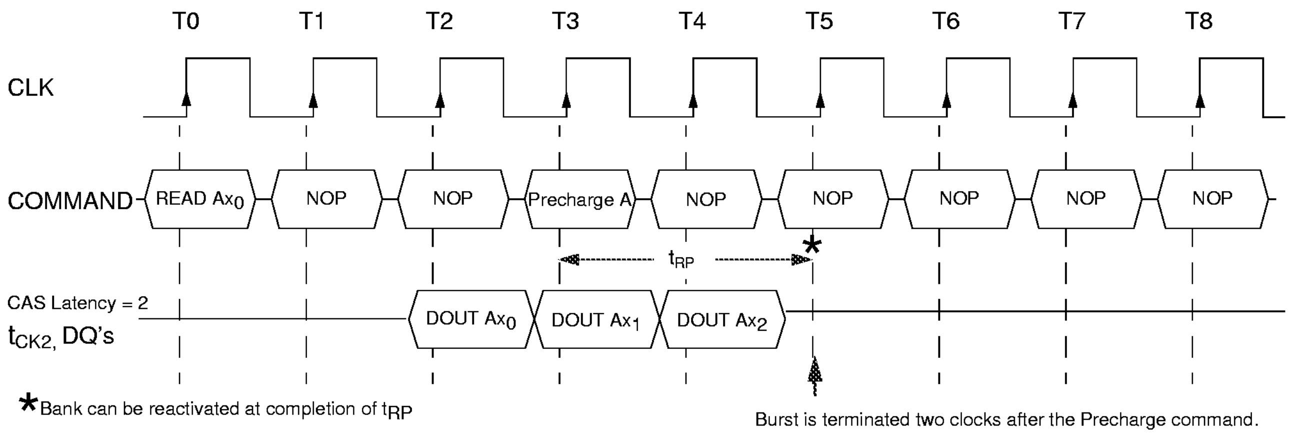
The Precharge command may be used to terminate either a burst read or burst write operation. When the Precharge command is issued, the burst operation is terminated and bank precharge begins. However, a Precharge command to one bank does not terminate a burst operation to or from the other bank.

For burst read operations, valid data continues to appear on the data bus as a function of CAS latency.

Burst Read Interrupted by Precharge (Burst Length = 8, CAS Latency = 1)

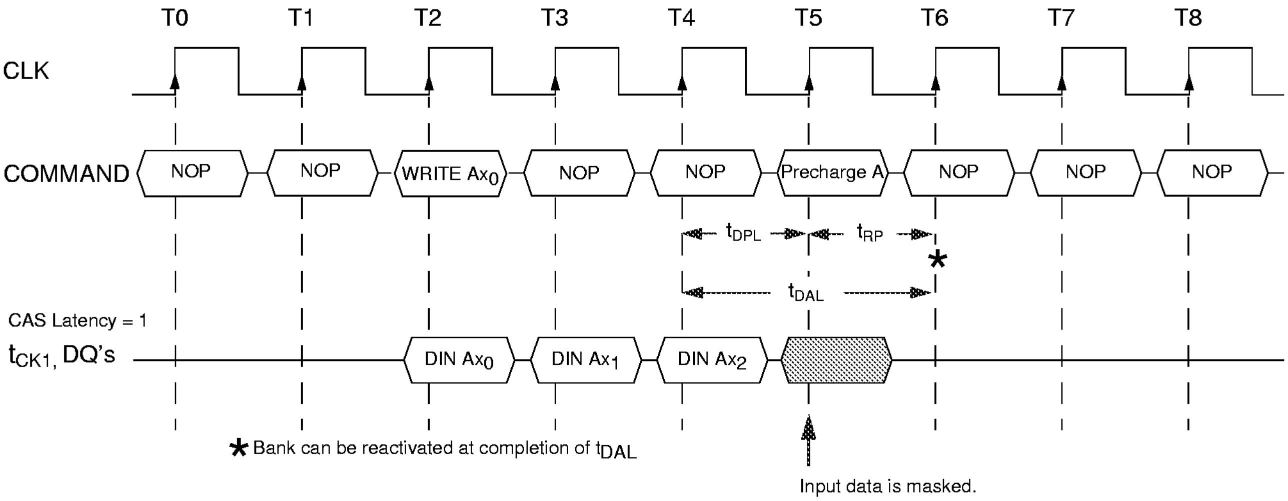


Burst Read Interrupted by Precharge (Burst Length = 8, CAS Latency = 2)

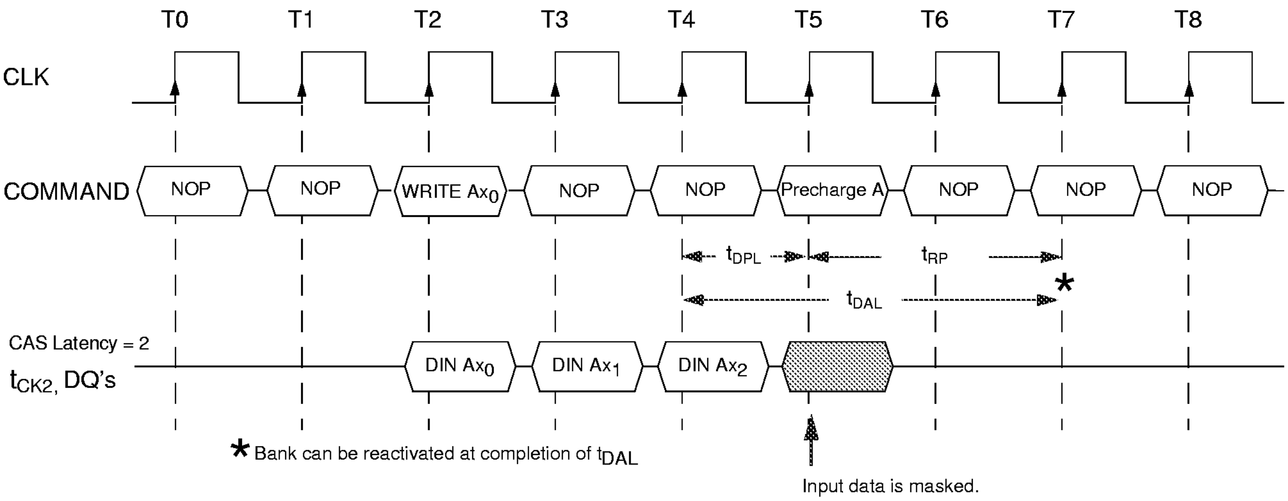


Burst write operations are terminated by the Precharge command. Write data written to the device during the Precharge command is masked.

Precharge Termination of a Burst Write (Burst Length ≥ 4, CAS Latency =1)



Precharge Termination of a Burst Write (Burst Length ≥ 4, CAS Latency = 2)



Auto-Refresh Command ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low with CKE and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Auto-Refresh mode (CBR). Both banks of the ESDRAM must be precharged and idle for a minimum of the precharge time (t_{RP}) before the Auto-Refresh command (CBR) can be applied. An address counter, internal to the device, decrements the word and bank address during the refresh cycle. No control of the external address pins is required once this cycle starts. The auto-refresh cycle restores the word line after the sense amplifiers are set, this eliminates the need to apply a Precharge command externally.

Note that the ESDRAM, unlike a standard SDRAM, allows Read commands during auto-refresh cycles. This can occur because read accesses occur from the cache and do not require access to the DRAM array.

When the refresh cycle completes, both banks of the ESDRAM are in the precharged (idle) state. A delay between the Auto-Refresh command (CBR) and the next Activate command or subsequent Auto-Refresh command must be greater than or equal to the $\overline{RAS}$ cycle time (t_{RC}).

Self Refresh Command

The ESDRAM device has a built-in timer to accommodate self refresh operation. The Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the Self Refresh command is registered, CKE must be held low to keep the device in Self Refresh mode. When the ESDRAM enters self refresh all of the external control signals, except CKE, are disabled. The clock is internally disabled during self refresh to save power. The user may halt the external clock while the device is in self refresh, however, the clock must be restarted before the device can exit self refresh. Once the clock is cycling, the device exits self refresh operation on the second positive clock transition after CKE is returned high. A minimum delay time is required when the device exits self refresh operation and before the next command is issued. This delay is equal to the $\overline{RAS}$ cycle time (t_{RC}).

No Operation Command

The purpose of the No Operation command is to prevent the ESDRAM from registering any unwanted commands between, or during, operations. A No Operation command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation command does not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect command performs the same function as a No Operation command. The Deselect command occurs when $\overline{CS}$ is brought high, at which time the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don’t cares.

Power Down Mode

In order to reduce standby power consumption, a Power Down mode is available. All banks must be precharged and the necessary precharge delay (t_{RP}) must occur before the ESDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device cannot remain in Power Down mode longer than the refresh period (t_{REF}) of the device.

The Power Down mode is exited by bringing CKE high. A one clock delay after the registration of CKE high is required for the ESDRAM to exit the Power Down mode.

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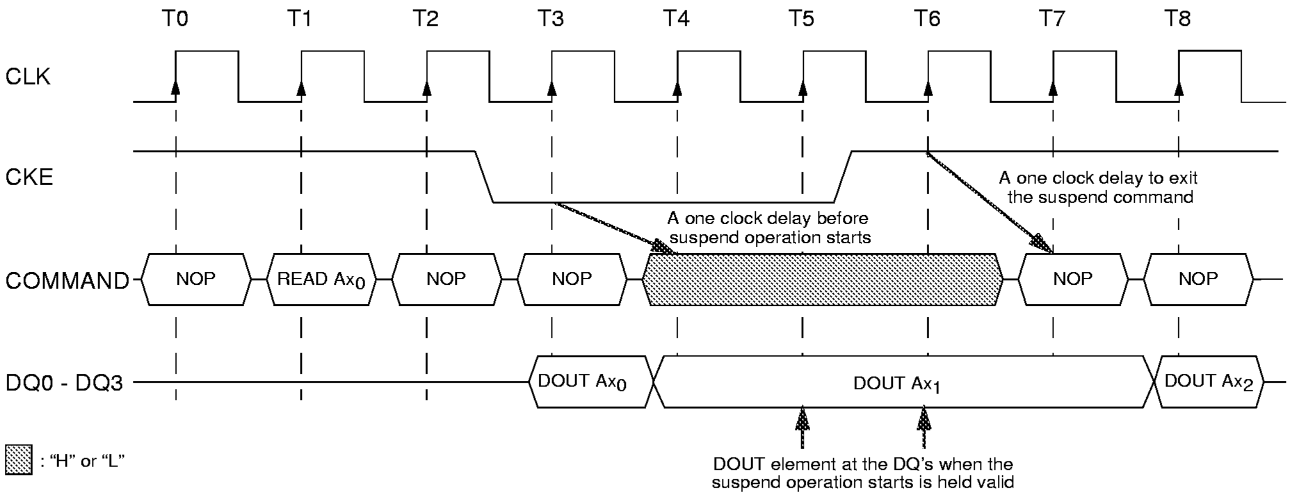
Clock Suspend Mode

During normal access operation, CKE is held high enabling the clock. When CKE is registered low, Clock Suspend mode is entered. The Clock Suspend mode deactivates the internal clock and suspends or "freezes" any clocked operation that is currently executing. There is a one clock delay between the registration of CKE low and the time at which ESDRAM operation is suspended. While in Clock Suspend mode, the ESDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

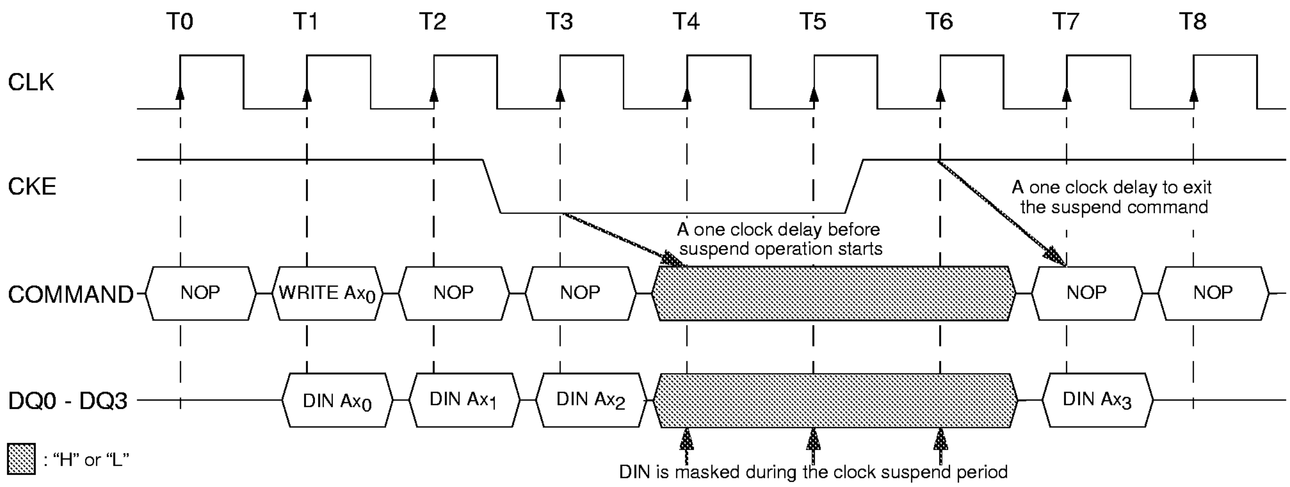
When the operation of the ESDRAM is suspended during the execution of a burst read operation, the last valid data on the DQ pins is actively held valid until Clock Suspend mode is exited.

Clock Suspend During a Read Cycle (Burst Length = 4, CAS Latency = 2)



If Clock Suspend mode is initiated during a burst write operation, then the input data is masked and ignored until the Clock Suspend mode is exited.

Clock Suspend During a Write Cycle (Burst Length = 4, CAS Latency = 2)



Clock Enable (CKE) Truth Table

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10 - A0		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit self refresh with device deselect	2
	L	H	L	H	H	H	X	X	Exit self refresh with no operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain self refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down mode exit, all banks idle	2
	L	H	L	X	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain power down mode	
All Banks Idle	H	H	H	X	X	X			Refer to the idle state section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	CBR refresh	
	H	H	L	L	L	L	OP Code		Mode register set	4
	H	L	H	X	X	X			Refer to the idle state section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry self refresh	4
	H	L	L	L	L	L	OP Code		Mode register set	
	L	X	X	X	X	X	X	X	Power down	4
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to operations in the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin clock suspend next cycle	5
	L	H	X	X	X	X	X	X	Exit clock suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain clock suspend	

1. For the given current state CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CKS}) must be satisfied before any command other than exit is issued.
3. The address inputs (A11 - A0) depend on the command that is issued. See the Idle State section of the Current State Truth Table for more information.
4. The Power Down mode, Self Refresh mode, and the Mode register set state can only be entered from the all banks idle state.
5. Must be a legal command as defined in the Current State Truth Table.

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Current State Truth Table (Notes: 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10 - A0	Description		
Idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode register	2
	L	L	L	H	X	X	Auto or Self Refresh	Start auto or self refresh	2, 3
	L	L	H	L	X	X	Precharge	No operation	
	L	L	H	H	BS	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BS	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BS	Column	Read w/o Precharge	Start a cache read	
	L	H	H	L	X	X	Burst Termination	No operation	
	L	H	H	H	X	X	No Operation	No operation	
	H	X	X	X	X	X	Device Deselect	No operation or power down	5
Row Active	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Precharge	6
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	If Write Transfer mode and if new row, load into cache; start write; determine if auto precharge	7, 8
	L	H	L	H	BS	Column	Read	If new row load into cache; start read; determine if auto precharge	7, 8
	L	H	H	L	X	X	Burst Termination	No operation	
	L	H	H	H	X	X	No Operation	No operation	
	H	X	X	X	X	X	Device Deselect	No operation	
Cache Read (DRAM Active)	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate burst; start the precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Terminate burst; start the write cycle	8, 9
	L	H	L	H	BS	Column	Read	Terminate burst; start a new read cycle	8, 9
	L	H	H	L	X	X	Burst Termination	Terminate the burst	
	L	H	H	H	X	X	No Operation	Continue the burst	
	H	X	X	X	X	X	Device Deselect	Continue the burst	

1. CKE is assumed active (high) in the previous cycle for all entries. The current state is the state of the bank to which the command is being applied.
2. Both banks must be idle otherwise it is an illegal action.
3. If CKE is active (high) the ESDRAM will start the auto refresh (CBR) operation, if CKE is inactive (low) then the Self Refresh mode is entered.
4. The current state refers only to one of the banks. If BS selects this bank then the action specified in the table is taken. However, if BS selects the bank not being referenced by the current state then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered, otherwise there is a no operation.
6. The minimum and maximum row active time (t_{RAS}) must be satisfied.
7. The $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the auto precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.
11. The precharge starts on the Nth clock following the issued command where N=burst length. Additional Read or Write commands may be issued prior to the completion of the burst to extend the time at which precharge begins.

Current State Truth Table (Continued) (Notes: 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10 - A0	Description		
Cache Read (DRAM Idle)	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	Self refresh is ILLEGAL; Start auto refresh	
	L	L	H	L	X	X	Precharge	Terminate burst;	
	L	L	H	H	BS	Row Address	Bank Activate	Activate a new DRAM row	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	Terminate burst; start a new read cycle	8, 9
	L	H	H	L	X	X	Burst Termination	Terminate the burst	
	L	H	H	H	X	X	No Operation	Continue the burst	
	H	X	X	X	X	X	Device Deselect	Continue the burst	
Write	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate burst; start the precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write, Write AP	Terminate burst; start a new write cycle	8, 9
	L	H	L	H	BS	Column	Read, Read AP	Terminate burst; start the read cycle	8, 9
	L	H	H	L	X	X	Burst Termination	Terminate the burst	
	L	H	H	H	X	X	No Operation	Continue the burst	
	H	X	X	X	X	X	Device Deselect	Continue the burst	
Cache Read with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	Self refresh is ILLEGAL; Start auto refresh	
	L	L	H	L	X	X	Precharge	Terminate burst	4
	L	L	H	H	BS	Row Address	Bank Activate	Activate a new DRAM row	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	Terminate burst; start a new read cycle	
	L	H	H	L	X	X	Burst Termination	Terminate burst	
	L	H	H	H	X	X	No Operation	Continue the burst	
	H	X	X	X	X	X	Device Deselect	Continue the burst	

1. CKE is assumed active (high) in the previous cycle for all entries. The current state is the state of the bank to which the command is being applied.
2. Both banks must be idle otherwise it is an illegal action.
3. If CKE is active (high) the ESDRAM will start the auto refresh (CBR) operation, if CKE is inactive (low) then the Self Refresh mode is entered.
4. The current state refers only to one of the banks. If BS selects this bank then the action specified in the table is taken. However, if BS selects the bank not being referenced by the current state then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered, otherwise there is a no operation.
6. The minimum and maximum row active time (t_{RAS}) must be satisfied.
7. The RAS to CAS delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the auto precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.
11. The precharge starts on the Nth clock following the issued command where N=burst length. Additional Read or Write commands may be issued prior to the completion of the burst to extend the time at which precharge begins.

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Current State Truth Table (Continued) (Notes: 1)

Current State	Command							Action	Notes
	CS	RAS	CAS	WE	A11	A10 - A0	Description		
Write with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate burst; start the precharge	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write, Write-AP	Terminate burst; start a new write cycle	11
	L	H	L	H	BS	Column	Read, Read-AP	Terminate burst; start a new read cycle	11
	L	H	H	L	X	X	Burst Termination	Terminate burst; start the precharge on the next clock	
	L	H	H	H	X	X	No Operation	Continue the burst	
	H	X	X	X	X	X	Device Deselect	Continue the burst	
Precharging	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	No operation; bank(s) idle after t_{RP}	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	Start a new read cycle	4
	L	H	H	L	X	X	Burst Termination	Terminates any ongoing burst bank(s) idle after t_{RP}	
	L	H	H	H	X	X	No Operation	No operation; bank(s) idle after t_{RP}	
	H	X	X	X	X	X	Device Deselect	No operation; bank(s) idle after t_{RP}	
Row Activating	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4, 10
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No operation; row active after t_{RCD}	
	L	H	H	H	X	X	No Operation	No operation; row active after t_{RCD}	
	H	X	X	X	X	X	Device Deselect	No operation; row active after t_{RCD}	

1. CKE is assumed active (high) in the previous cycle for all entries. The current state is the state of the bank to which the command is being applied.
2. Both banks must be idle otherwise it is an illegal action.
3. If CKE is active (high) the ESDRAM will start the auto refresh (CBR) operation, if CKE is inactive (low) then the Self Refresh mode is entered.
4. The current state refers only to one of the banks. If BS selects this bank then the action specified in the table is taken. However, if BS selects the bank not being referenced by the current state then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered, otherwise there is a no operation.
6. The minimum and maximum row active time (t_{RAS}) must be satisfied.
7. The RAS to CAS delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the auto precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.
11. The precharge starts on the Nth clock following the issued command where N=burst length. Additional Read or Write commands may be issued prior to the completion of the burst to extend the time at which precharge begins.

Current State Truth Table (Continued) (Notes: 1)

Current State	CS	RAS	CAS	WE	A11	A10 - A0	Description	Action	Notes
Write Recovering	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate burst; start the precharge	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	Start write; determine if auto precharge	9
	L	H	L	H	BS	Column	Read	Start read; determine if auto precharge	9
	L	H	H	L	X	X	Burst Termination	No operation; row active after t_{DPL}	
	L	H	H	H	X	X	No Operation	No operation; row active after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No operation; row active after t_{DPL}	
Write Recovering with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate burst; start the precharge	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4, 9
	L	H	L	H	BS	Column	Read	ILLEGAL	4, 9
	L	H	H	L	X	X	Burst Termination	No operation; precharge after t_{DPL}	
	L	H	H	H	X	X	No Operation	No operation; precharge after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No operation; precharge after t_{DPL}	
Refreshing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	Start a cache read (If auto refresh)	
	L	H	H	L	X	X	Burst Termination	No operation; idle after t_{RC}	
	L	H	H	H	X	X	No Operation	No operation; idle after t_{RC}	
	H	X	X	X	X	X	Device Deselect	No operation; idle after t_{RC}	

1. CKE is assumed active (high) in the previous cycle for all entries. The current state is the state of the bank to which the command is being applied.
2. Both banks must be idle otherwise it is an illegal action.
3. If CKE is active (high) the ESDRAM will start the auto refresh (CBR) operation, if CKE is inactive (low) then the Self Refresh mode is entered.
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5. If CKE is inactive (low) then the Power Down mode is entered, otherwise there is a no operation.
6. The minimum and maximum row active time (t_{RAS}) must be satisfied.
7. The RAS to CAS delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the auto precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.
11. The precharge starts on the Nth clock following the issued command where N=burst length. Additional Read or Write commands may be issued prior to the completion of the burst to extend the time at which precharge begins.

Current State Truth Table (Continued) (Notes: 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10 - A0	Description		
Mode Register Accessing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	No operation; idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No operation; idle after two clock cycles	

1. CKE is assumed active (high) in the previous cycle for all entries. The current state is the state of the bank to which the command is being applied.
2. Both banks must be idle otherwise it is an illegal action.
3. If CKE is active (high) the ESDRAM will start the auto refresh (CBR) operation, if CKE is inactive (low) then the Self Refresh mode is entered.
4. The current state refers only to one of the banks. If BS selects this bank then the action specified in the table is taken. However, if BS selects the bank not being referenced by the current state then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered, otherwise there is a no operation.
6. The minimum and maximum row active time (t_{RAS}) must be satisfied.
7. The RAS to CAS delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the auto precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.
11. The precharge starts on the Nth clock following the issued command where N=burst length. Additional Read or Write commands may be issued prior to the completion of the burst to extend the time at which precharge begins.

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Power Supply Voltage	-1.0 to +4.6	V	1
V_{DDQ}	Power Supply Voltage for Output	-1.0 to +4.6	V	1
V_{IN}	Input Voltage	-1.0 to +4.6	V	1
V_{OUT}	Output Voltage	-1.0 to +4.6	V	1
T_A	Operating Temperature (ambient)	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A= 0 to 70°C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V_{DDQ}	Supply Voltage for Output	2.3	—	V_{DD} + 0.3	V	1
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1
V_{IH2}	Input High Voltage for DQ pins	1.7	—	V_{DDQ} + 0.3	V	1, 2
V_{IL2}	Input Low Voltage for DQ pins	-0.3	—	0.7	V	1

1. All voltages referenced to V_{SS} and V_{SSQ}.
2. V_{IH2} (max) applies only when V_{DDQ} is less than or equal to V_{DD}.

Capacitance (T_A= 25°C, f=1MHz, V_{DD}= 3.3V $\pm$ 0.3V)

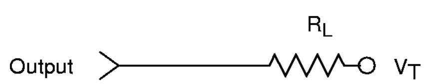
Symbol	Parameter	Min.	Typ	Max.	Units	Notes
C_{I1}	Input Capacitance (A0 - A11)	2.0	2.7	4.0	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CLK, CKE, DQM)	2.0	2.7	4.0	pF	
C_O	Output Capacitance (DQ0 - DQ15)	2.0	4.0	5.0	pF	

Output Characteristics (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Min.	Max.	Units	Notes
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ V_{DD}+0.3V), All Other Pins Not Under Test = 0V	—	±1	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ V_{DDQ}+0.3V)	—	±1	µA	
V_{OH}	Output Level (I_{OUT} = -2.0mA, V_{DDQ} = +3.3V ±0.3V)	2.4	V_{DDQ}	V	1
V_{OL}	Output Level (I_{OUT} = +2.0mA, V_{DDQ} = +3.3V ±0.3V)	0.0	0.4	V	1
V_{OH2}	Output Level (I_{OUT} = -2.0mA, V_{DDQ} = +2.5V ±0.2V)	2.1	V_{DDQ}	V	1
V_{OL2}	Output Level (I_{OUT} = +2.0mA, V_{DDQ} = +2.5V ±0.2V)	0.0	0.3	V	1

1. See DC output load circuit.

DC Output Load Circuit



For VDDQ = +3.3V,
V_{OH} (DC) = 2.4V, I_{OH} = -2mA
V_{OL} (DC) = 0.4V, I_{OL} = 2mA
V_T = 1.4V, R_L = 500Ω

For VDDQ = +2.5V,
V_{OH} (DC) = 2.1V, I_{OH} = -2mA
V_{OL} (DC) = 0.3V, I_{OL} = 2mA
V_T = 1.25V, R_L = 450Ω

Operating Currents (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

Parameter	Symbol	Test Condition	Value -6	Value -7.5	Value -10	Units	Notes
Operating Current (One Bank Active)	I_{CC1A}	BL = 1, CL = 1, Read or Write, CKE ≥ V_{IH}(min), t_{RC} = min., t_{CK} = min.	230	190	150	mA	1
	I_{CC1B}	BL = 1, CL = 2,3, Read or Write, CKE ≥ V_{IH}(min), t_{RC} = min, t_{CK} = 15ns (10ns for -7.5, 7.5ns for -6)	280	220	150	mA	
Standby Current in Power Down Mode (DRAM Precharged)	I_{CC2P}	CKE ≤ V_{IL}, t_{CK} = 15ns (10ns for -7.5, 7.5ns for -6) Input Change Every Two Cycles	2			mA	
	I_{CC2PS}	CKE ≤ V_{IL}, t_{CK} = Infinity No Input Change	1.5			mA	
Standby Current in Non-Power Down Mode (DRAM Pre-charged)	I_{CC2N}	CKE ≥ V_{IH}, t_{CK} = 15ns (10ns for -7.5, 7.5ns for -6)	65	60	50	mA	
	I_{CC2NS}	CKE ≥ V_{IH}, t_{CK} = Infinity	8			mA	
Device Deselected (DRAM Active)	I_{CC3N}	CKE ≥ V_{IH}, t_{CK} = 15ns (10ns for -7.5, 7.5ns for -6) Input Change Every Two Cycles	70	65	60	mA	
	I_{CC3P}	CKE ≤ V_{IL}, t_{CK} = 15ns (10ns for -7.5, 7.5ns for -6) Input Change Every Two Cycles	3	2.5	2	mA	
Burst Operating Current (Both Banks Active)	I_{CC4A}	BL = Full Page, CL = 1, Read or Write, t_{RC} = Infinity, t_{CK} = min.	110	90	70	mA	1,2
	I_{CC4B}	BL = Full Page, CL = 2,3, Read or Write, t_{RC} = Infinity, t_{CK} = 15ns (10ns for -7.5, 7.5ns for -6)	165	130	90	mA	
Auto (CBR) Refresh Current	I_{CC5F}	t_{CK} = 15ns (10ns for -7.5, 7.5ns for -6), t_{RC} = t_{RC}(min)	280	240	160	mA	3,4,5
	I_{CC5D}	t_{CK} = 15ns (10ns for -7.5, 7.5ns for -6), t_{RC} = 31.25 µs	15	15	10	mA	
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	1.5			mA	

1. The specified values are obtained with the outputs open.
2. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst read or burst write cycle.
3. The specified values are valid when addresses are changed no more than once during t_{CK}(min).
4. The specified values are valid when No Operation commands are registered on every rising clock edge during t_{RC}(min).
5. The specified values are valid when data inputs (DQ's) are stable during t_{RC}(min).

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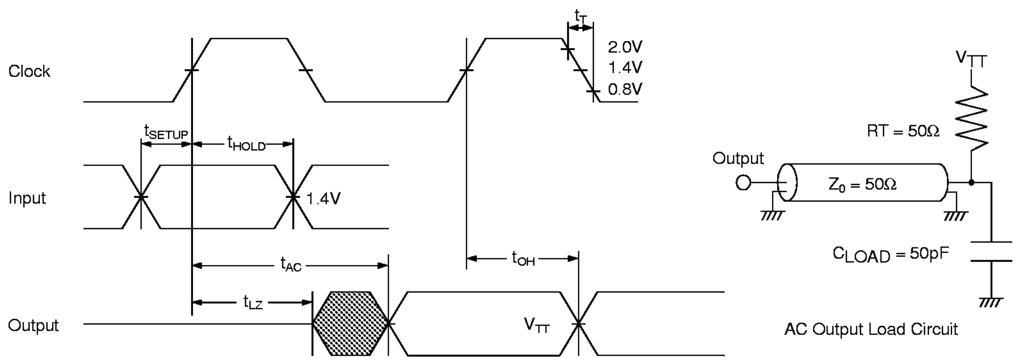
AC Characteristics

(T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

1. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of two Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0 V with the timing referenced to the 1.4 V (V_{TT}) cross-over point for V_{DDQ}=3.3V.
3. AC timing tests have V_{IL} = 0.7V and V_{IH} = 1.7V with the timing referenced to the1.25V (V_{TT}) crossover point for V_{DDQ}=2.5V.



4. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
5. AC measurements assume t_T=1ns.
6. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. The C_{LOAD} value is 30pF for the -6ns speed grade.

Clock and Clock Enable Parameters

Symbol	Parameter	-6		-7.5		-10		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CK2}	Clock Cycle Time, CAS Latency = 2, 3	6	**166MHz**	7.5	**133MHz**	10	**100MHz**	ns	
t_{CK1}	Clock Cycle Time, CAS Latency = 1	12	**83MHz**	15	**66MHz**	20	**50MHz**	ns	
t_{AC2}	Clock Access Time, CAS Latency = 2, 3	—	4.3	—	4.5	—	5	ns	1, 2
t_{AC1}	Clock Access Time, CAS Latency = 1	—	10.5	—	12	—	15	ns	1, 2
t_{CKH2}	Clock High Pulse Width, CAS Latency = 2, 3	2.4	—	2.8	—	3.5	—	ns	3
t_{CKH1}	Clock High Pulse Width, CAS Latency = 1	4	—	5	—	6	—	ns	3
t_{CKL2}	Clock Low Pulse Width, CAS Latency = 2, 3	2.4	—	2.8	—	3.5	—	ns	3
t_{CKL1}	Clock Low Pulse Width, CAS Latency = 1	4	—	5	—	6	—	ns	3
t_{CKES}	Clock Enable Set-up Time	2	—	2	—	2.5	—	ns	
t_{CKEH}	Clock Enable Hold Time	1	—	1	—	1	—	ns	
t_{CKESP}	CKE Set-up Time (Power Down mode)	2	—	2	—	2.5	—	ns	
t_T	Transition Time (Rise and Fall)	—	4	—	4	—	4	ns	

1. Access time is measured at 1.4V (V_{DDQ}=3.3V) and 1.25V (V_{DDQ}=2.5V). See AC output circuit.
2. Access time is measured assuming a clock rise time of 1ns. If clock rise time is longer than 1ns, then (trise/2-0.5)ns should be added to the parameter.
3. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, then other AC parameters under consideration should be compensated by an additional [(trise+tfall)/2-1]ns.

Common Parameters

Symbol	Parameter	-6		-7.5		-10		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CS}	Command Setup Time	2	—	2	—	2.5	—	ns	
t_{CH}	Command Hold Time	1	—	1	—	1	—	ns	
t_{AS}	Address and Bank Select Set-up Time	2	—	2	—	2.5	—	ns	
t_{AH}	Address and Bank Select Hold Time	1	—	1	—	1	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	12	—	15	—	20	—	ns	
t_{RC}	Bank Cycle Time	36	120000	37.5	120000	50	120000	ns	
t_{RAS}	Active Command Period	18	120000	22.5	120000	30	120000	ns	
t_{RP}	Precharge Time	14	—	15	—	20	—	ns	
t_{RRD}	Bank to Bank Delay Time	12	—	15	—	20	—	ns	
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Same Bank)	6	—	7.5	—	10	—	ns	

Refresh Cycle

Symbol	Parameter	-6		-7.5		-10		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Refresh Period	—	64	—	64	—	64	ms	1, 2
t_{SREX}	Self Refresh Exit Time	2CLK + t_{RC}	—	2CLK + t_{RC}	—	2CLK + t_{RC}	—	ns	3

1. 2048 cycles.
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake-up” the device.
3. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.

Read Cycle

Symbol	Parameter	-6		-7.5		-10		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{OH1}	Data Out Hold Time (CL=1)	3	—	3	—	3	—	ns	
t_{OH2}	Data Out Hold Time (CL=2, 3)	2	—	2	—	2	—	ns	
t_{LZ}	Data Out to Low Impedance Time	0	—	0	—	0	—	ns	
t_{HZ1}	Data Out to High Impedance Time (CL=1)	—	7	—	7.5	—	8	ns	1
t_{HZ2}	Data Out to High Impedance Time (CL=2, 3)	—	4.3	—	4.5	—	5	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	—	2	—	2	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

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Write Cycle

Symbol	Parameter	-6		-7.5		-10		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{DS}	Data In Set-up Time	2	—	2	—	2.5	—	ns	
t_{DH}	Data In Hold Time	1	—	1	—	1	—	ns	
t_{DPL}	Data input to Precharge	6	—	7.5	—	10	—	ns	
t_{DAL}	Data In to Active/Refresh	22	—	24	—	30	—	ns	1
t_{DQW}	DQM Write Mask Latency	0	—	0	—	0	—	CLK	

1. t_{DAL} must satisfy t_{DPL} + t_{RP}.

Clock Frequency and Latency

Symbol	Parameter	Speed Sort						Units	Notes
		-6		-7.5		-10			
fCK	**Clock Frequency**	**166**	**83**	**133**	**66**	**100**	**50**	**MHz**	
t_{CK}	Clock Cycle Time	6	12	7.5	15	10	20	ns	
t_{AA}	CAS Latency	2	1	2	1	2	1	t_{CK}	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	2	1	2	1	2	1	t_{CK}	
t_{RL}	RAS Latency	4	2	4	2	4	2	t_{CK}	
t_{RC}	Bank Cycle Time	6	3	5	3	5	3	t_{CK}	
t_{RAS}	Minimum Bank Active Time	3	2	3	2	3	2	t_{CK}	
t_{RP}	Precharge Time	3	2	2	1	2	1	t_{CK}	
t_{DPL}	Data In to Precharge	1	1	1	1	1	1	t_{CK}	
t_{DAL}	Data In to Active/Refresh	4	2	3	2	3	2	t_{CK}	
t_{RRD}	Bank to Bank Delay Time	2	1	2	1	2	1	t_{CK}	
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	1	1	1	1	1	t_{CK}	
t_{WL}	Write Latency	0	0	0	0	0	0	t_{CK}	
t_{DQW}	DQM Write Mask Latency	0	0	0	0	0	0	t_{CK}	
t_{DQZ}	DQM Data Disable Latency	2	2	2	2	2	2	t_{CK}	
t_{CSL}	Clock Suspend Latency	1	1	1	1	1	1	t_{CK}	

Timing Diagrams

NOTE: Some CL=2 diagrams reflect timing up to 133MHz. For -6ns speed grade operation at 166MHz, an additional cycle may be required to satisfy timing specifications. See Clock Frequency and Latency table on preceeding Page

Reference List of Timing Diagrams

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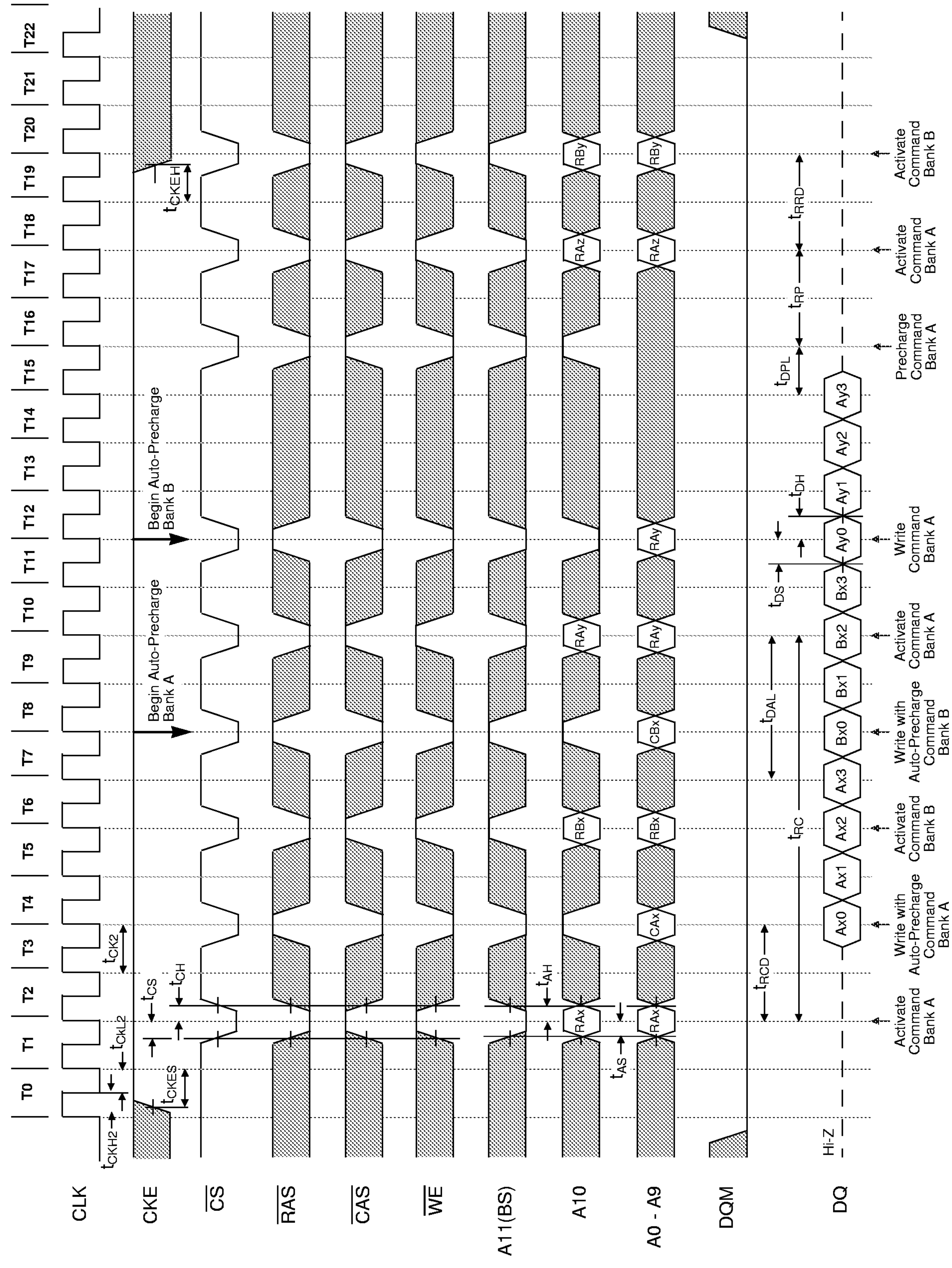
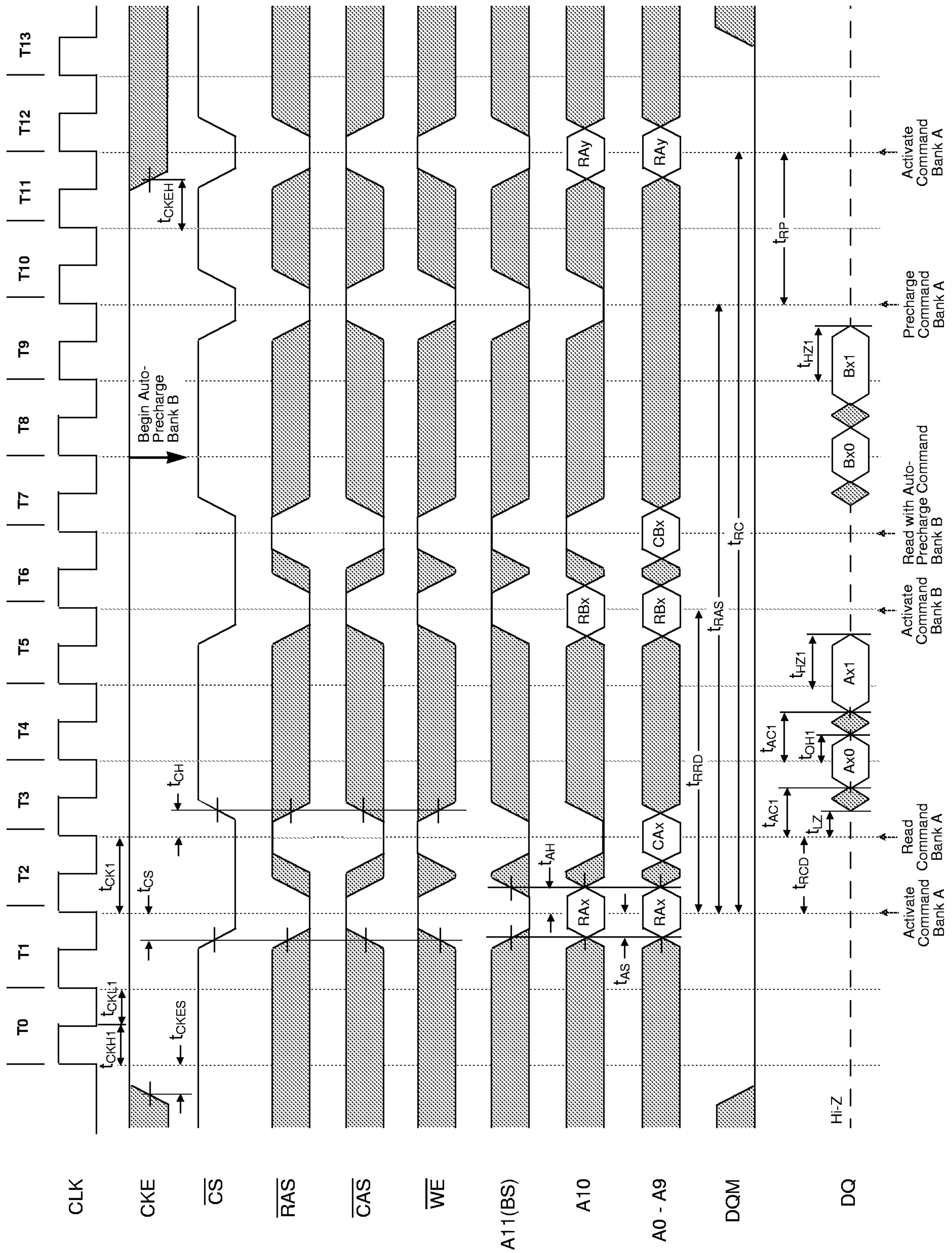
AC Parameters for Write Timing

Burst Length = 4, CAS Latency = 2



AC Parameters for Read Timing (1 of 2)

Burst Length = 2, CAS Latency = 1



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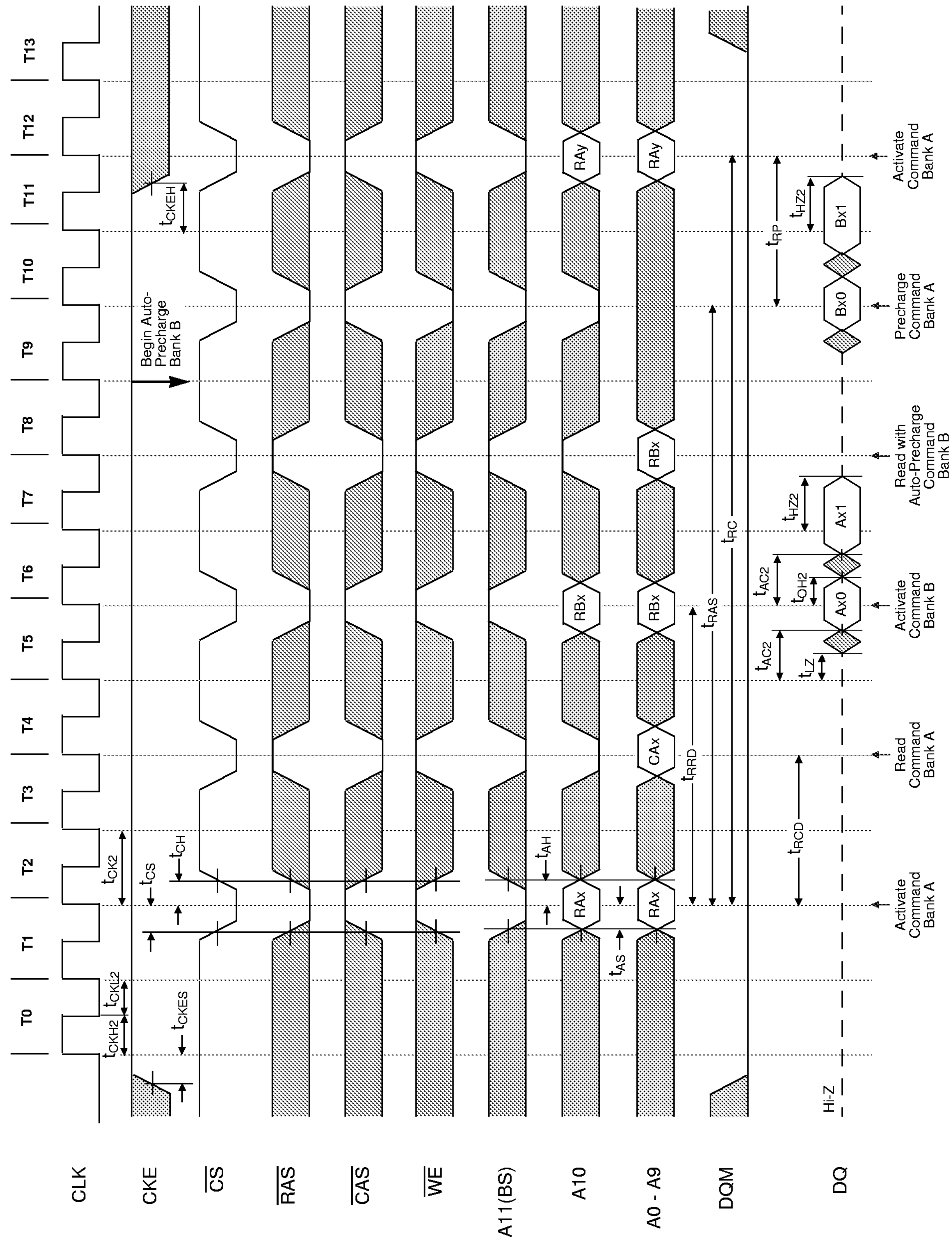
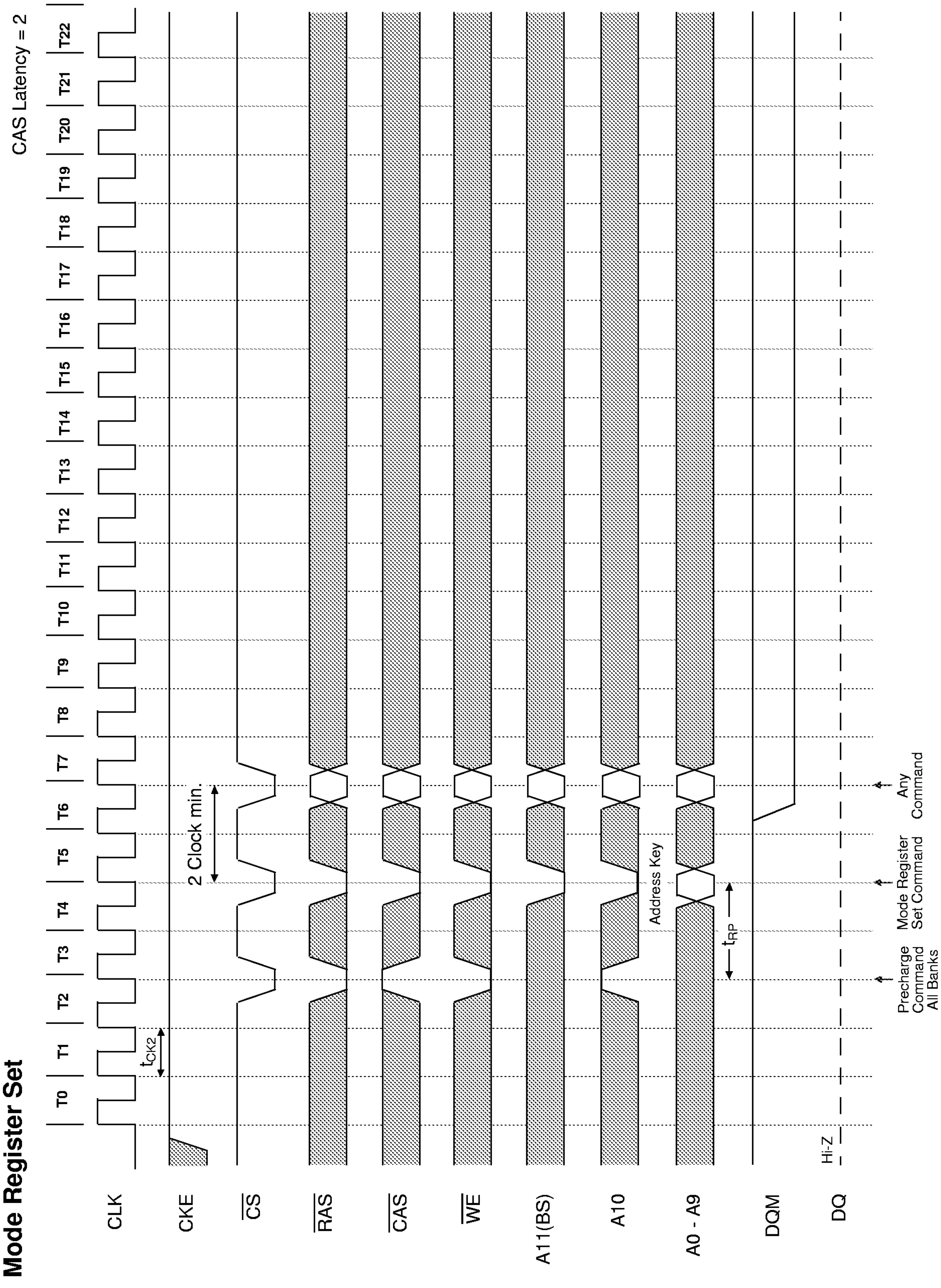
AC Parameters for Read Timing (2 of 2)

Burst Length = 2, CAS Latency = 2



Mode Register Set



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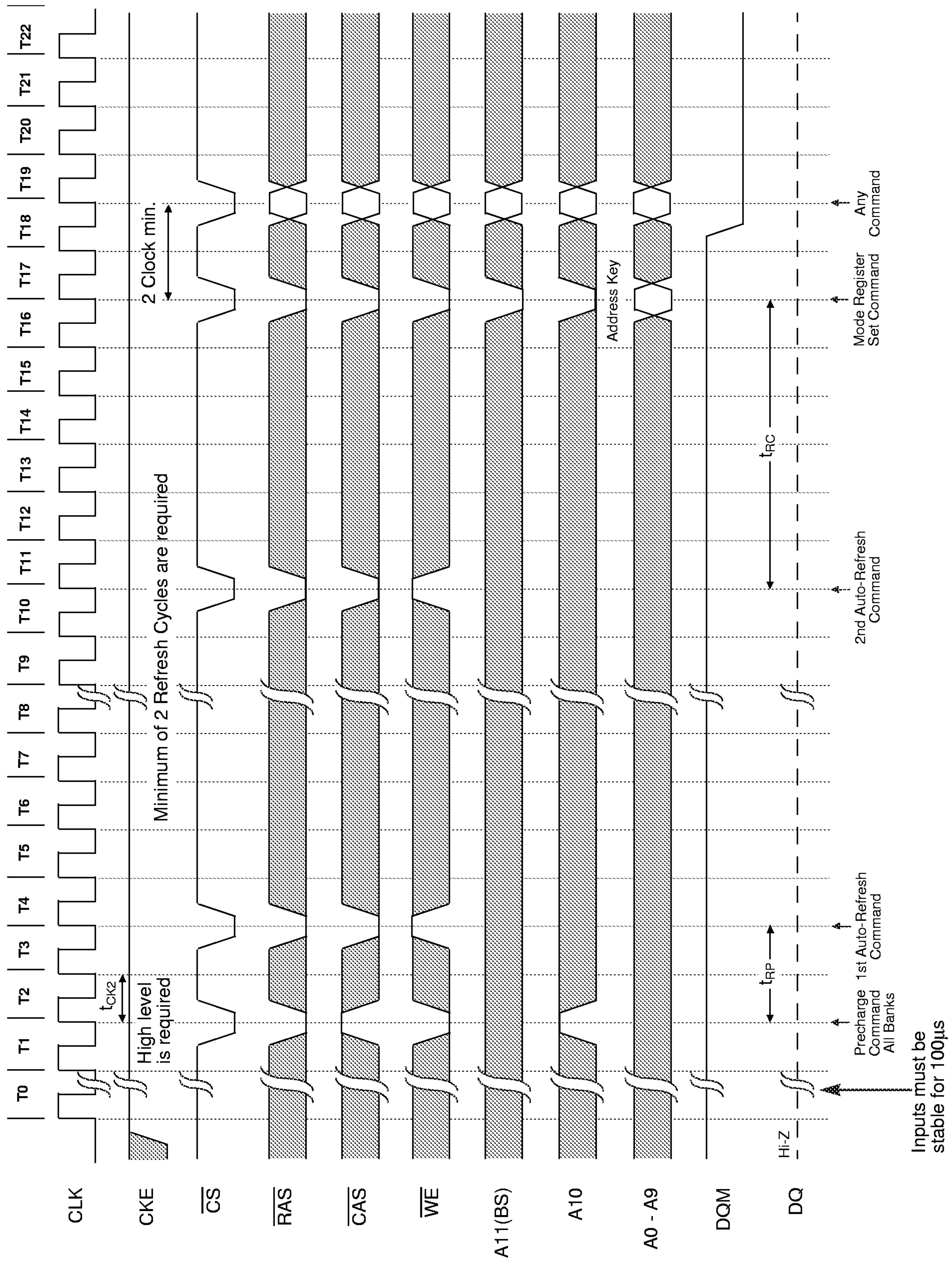
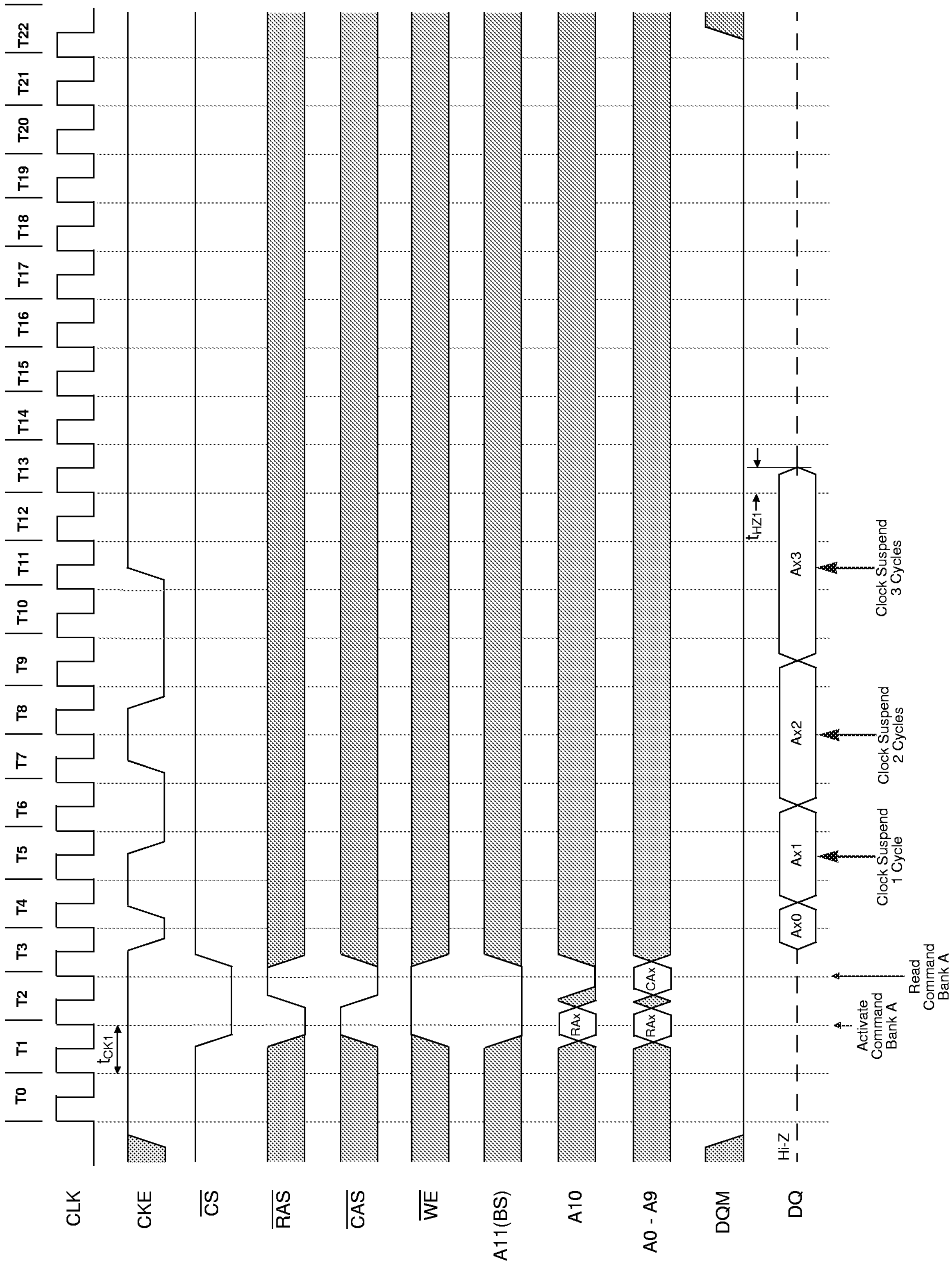
Power on Sequence and Auto-Refresh (CBR)



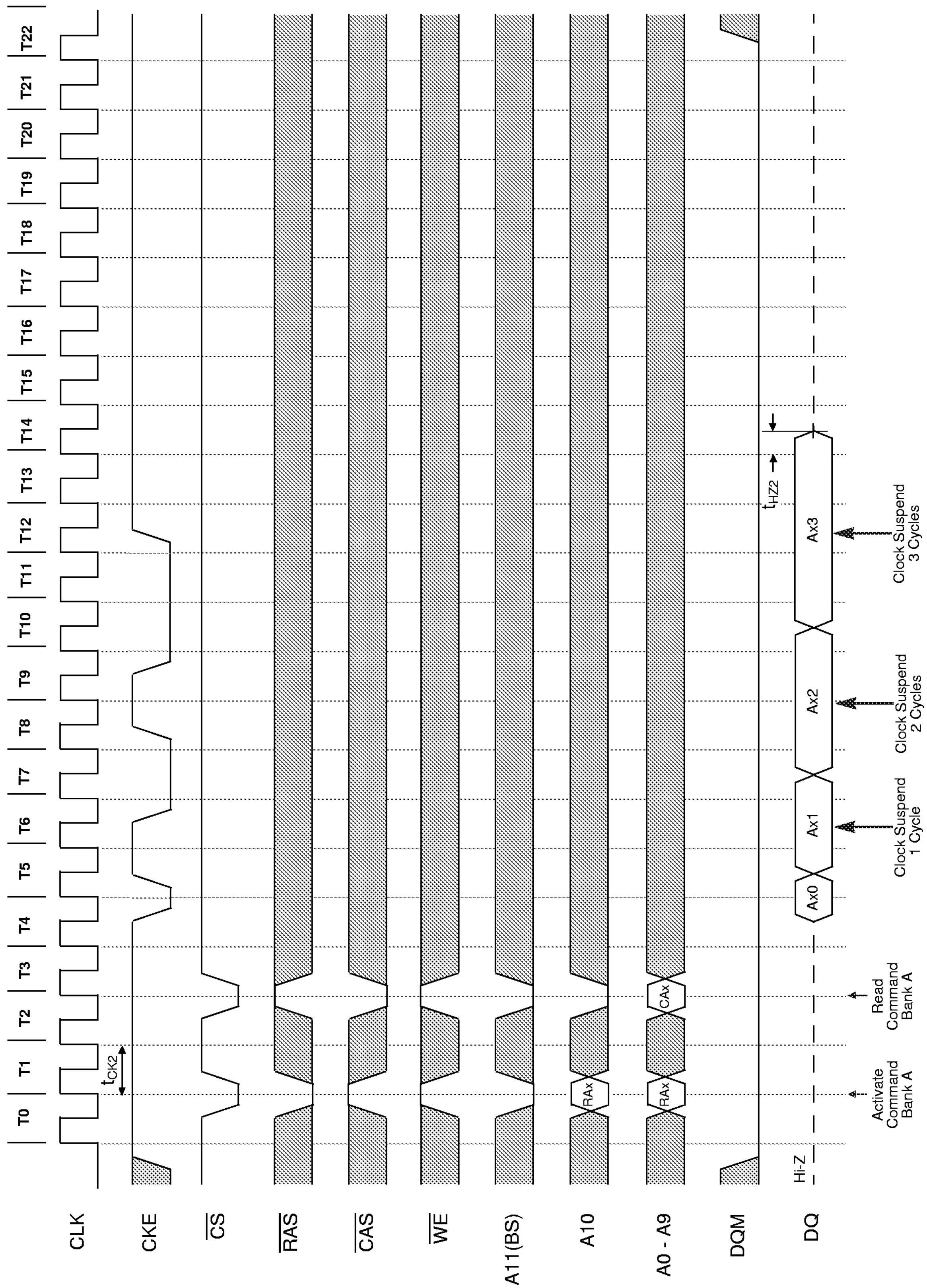
Clock Suspension During Burst Read (Using CKE) (1 of 2)

Burst Length = 4, CAS Latency = 1



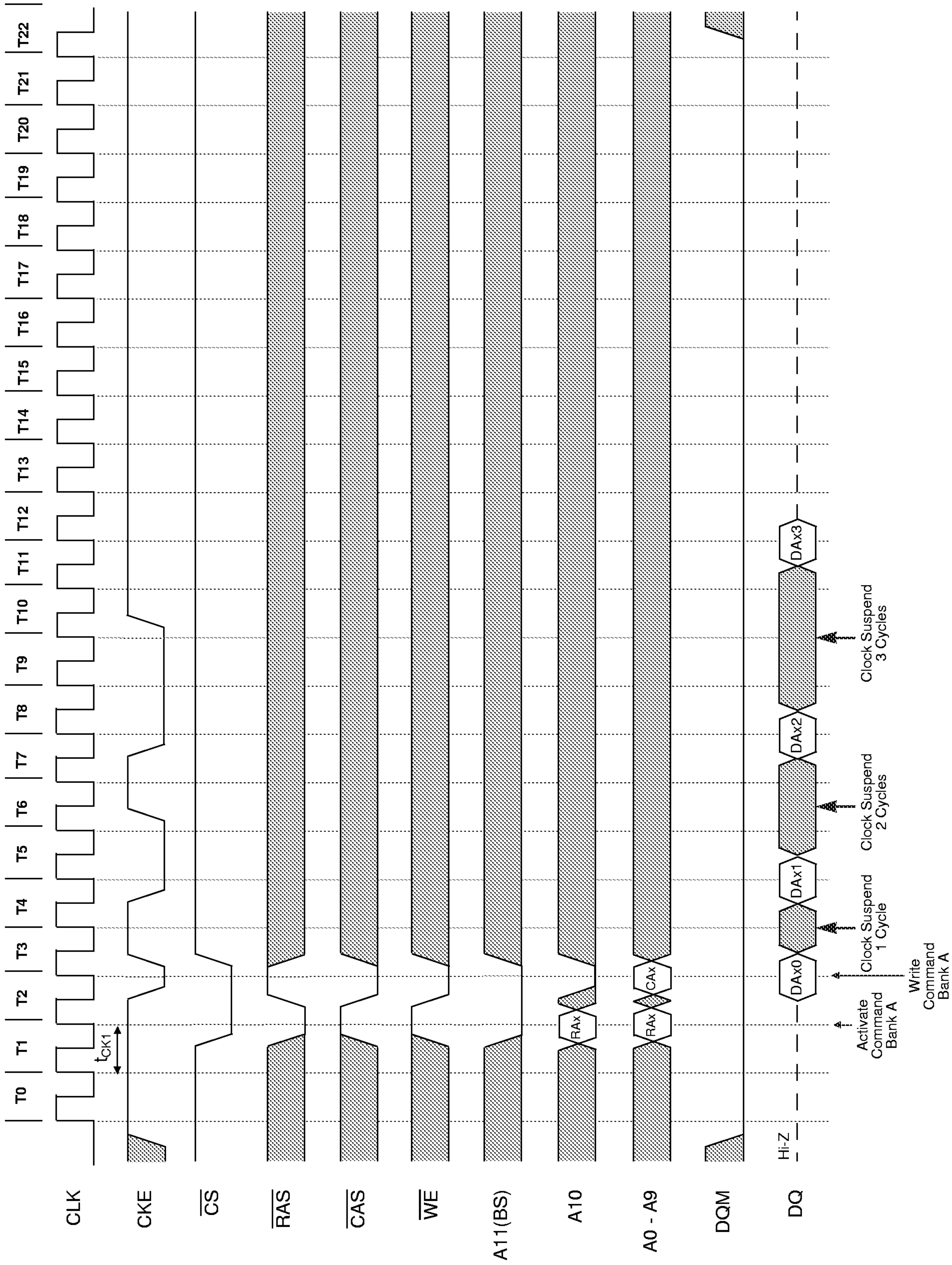
Clock Suspension During Burst Read (Using CKE) (2 of 2)

Burst Length = 4, CAS Latency = 2



Clock Suspension During Burst Write (Using CKE) (1 of 2)

Burst Length = 4, CAS Latency = 1



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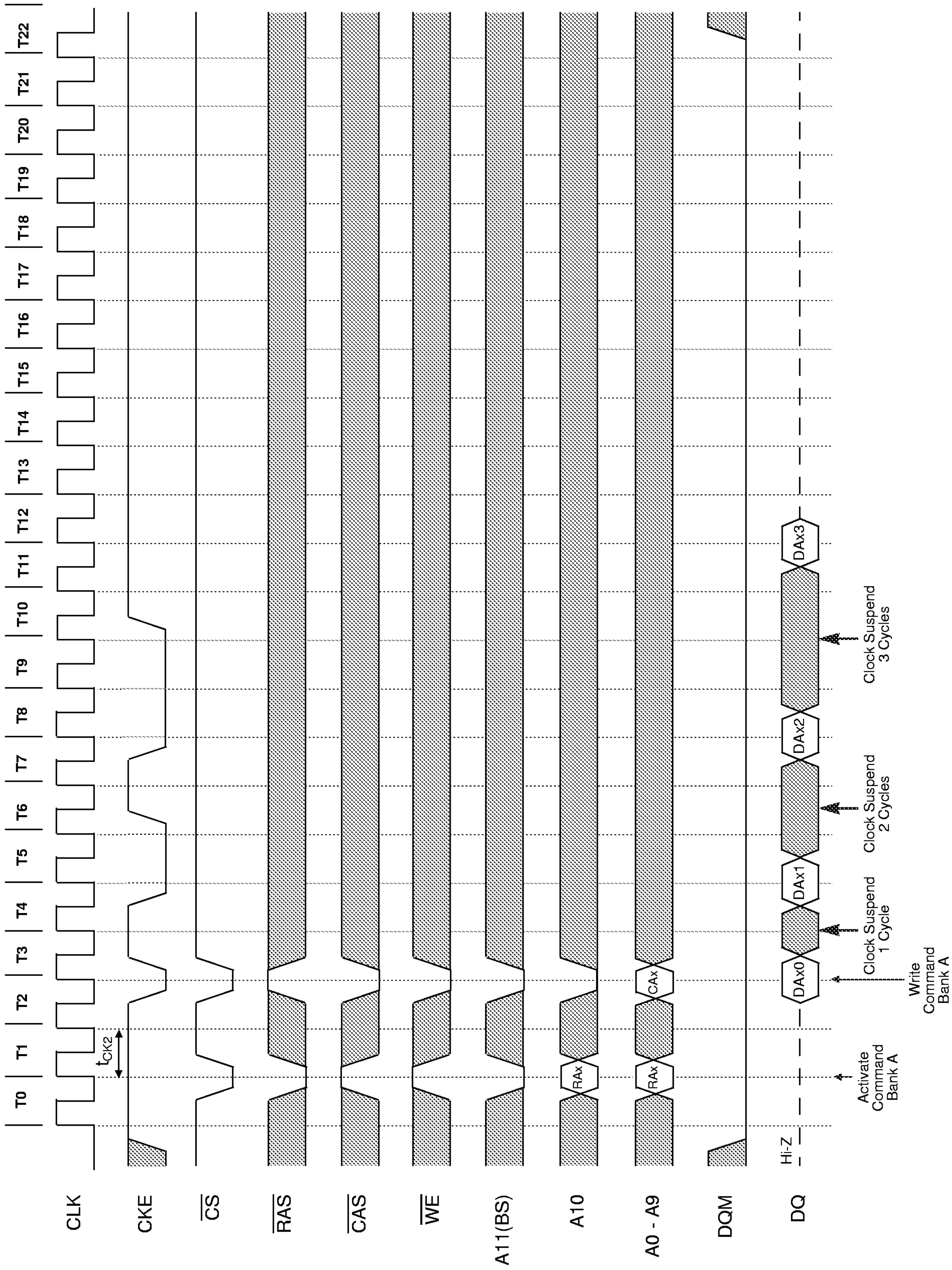
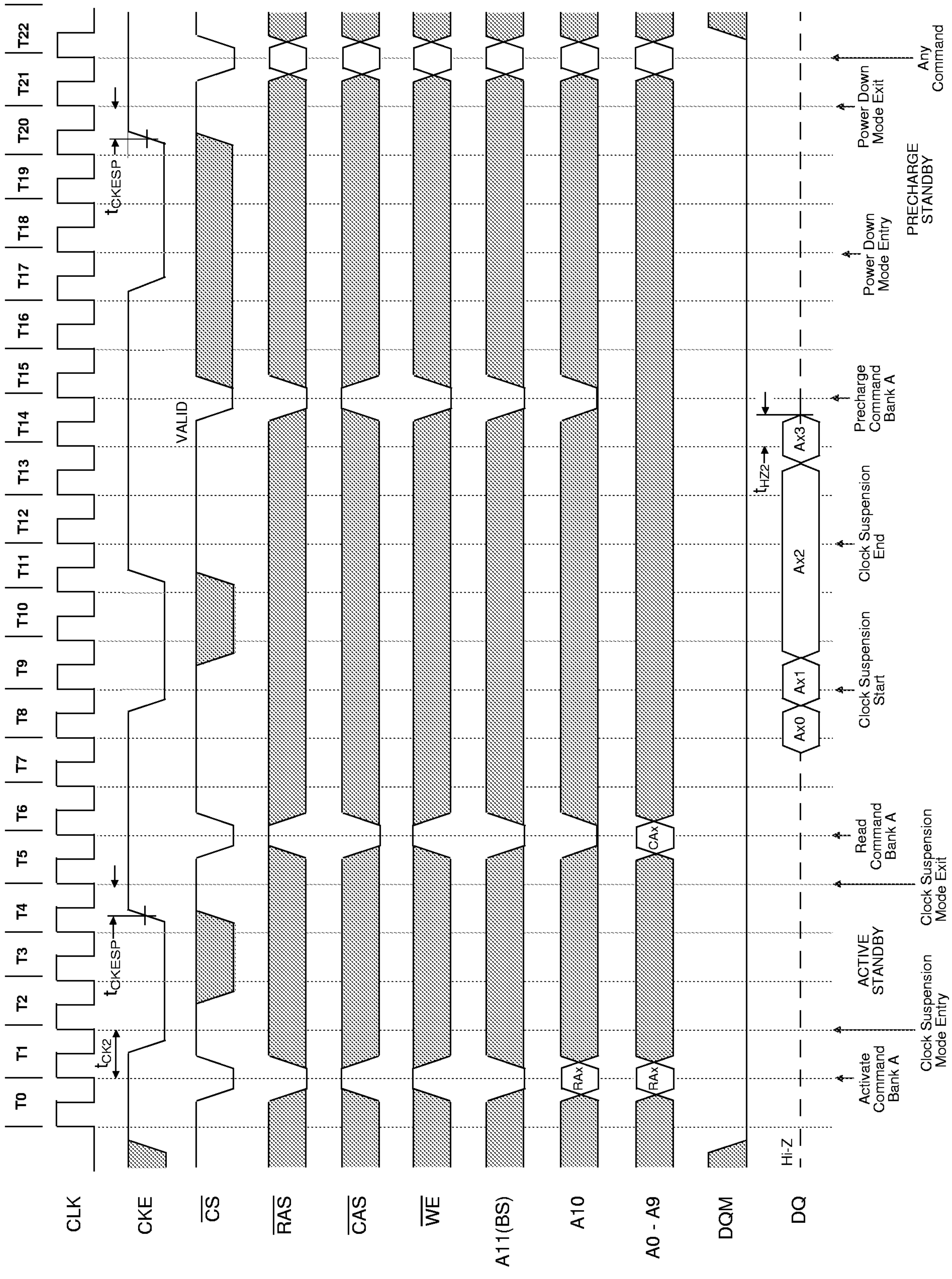
Clock Suspension During Burst Write (Using CKE) (2 of 2)

Burst Length = 4, CAS Latency = 2



Power Down Mode and Clock Suspend

Burst Length = 4, CAS Latency = 2



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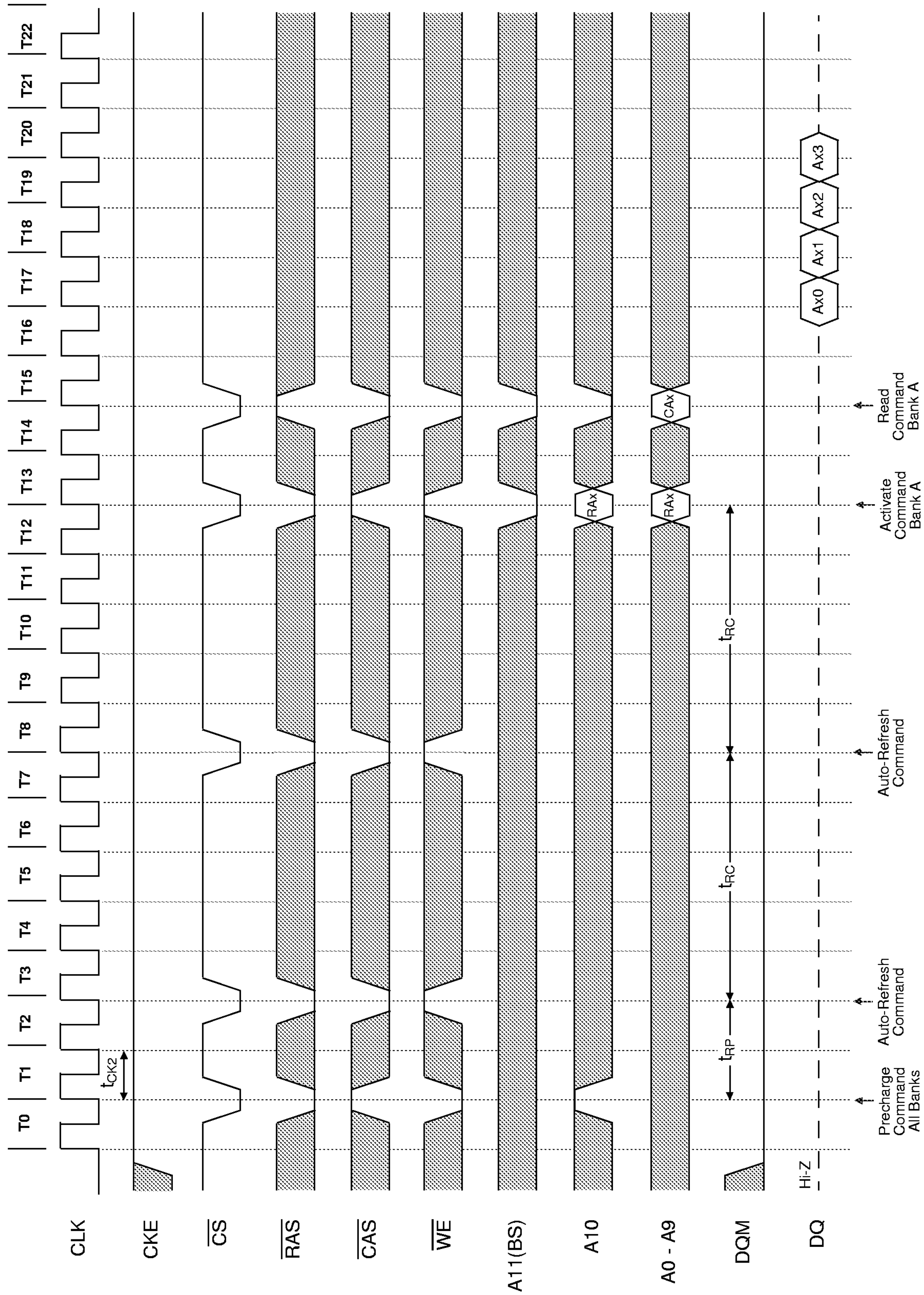
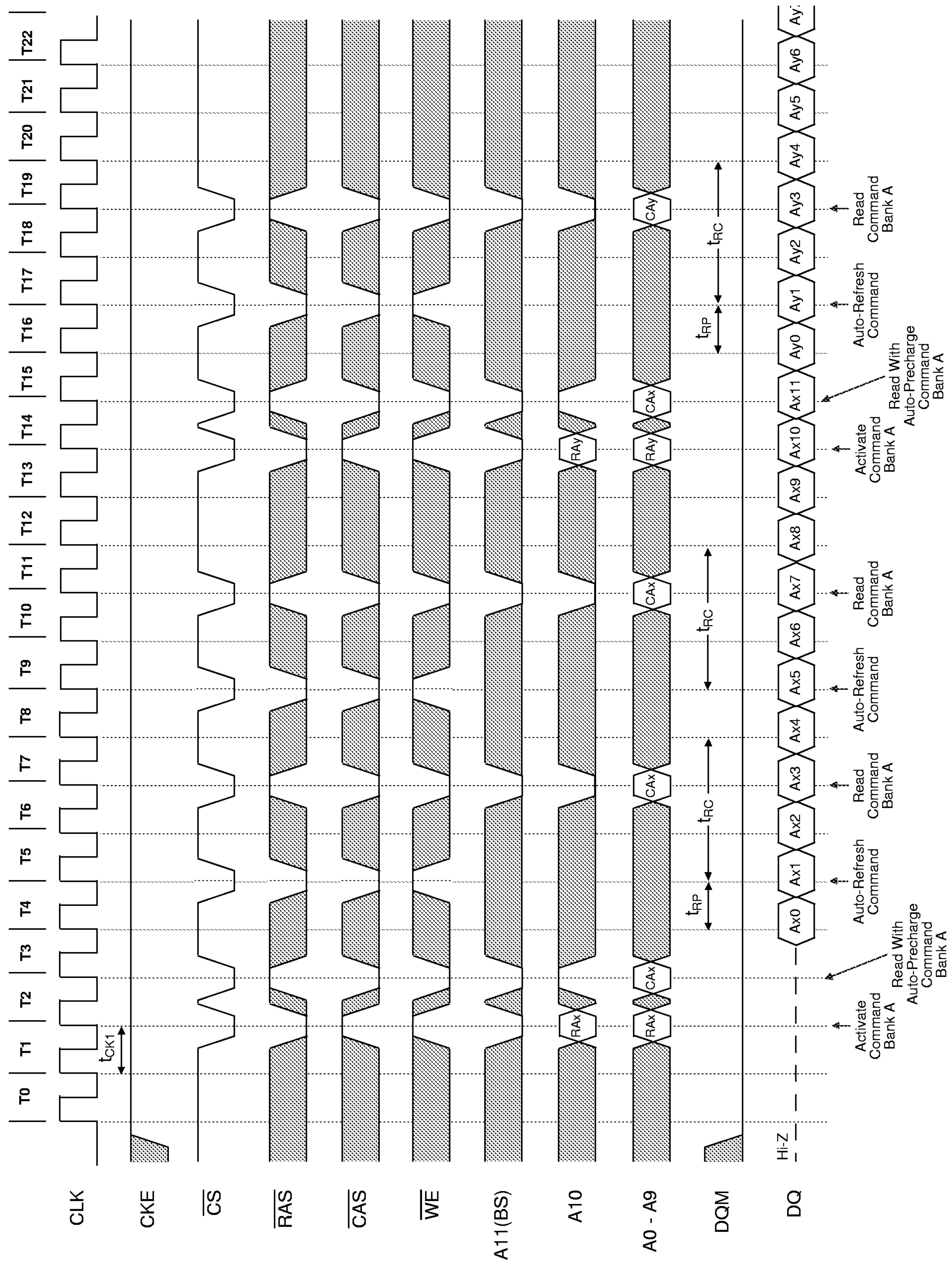
Auto Refresh (CBR)

Burst Length = 4, CAS Latency = 2



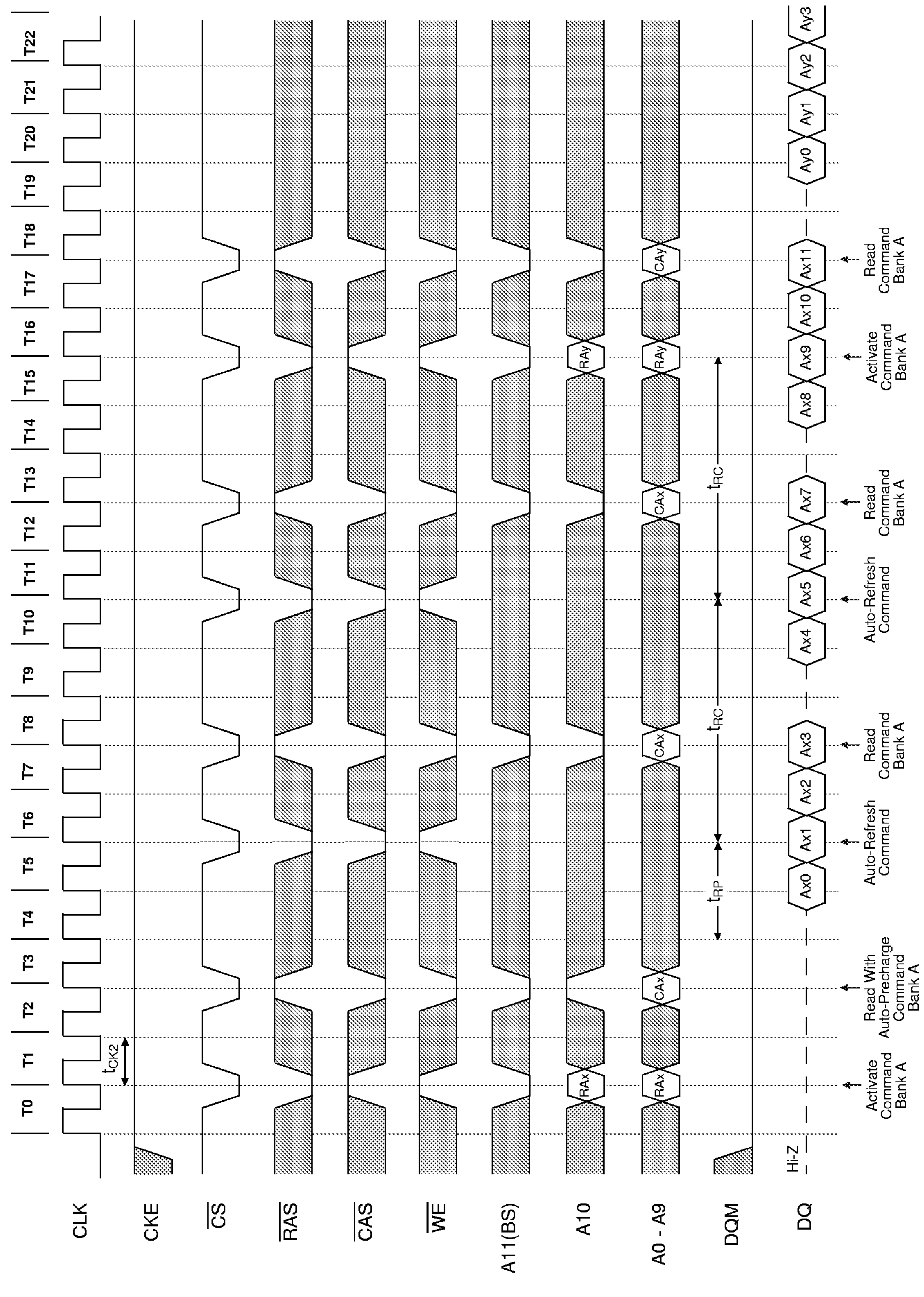
Hidden Auto Refresh (1 of 2)

Burst Length = 4, CAS Latency = 1

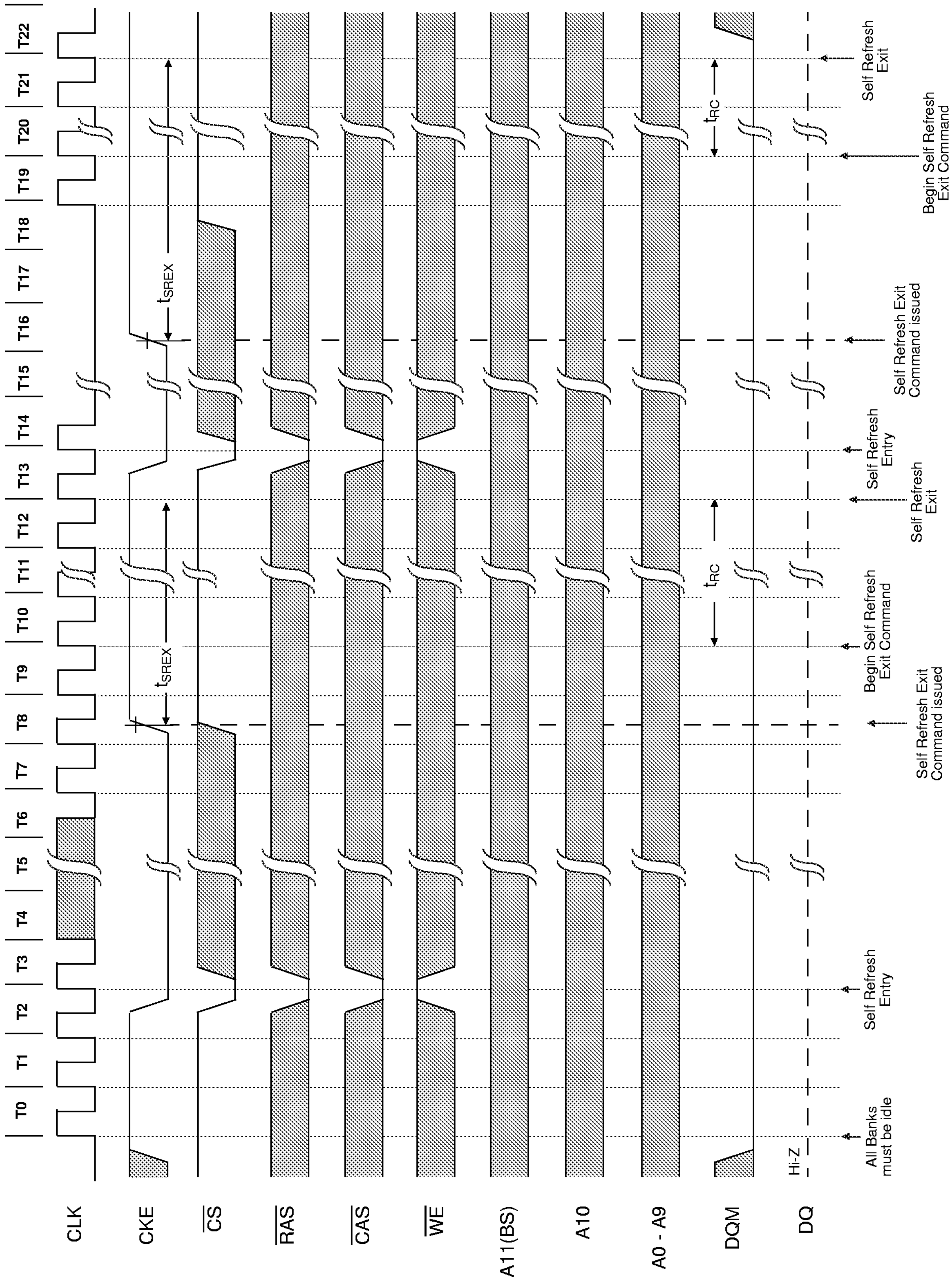


Hidden Auto Refresh (2 of 2)

Burst Length = 4, CAS Latency = 2

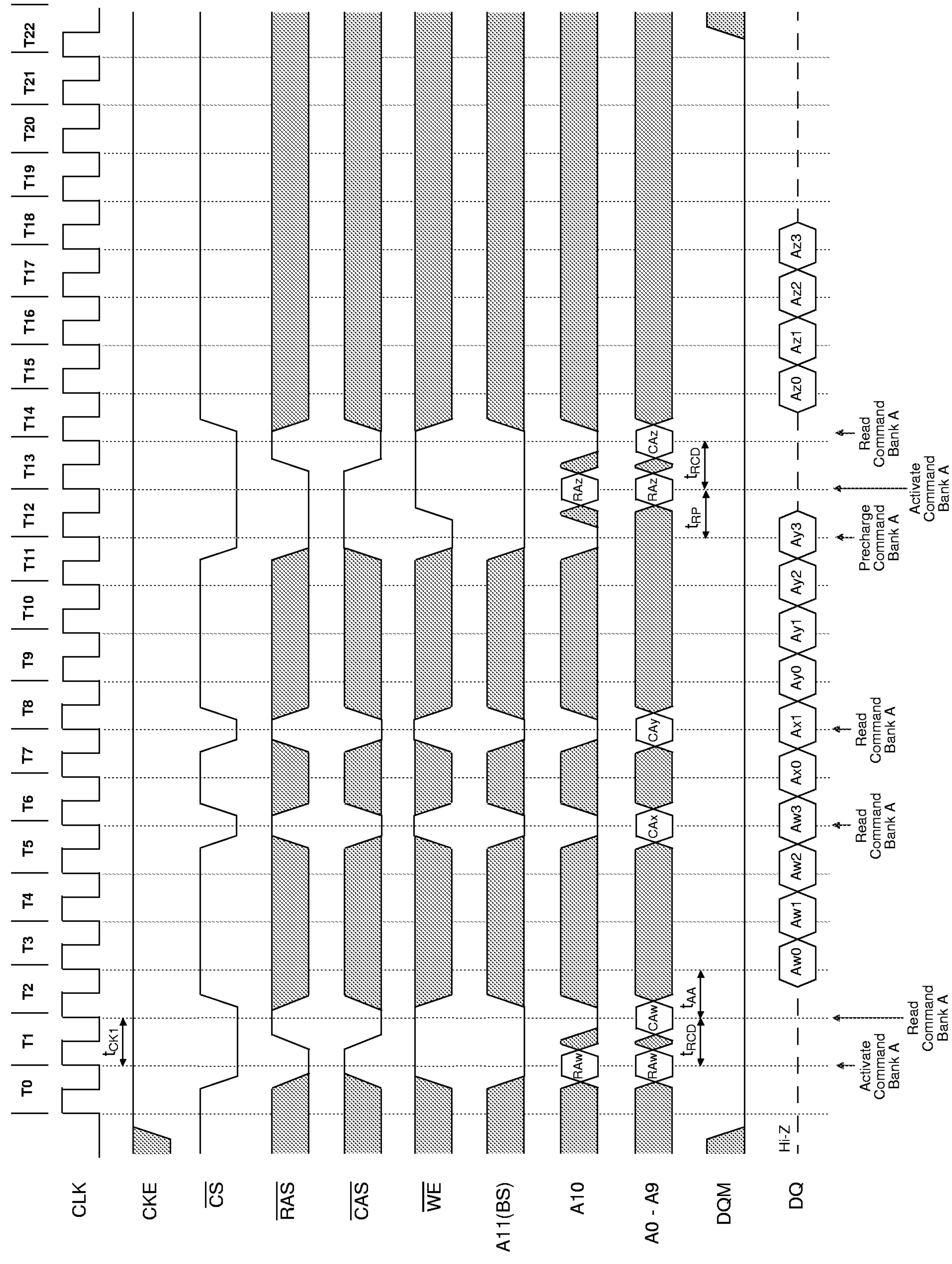


Self Refresh (Entry and Exit) ***Note: The CLK signal must be established prior to CKE returning high.



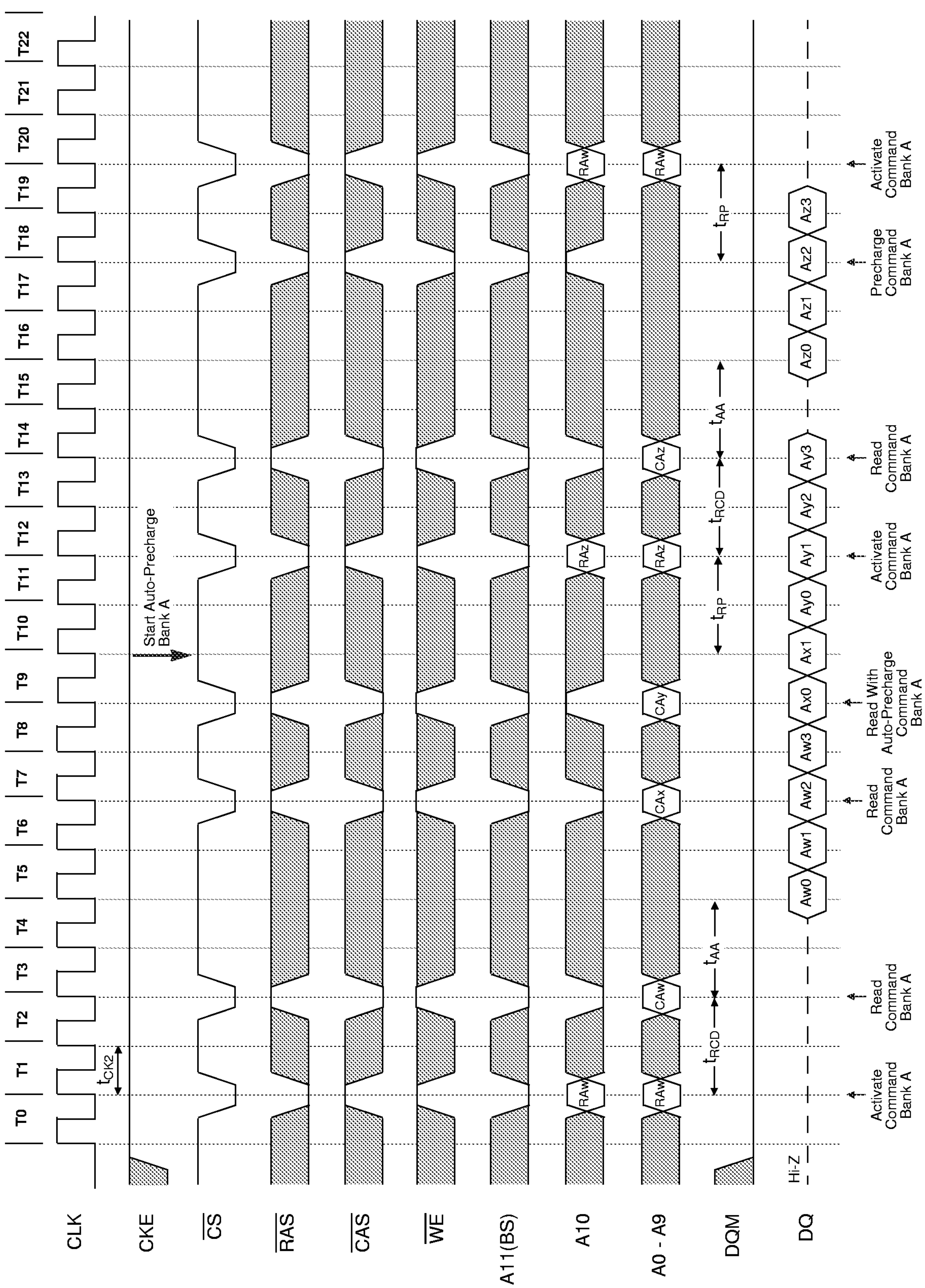
Random Column Read (Page within same Bank) (1 of 2)

Burst Length = 4, CAS Latency = 1

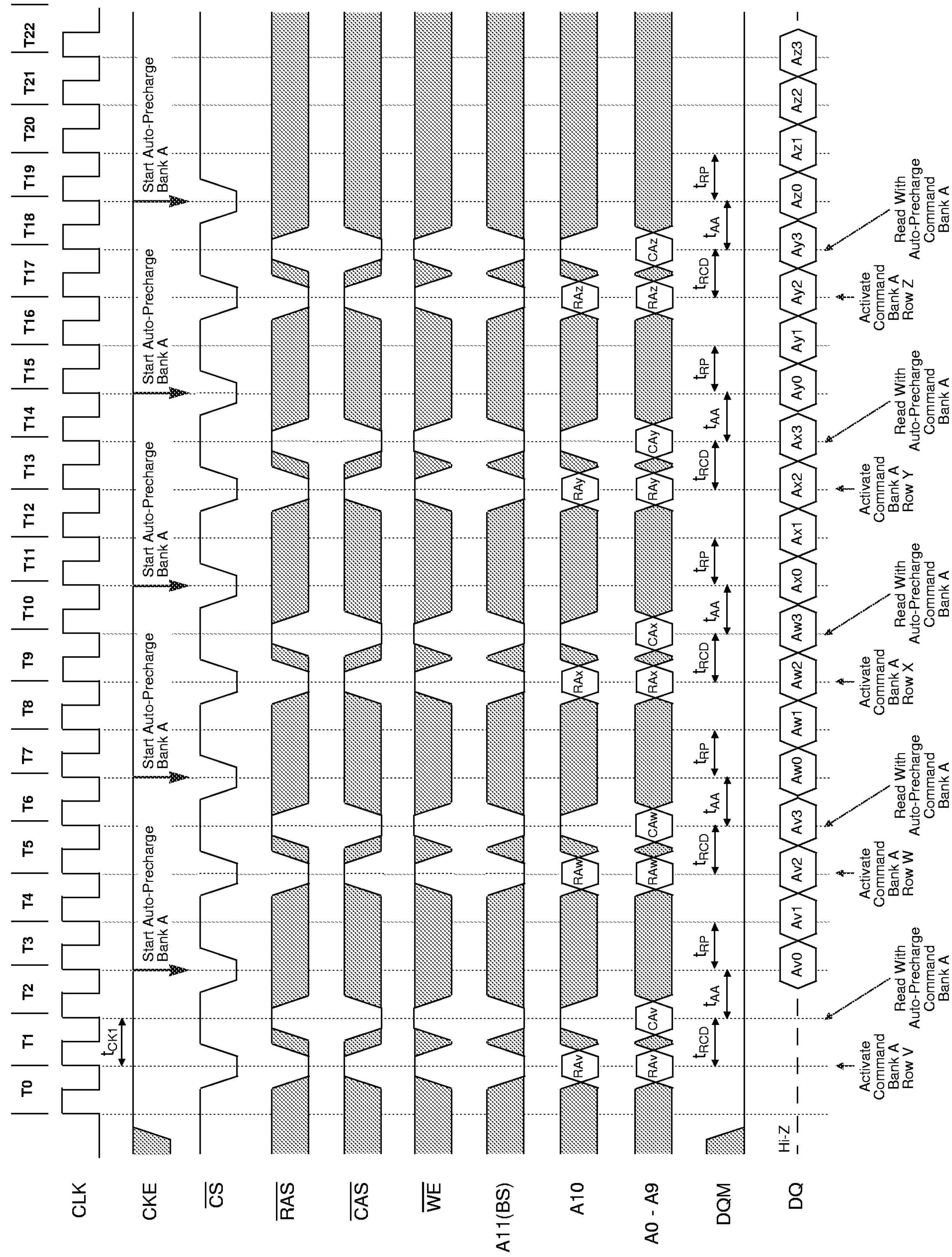


Random Column Read (Page within same Bank) (2 of 2)

Burst Length = 4, CAS Latency = 2

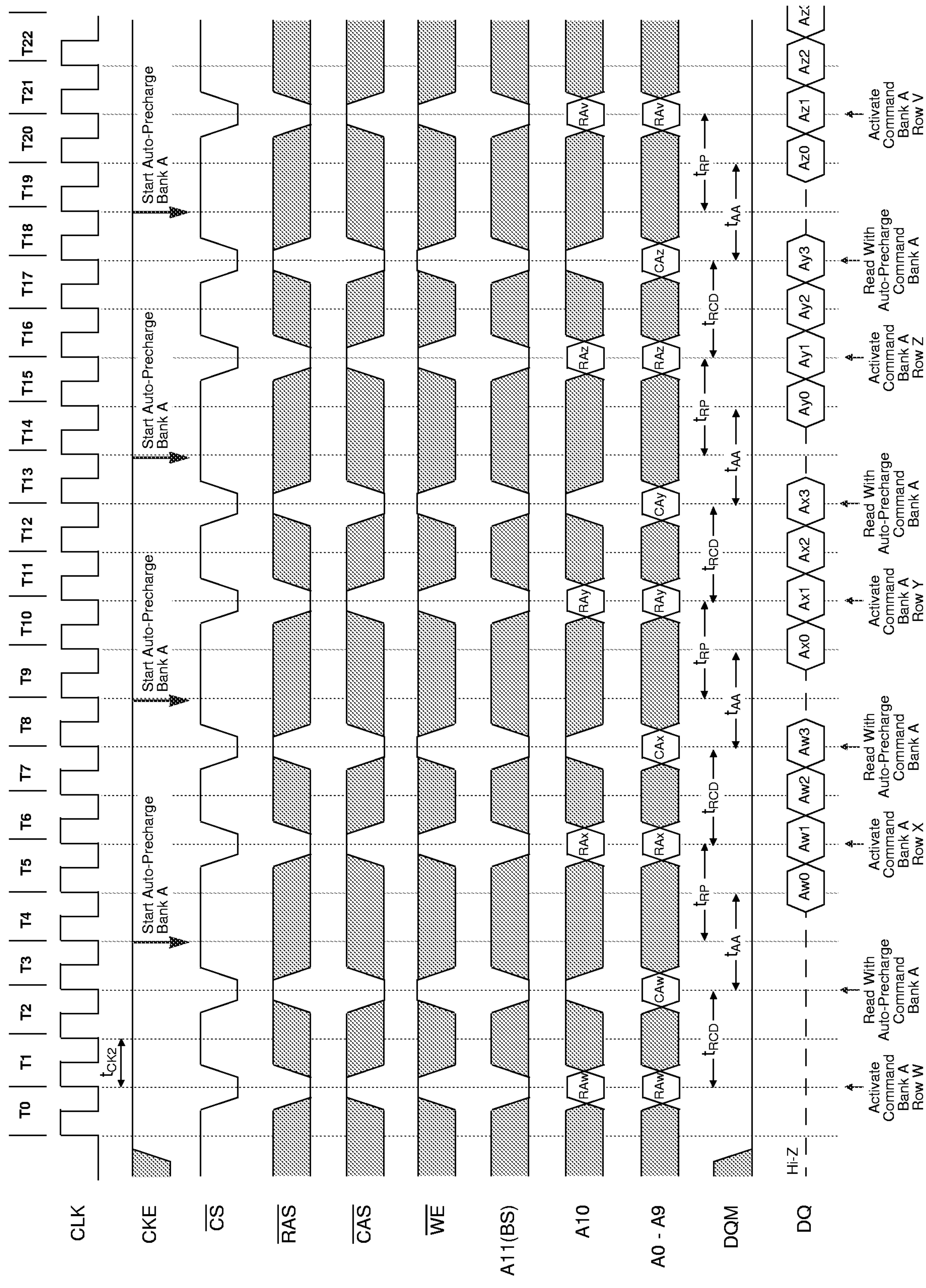


Pipelined Random Row Reads (Page within same Bank) (1 of 2)



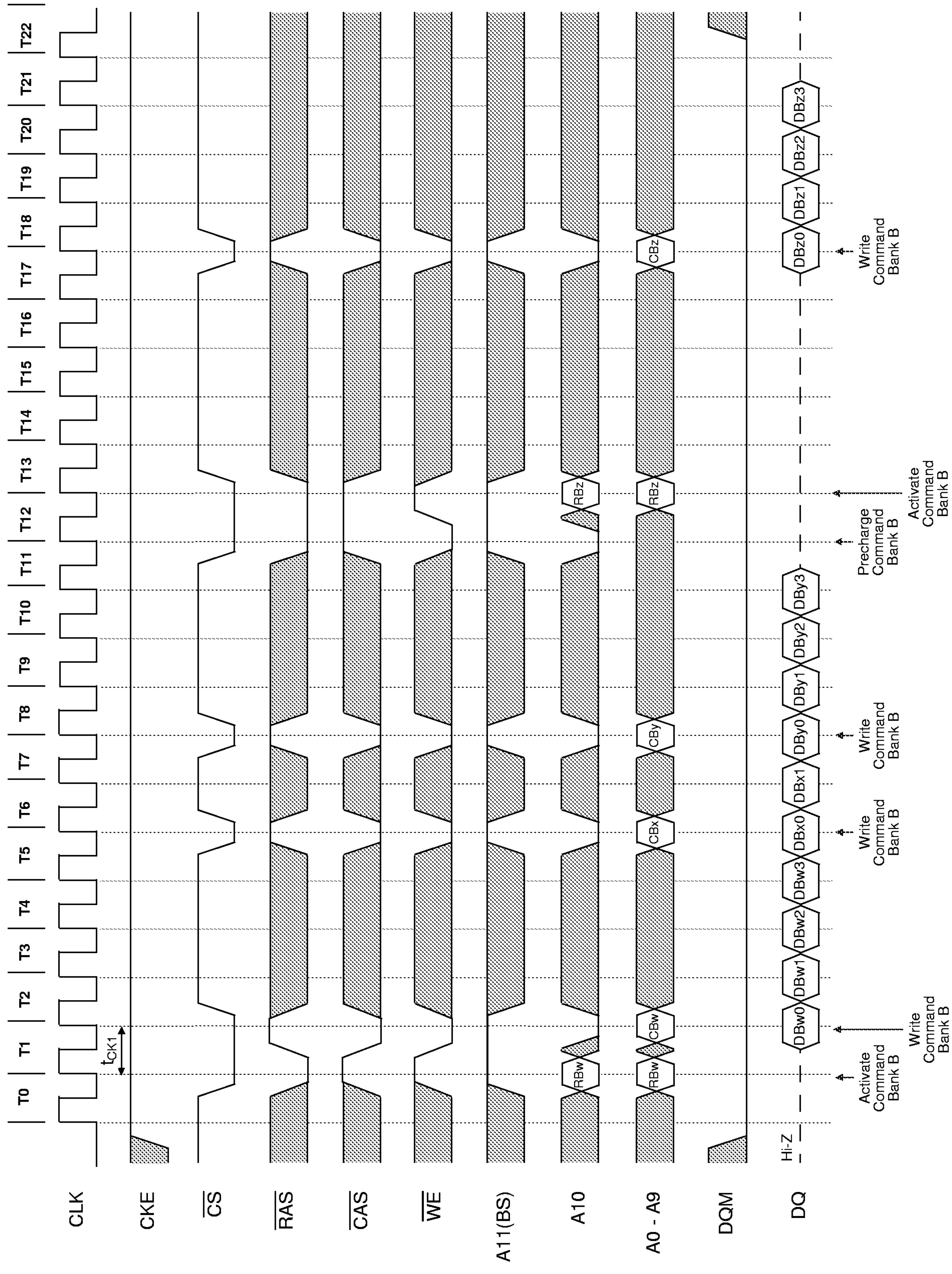
Pipelined Random Row Reads (Page within same Bank) (2 of 2)

Burst Length = 4, CAS Latency = 2



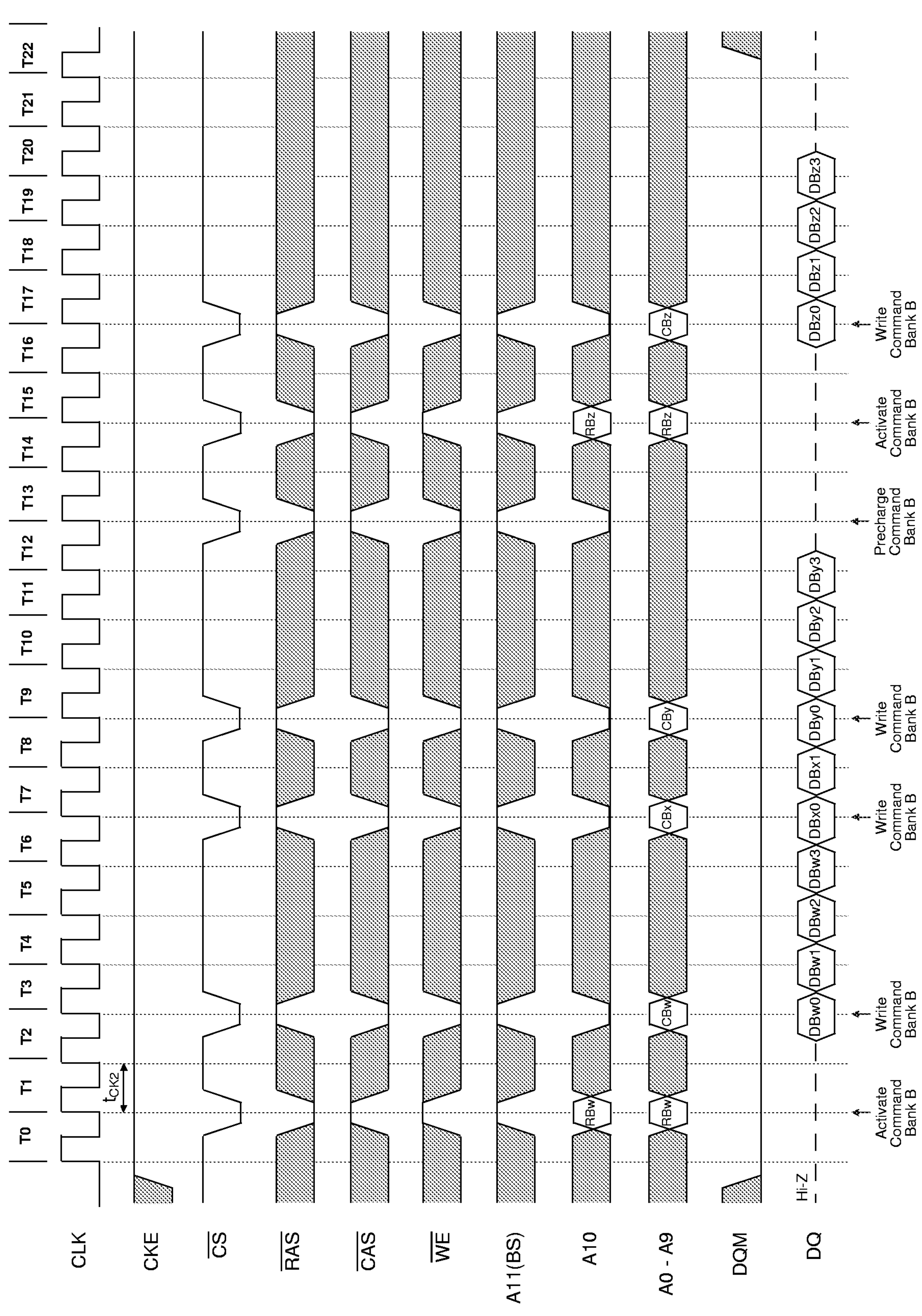
Random Column Write (Page within same Bank) (1 of 2)

Burst Length = 4, CAS Latency = 1



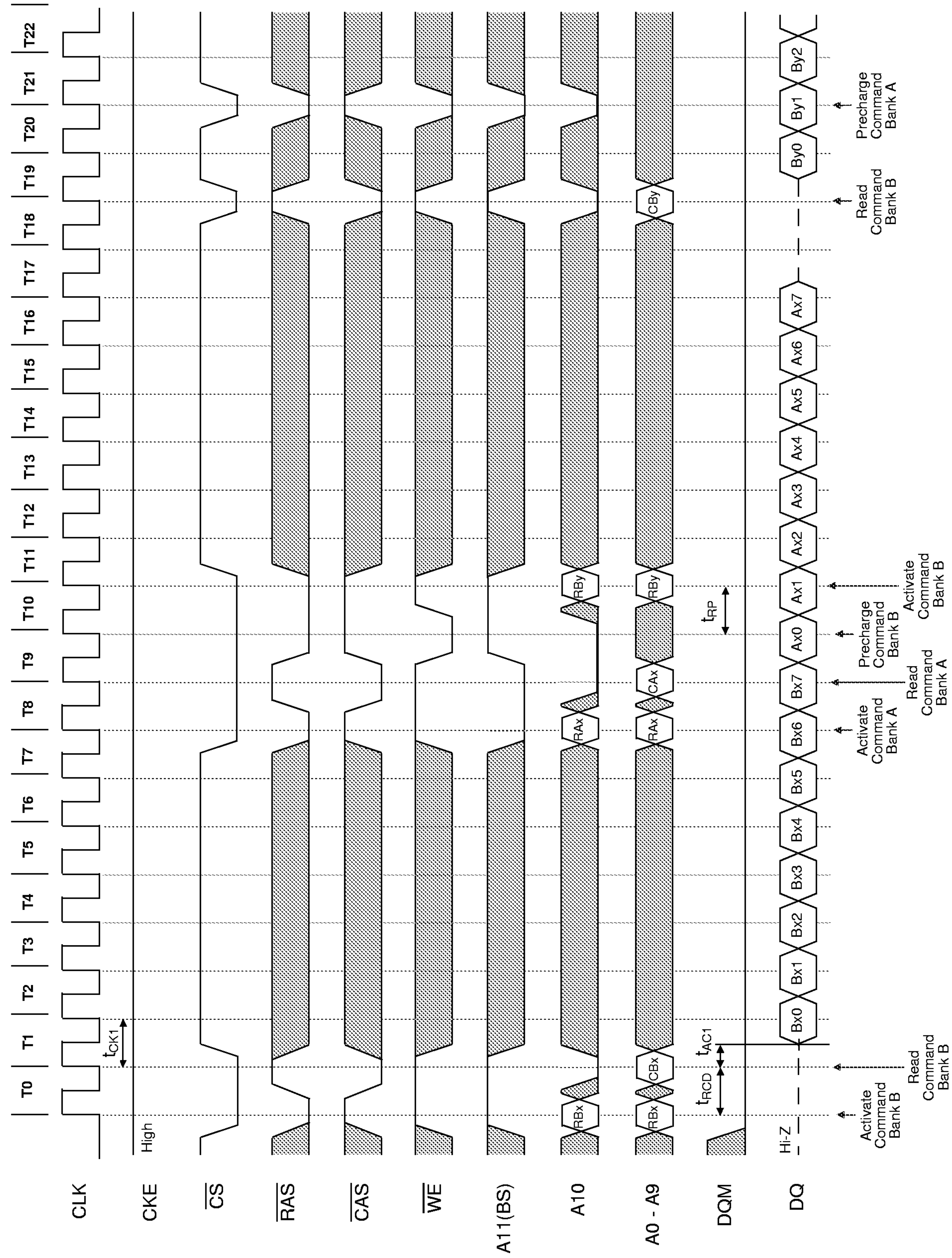
Random Column Write (Page within same Bank) (2 of 2)

Burst Length = 4, CAS Latency = 2



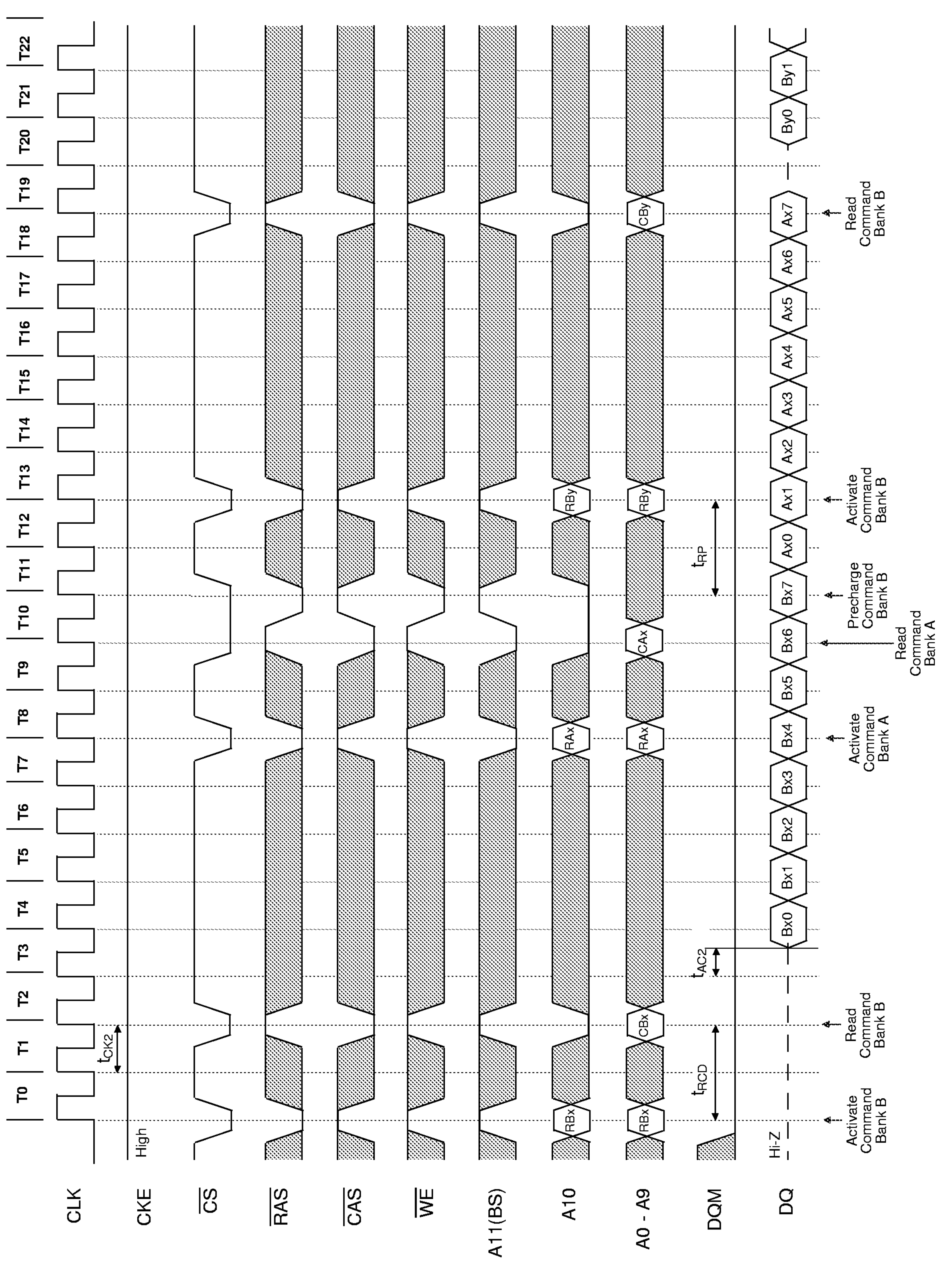
Random Row Read (Interleaving Banks) (1 of 2)

Burst Length = 8, CAS Latency = 1



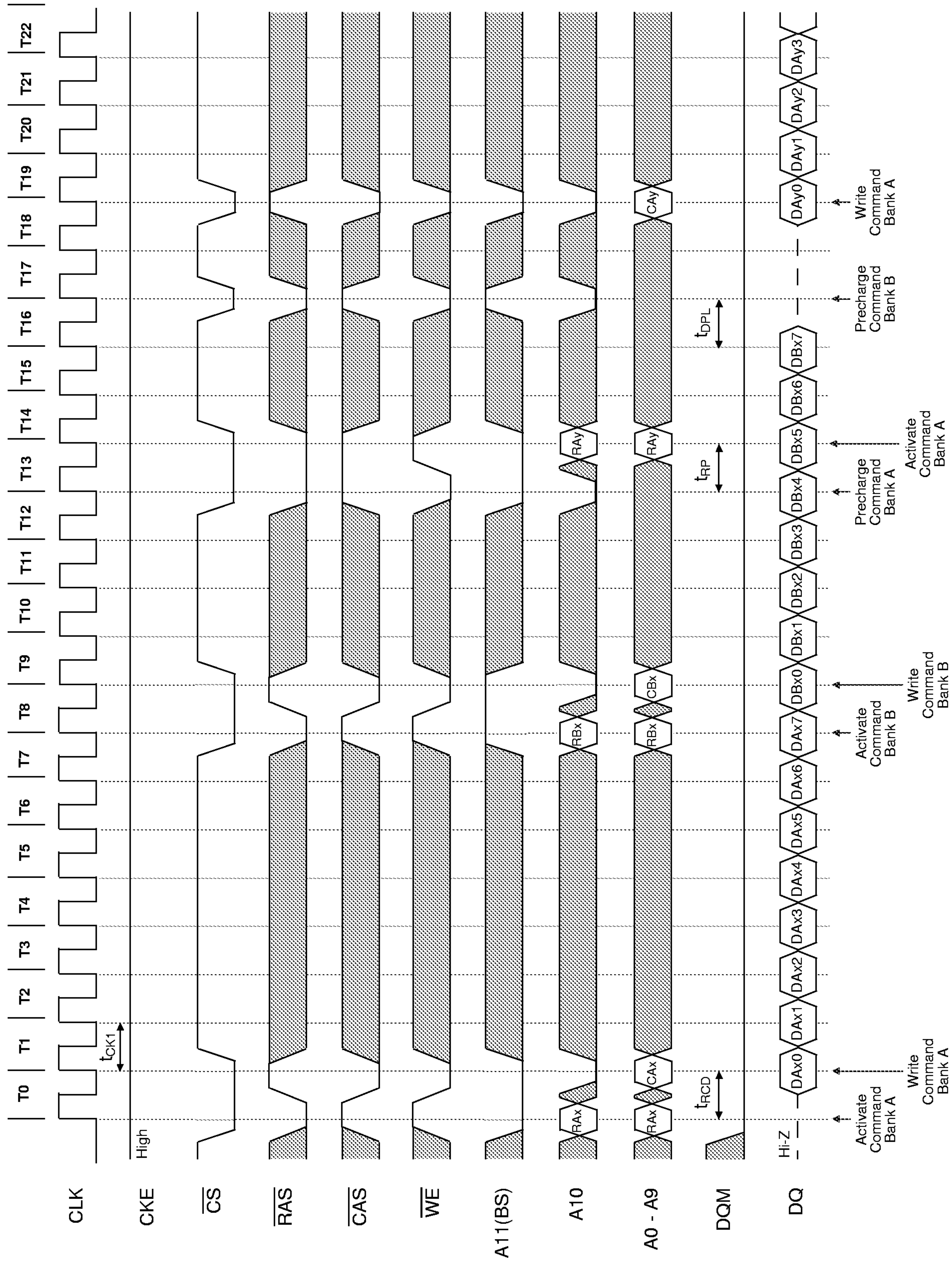
Random Row Read (Interleaving Banks) (2 of 2)

Burst Length = 8, CAS Latency = 2



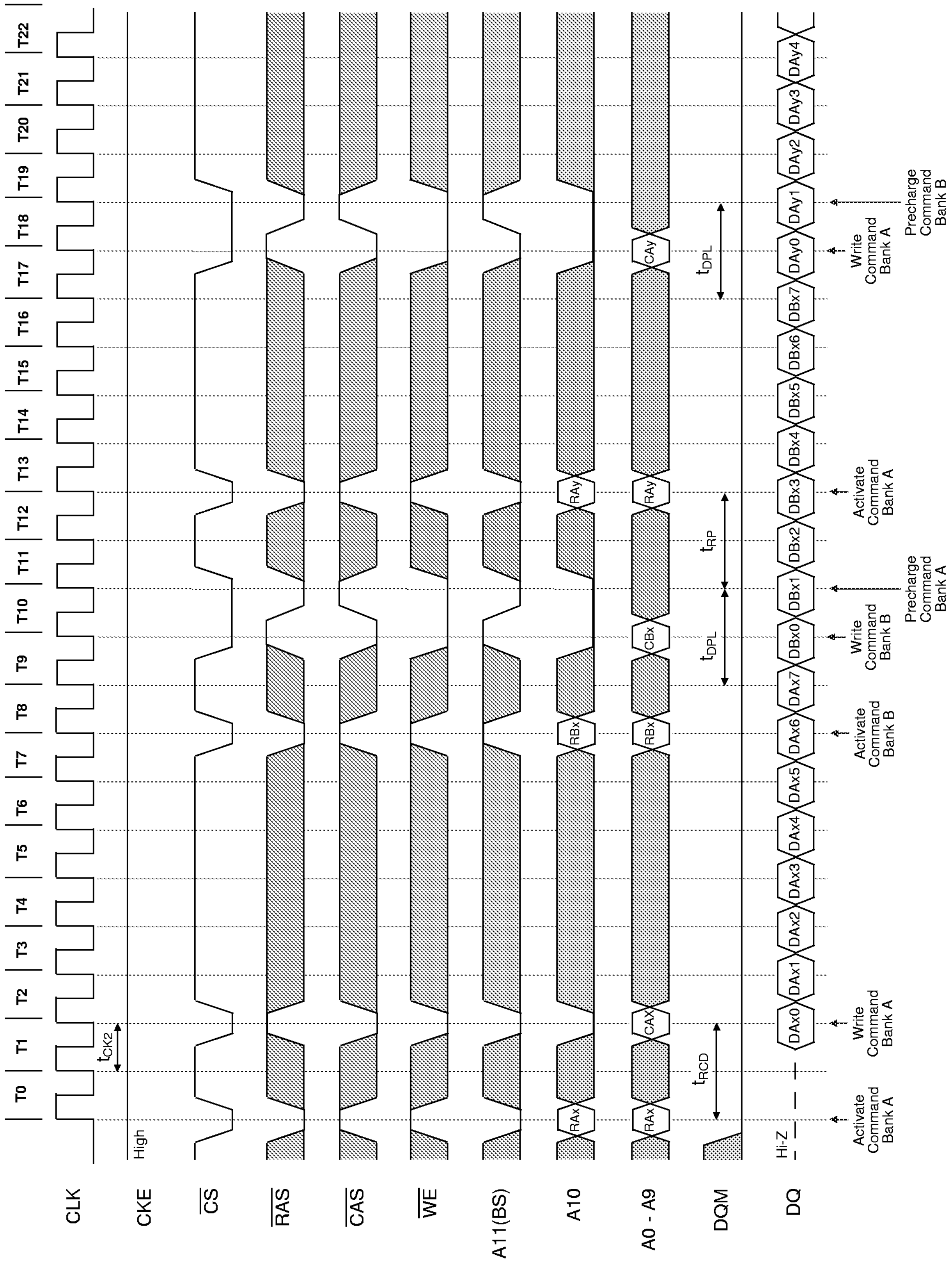
Random Row Write (Interleaving Banks) (1 of 2)

Burst Length = 8, CAS Latency = 1



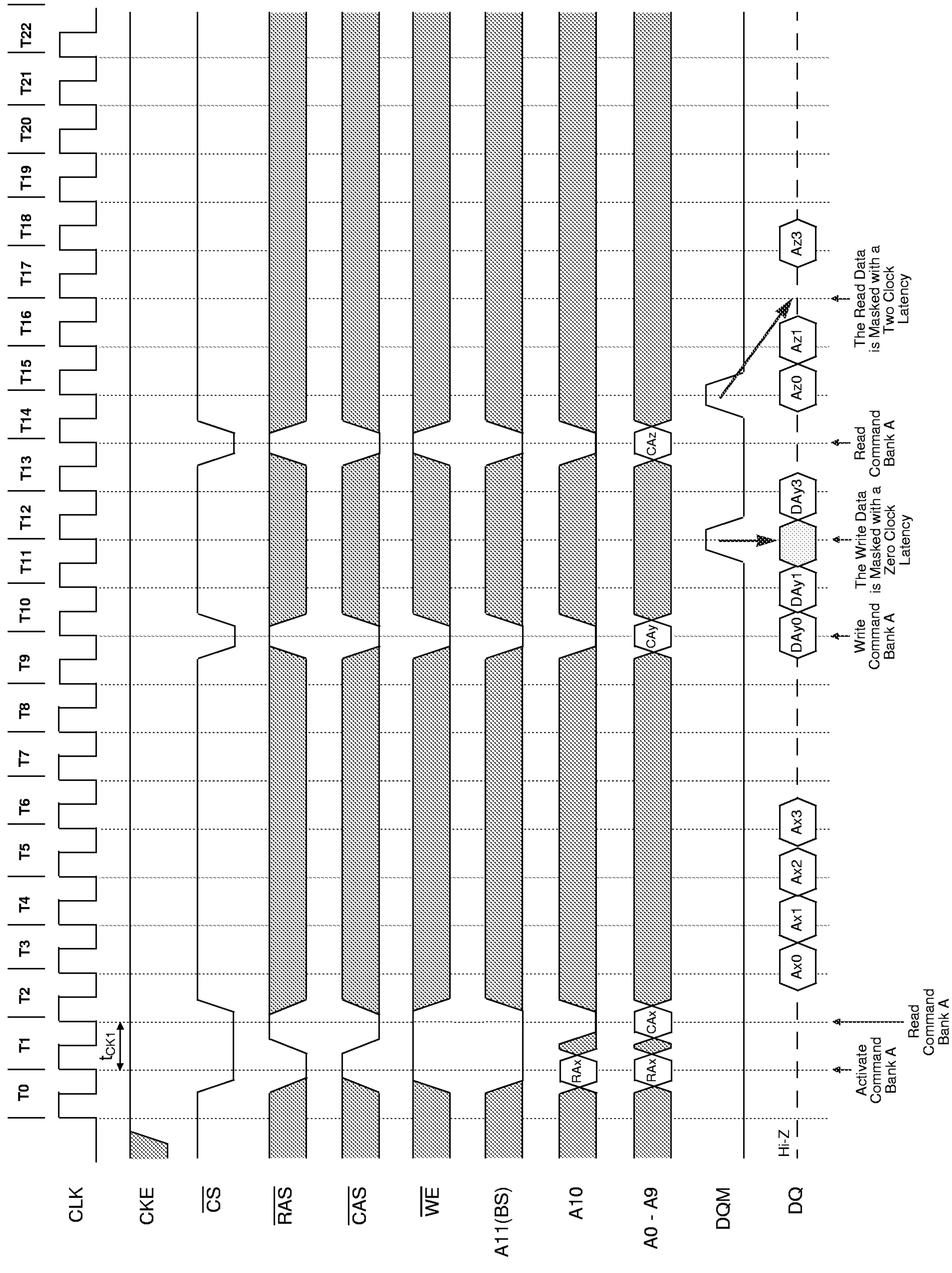
Random Row Write (Interleaving Banks) (2 of 2)

Burst Length = 8, CAS Latency = 2



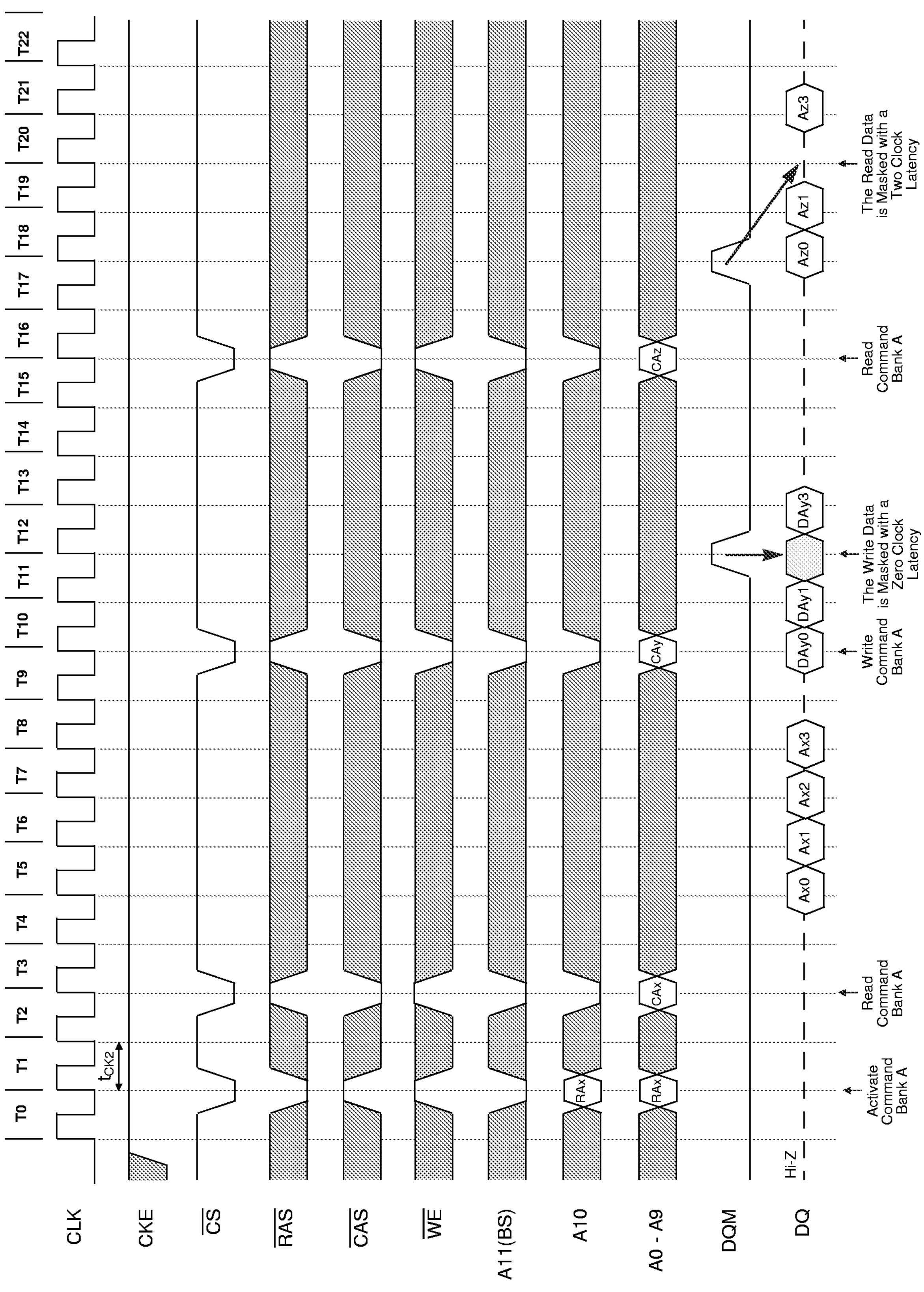
Read and Write Cycle (Page Hits) (1 of 2)

Burst Length = 4, CAS Latency = 1



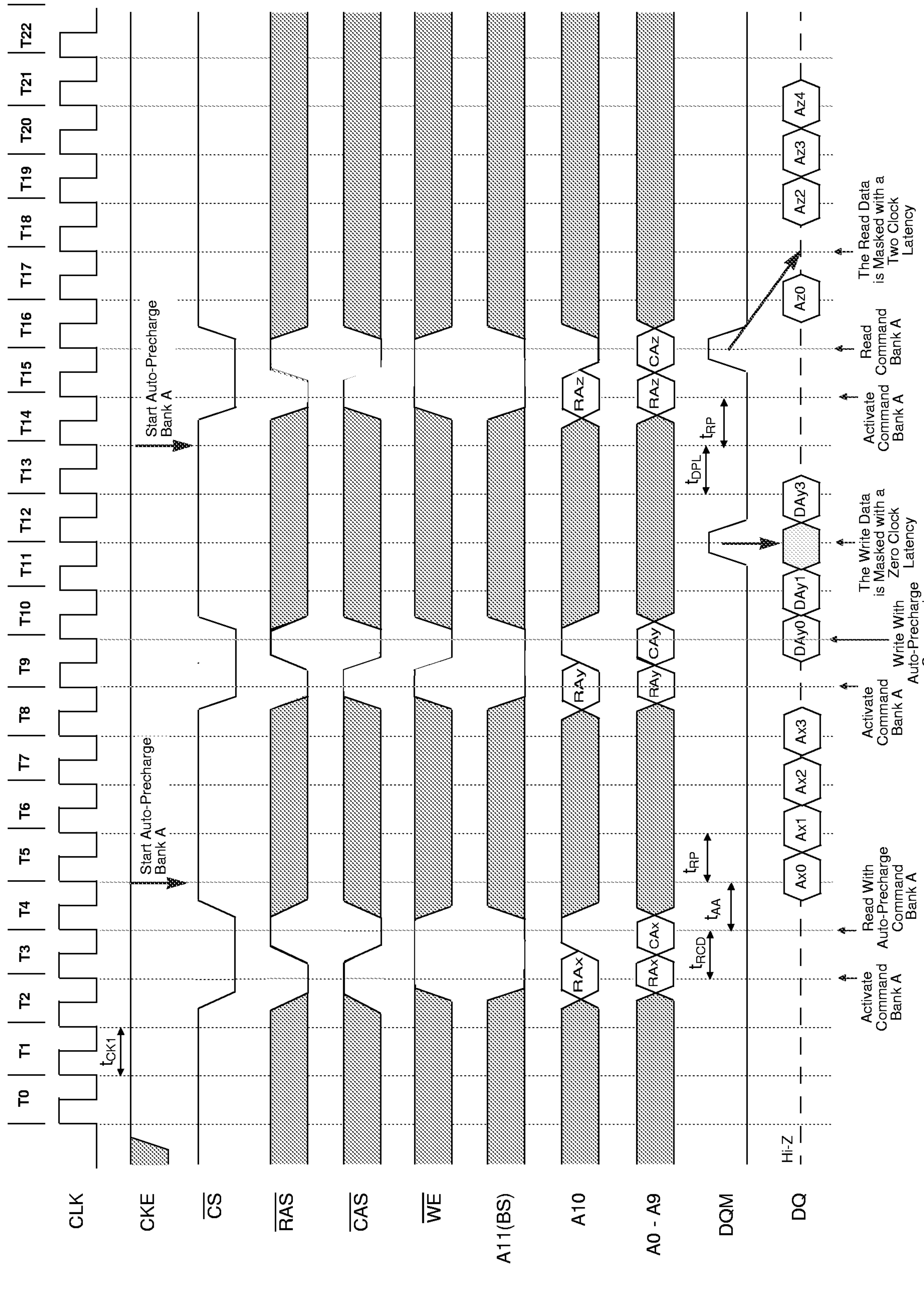
Read and Write Cycle (Page Hits) (2 of 2)

Burst Length = 4, CAS Latency = 2



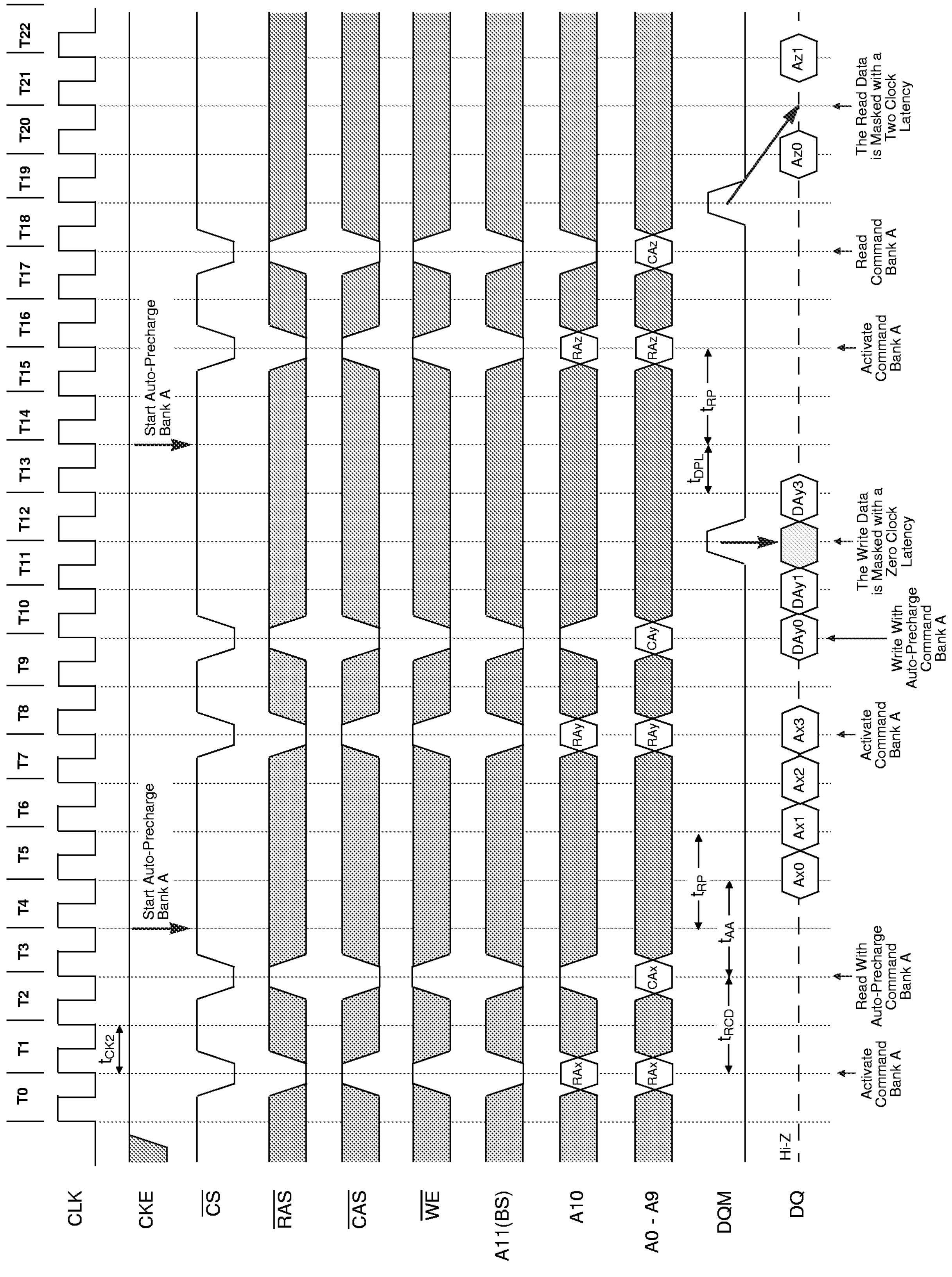
Read and Write Cycle (Random Row) (1 of 2)

Burst Length = 4, CAS Latency =1



Read and Write Cycle (Random Row) (2 of 2)

Burst Length = 4, CAS Latency = 2



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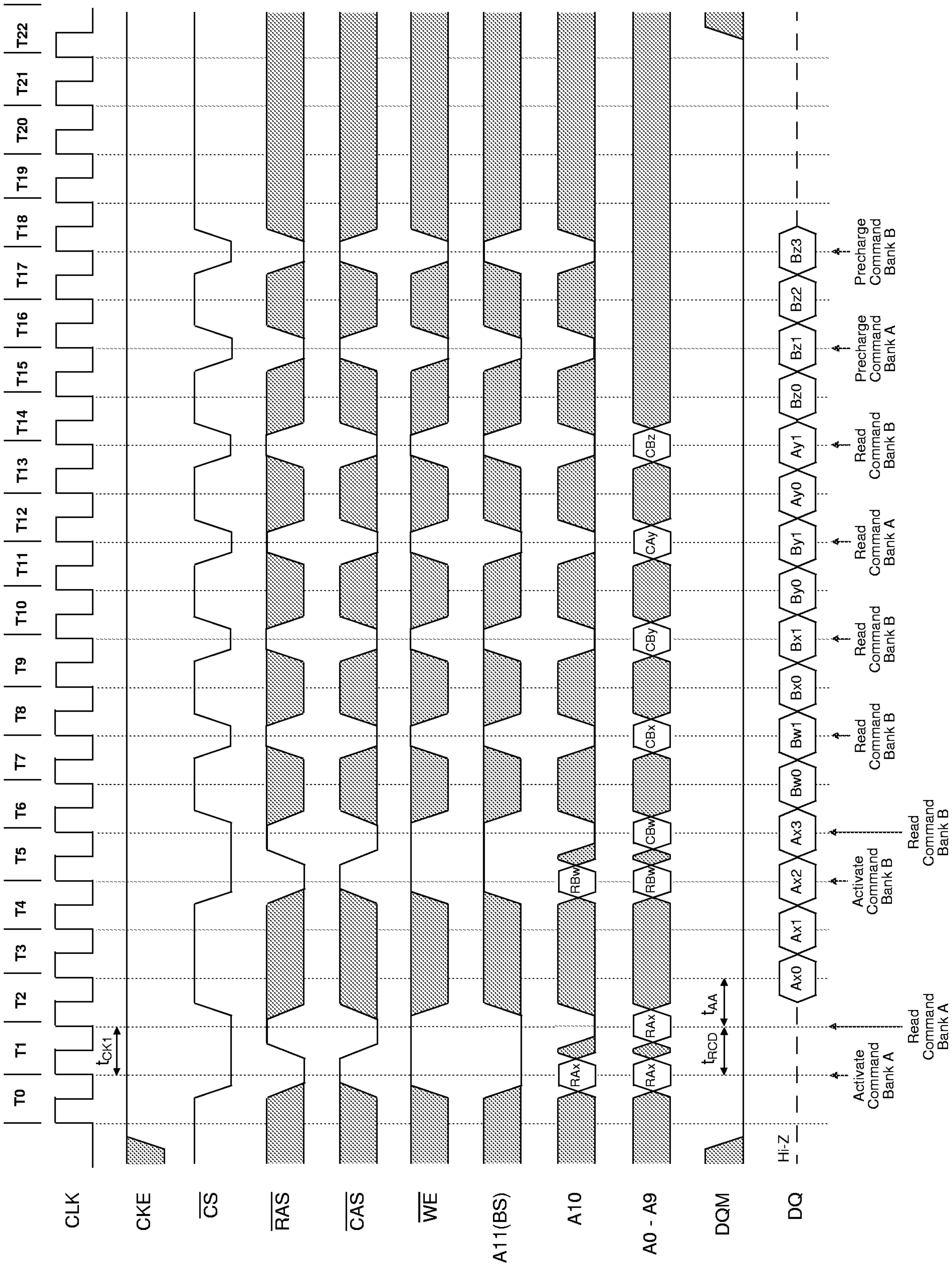
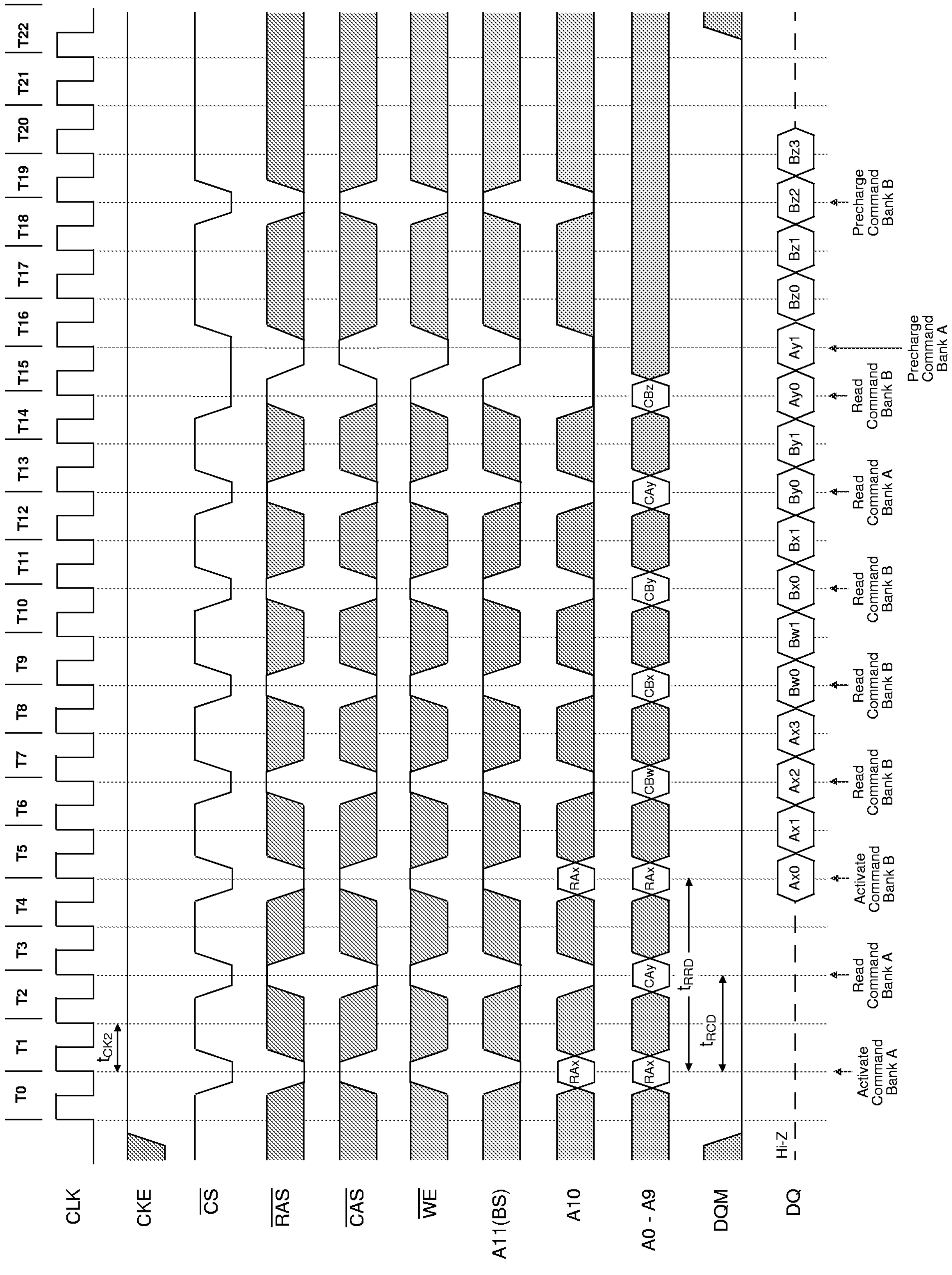
Interleaved Column Read Cycle (1 of 2)

Burst Length = 4, CAS Latency = 1



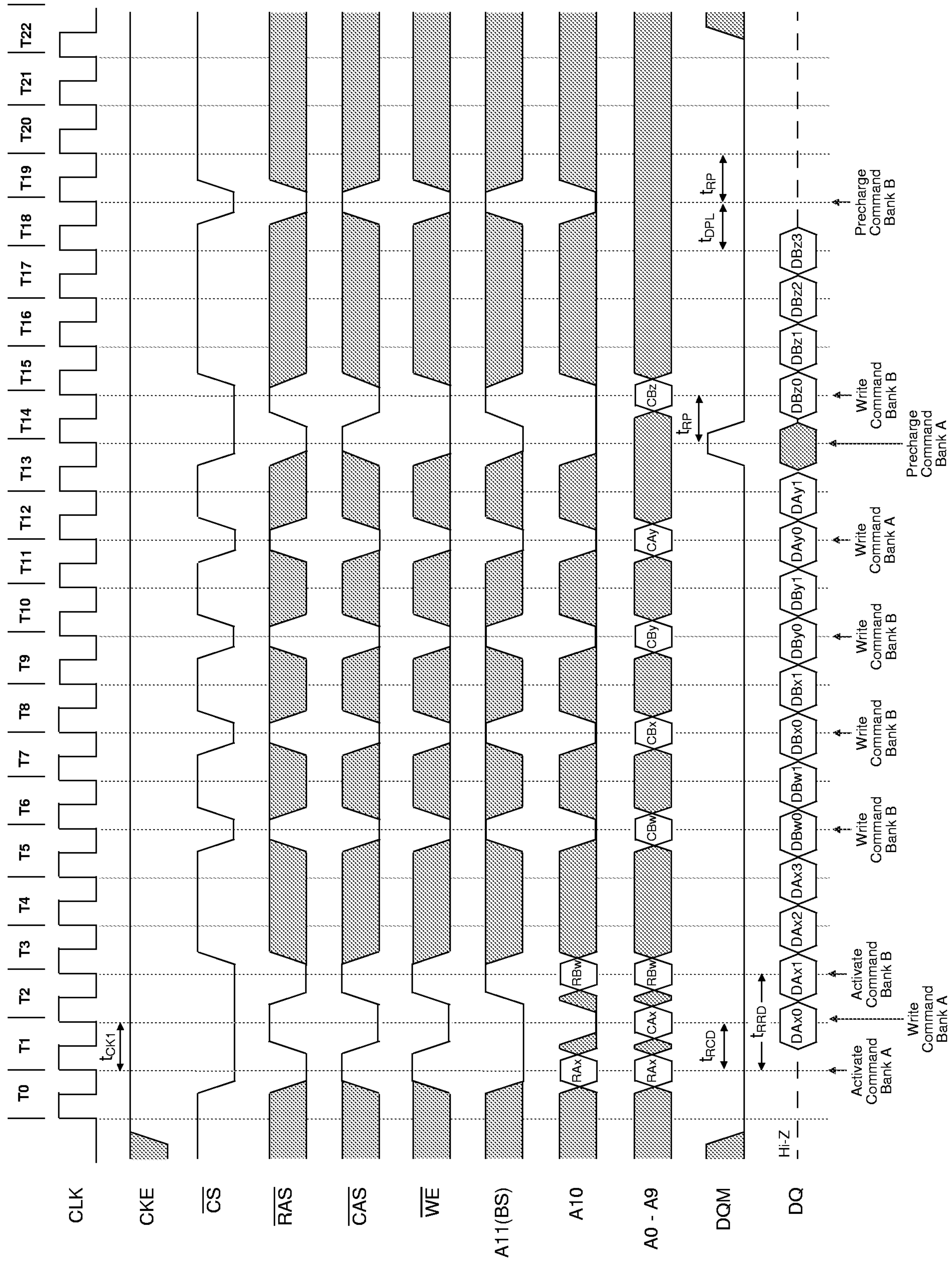
Interleaved Column Read Cycle (2 of 2)

Burst Length = 4, CAS Latency = 2



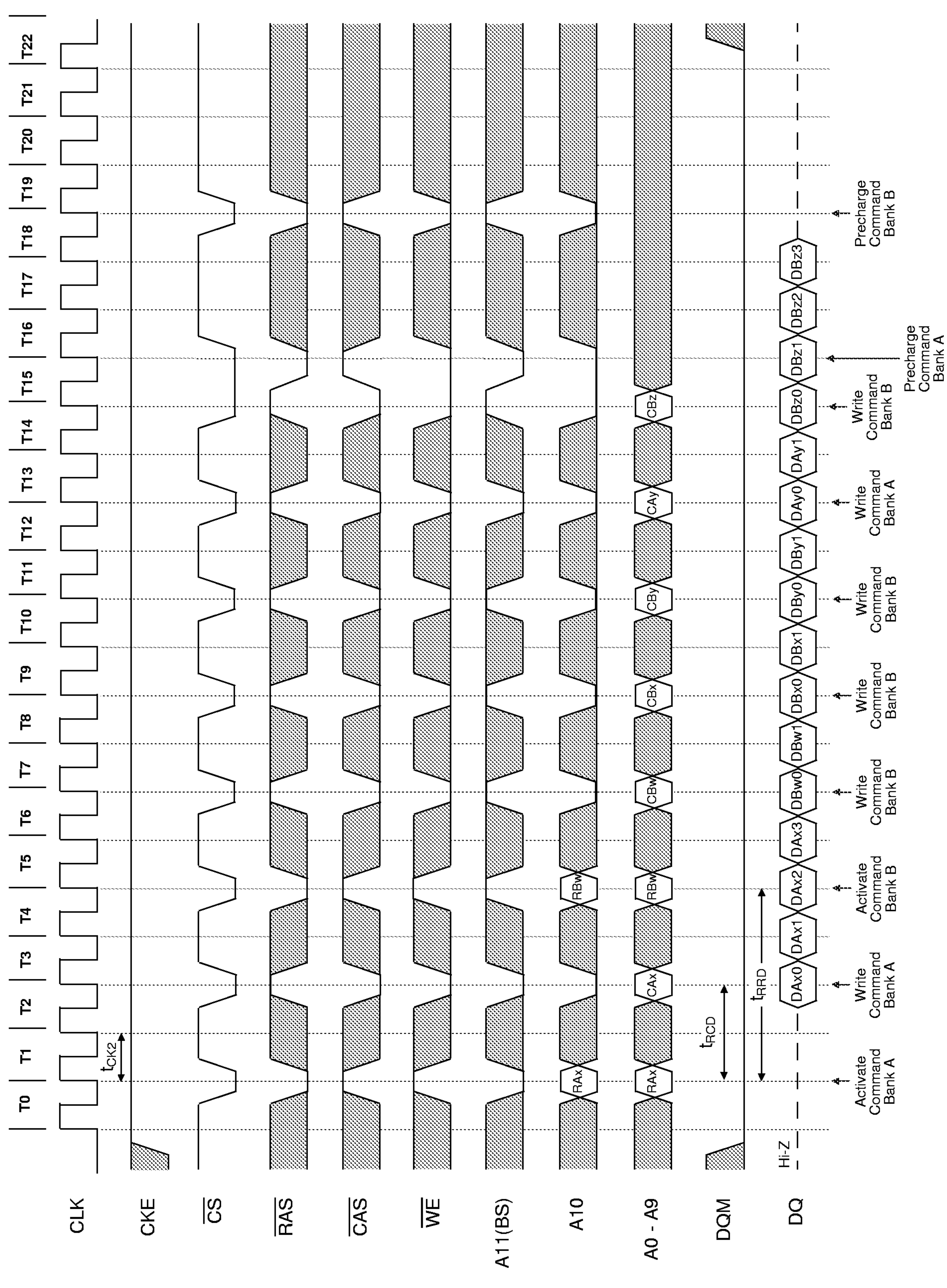
Interleaved Column Write Cycle (1 of 2)

Burst Length = 4, CAS Latency = 1



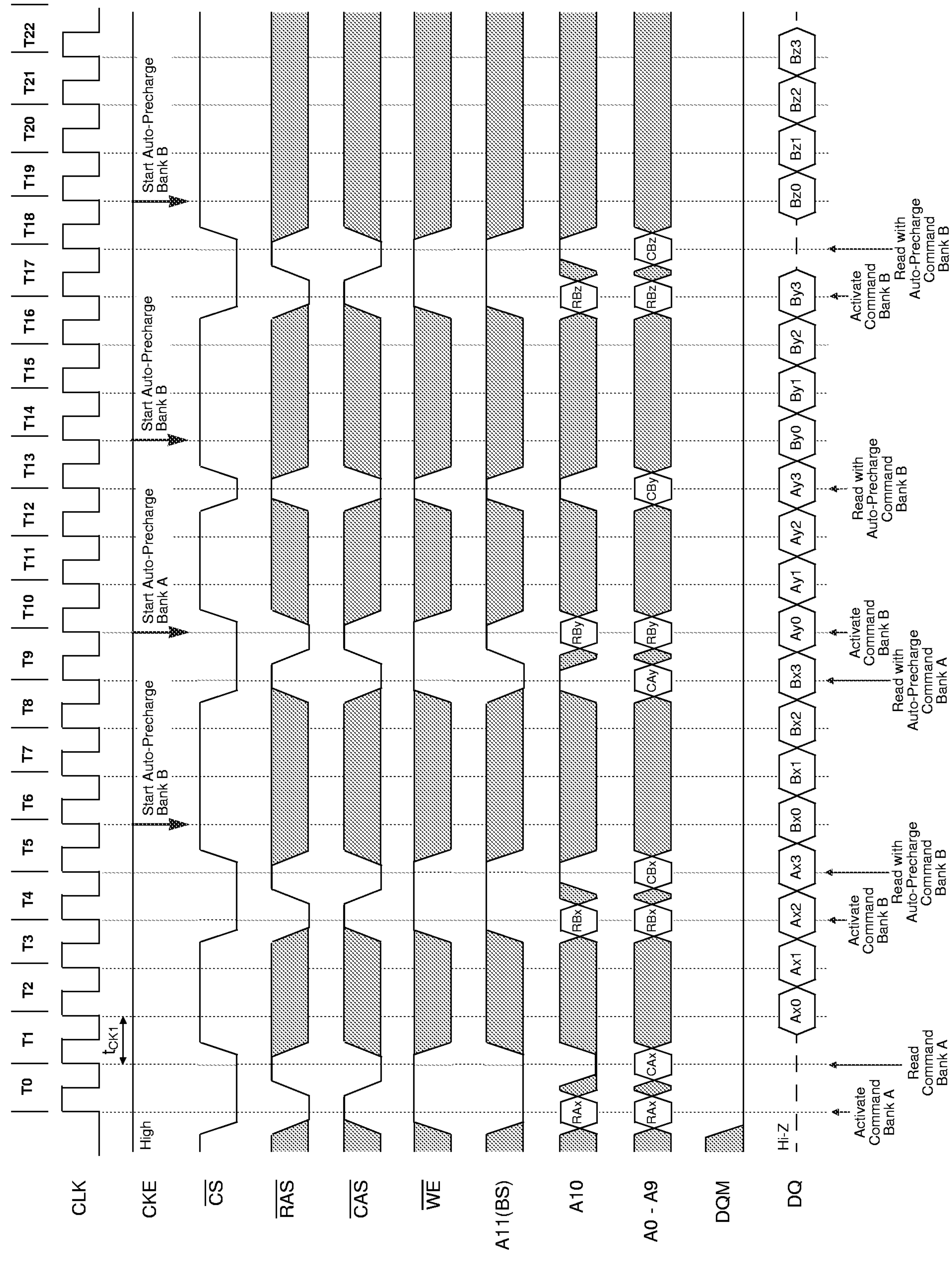
Interleaved Column Write Cycle (2 of 2)

Burst Length = 4, CAS Latency = 2



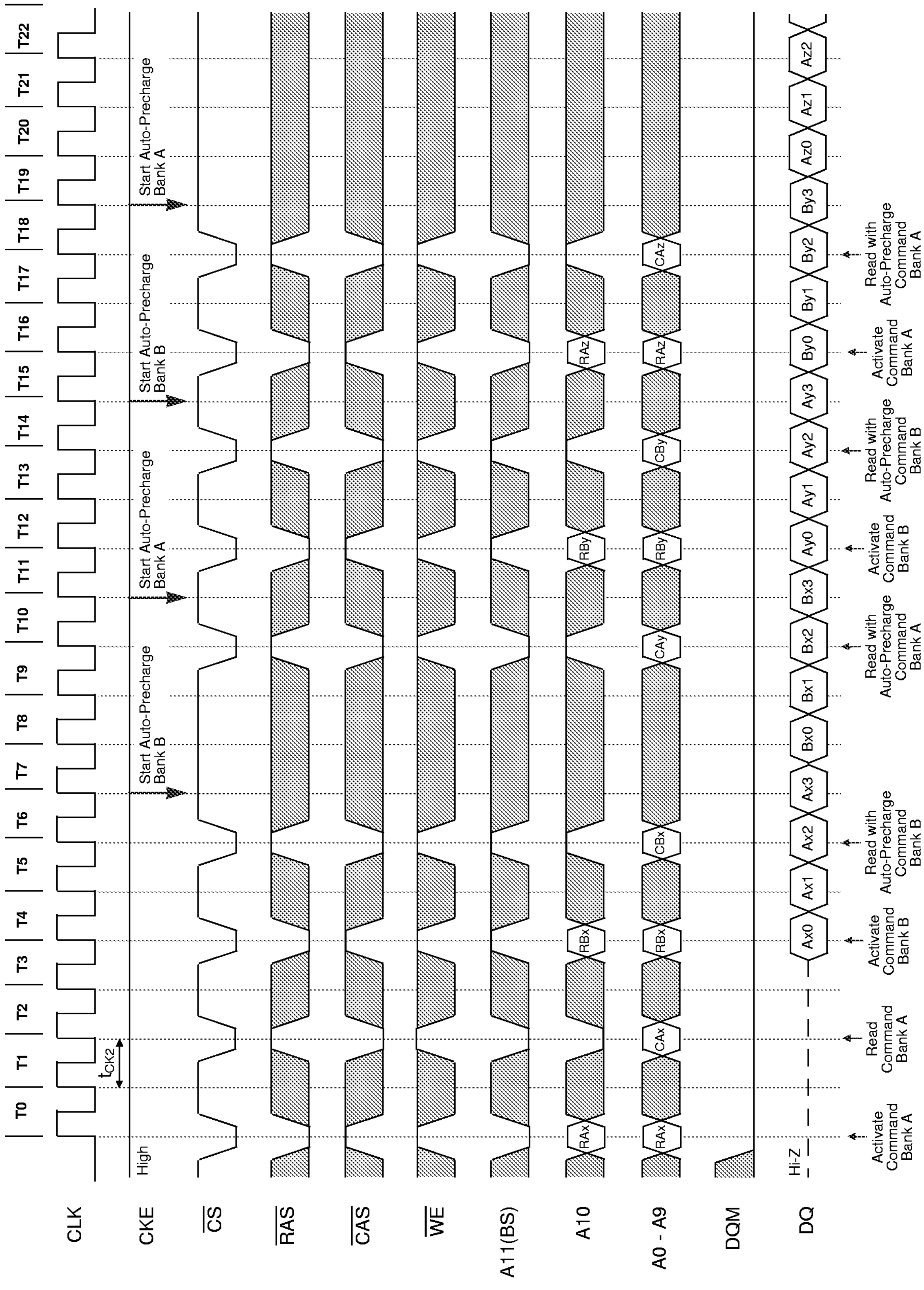
Auto Precharge after Read Burst (1 of 2)

Burst Length = 4, CAS Latency = 1



Auto Precharge after Read Burst (2 of 2)

Burst Length = 4, CAS Latency = 2



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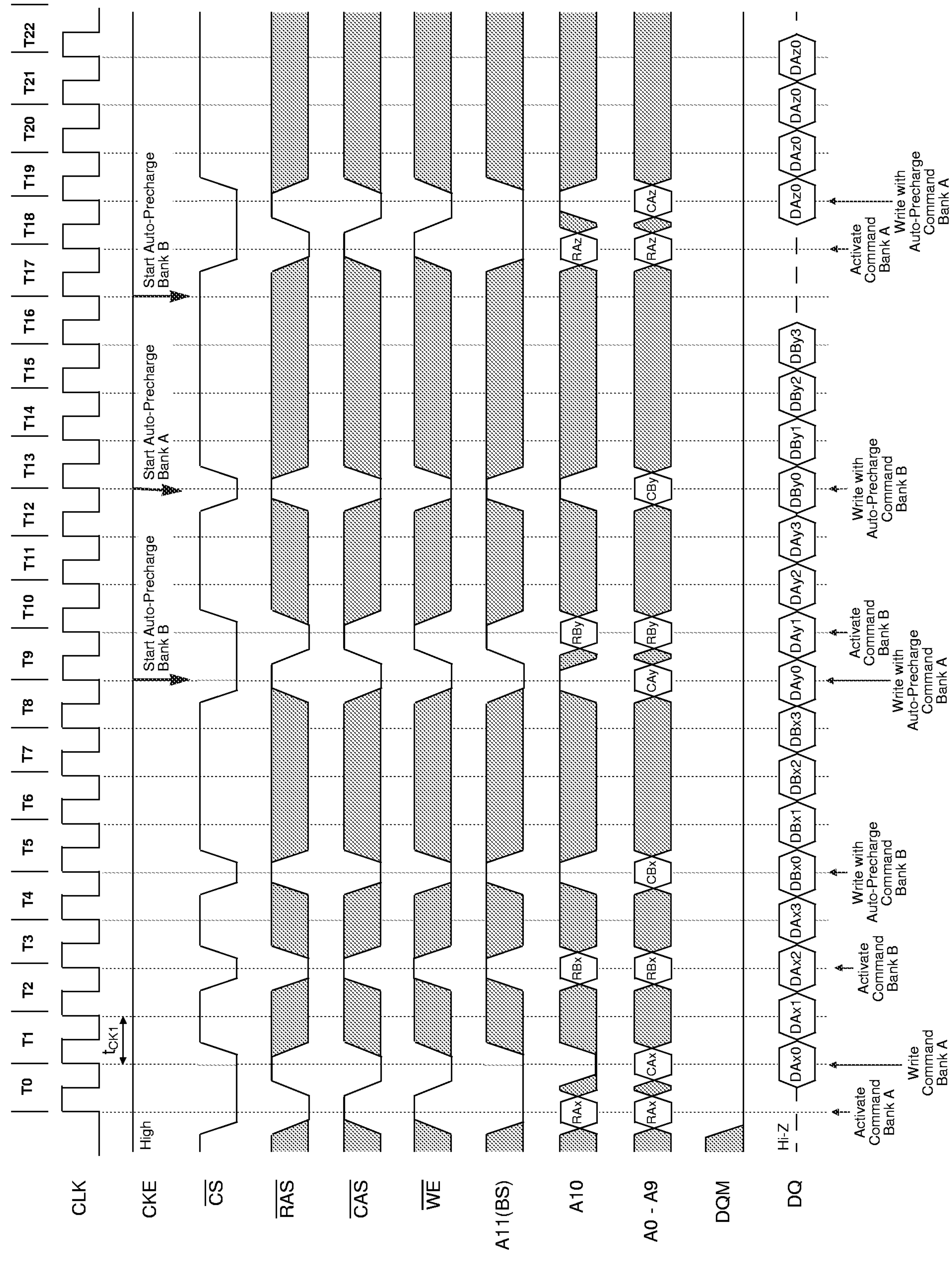
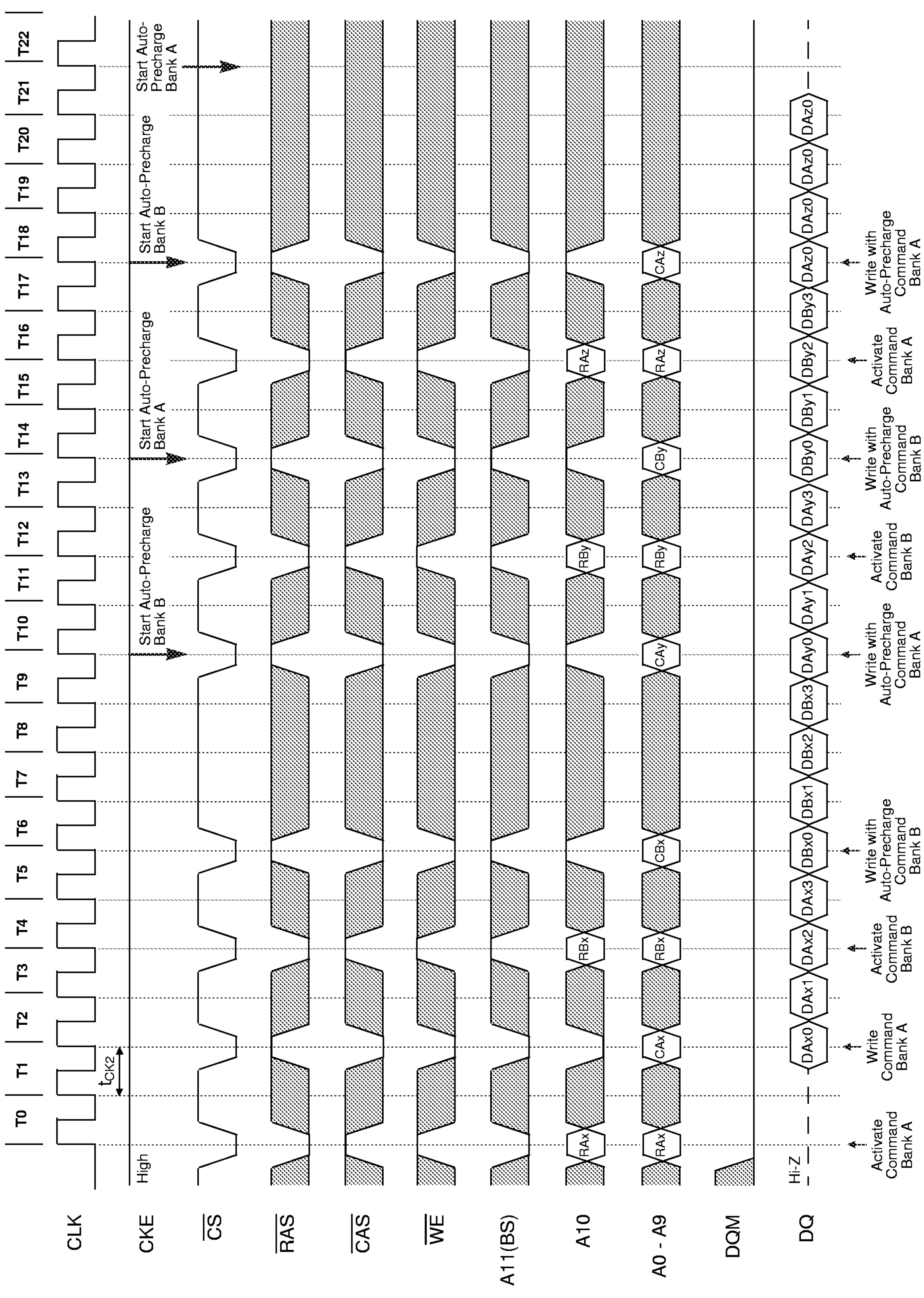
Auto Precharge after Write Burst (1 of 2)

Burst Length = 4, CAS Latency = 1



Auto Precharge after Write Burst (2 of 2)

Burst Length = 4, CAS Latency = 2



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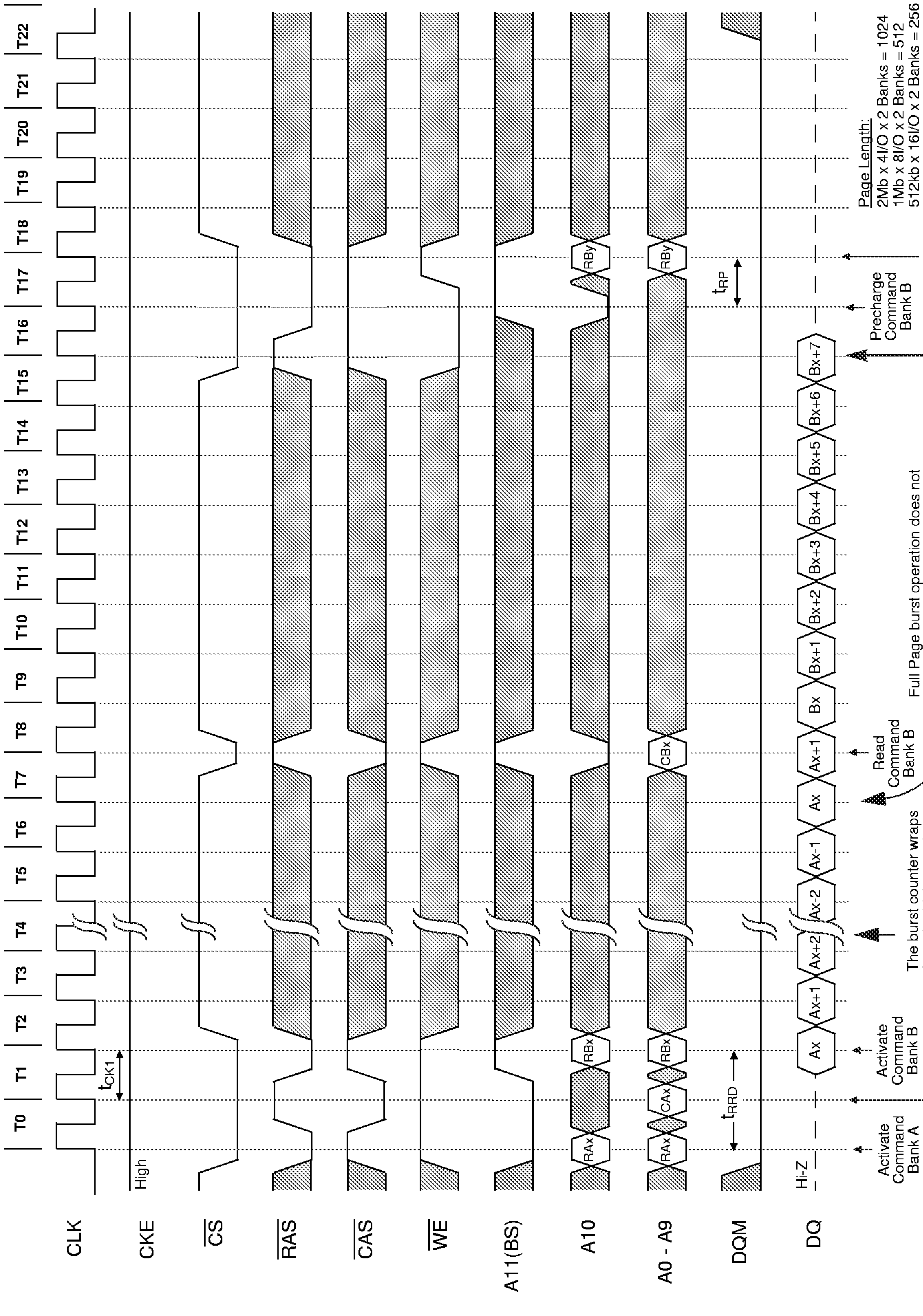
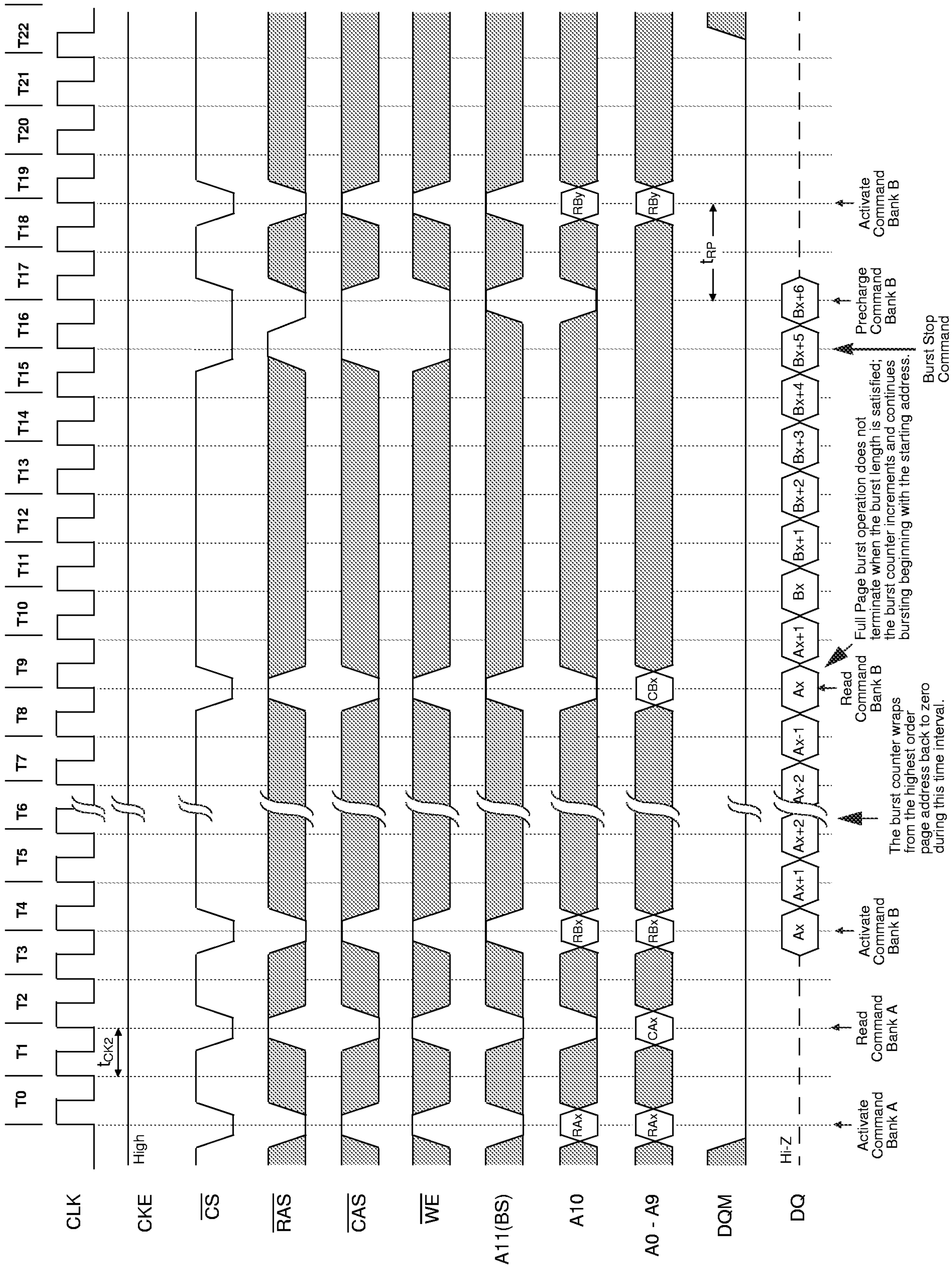
Full Page Read Cycle (1 of 2)

Burst Length = Full Page, CAS Latency = 1



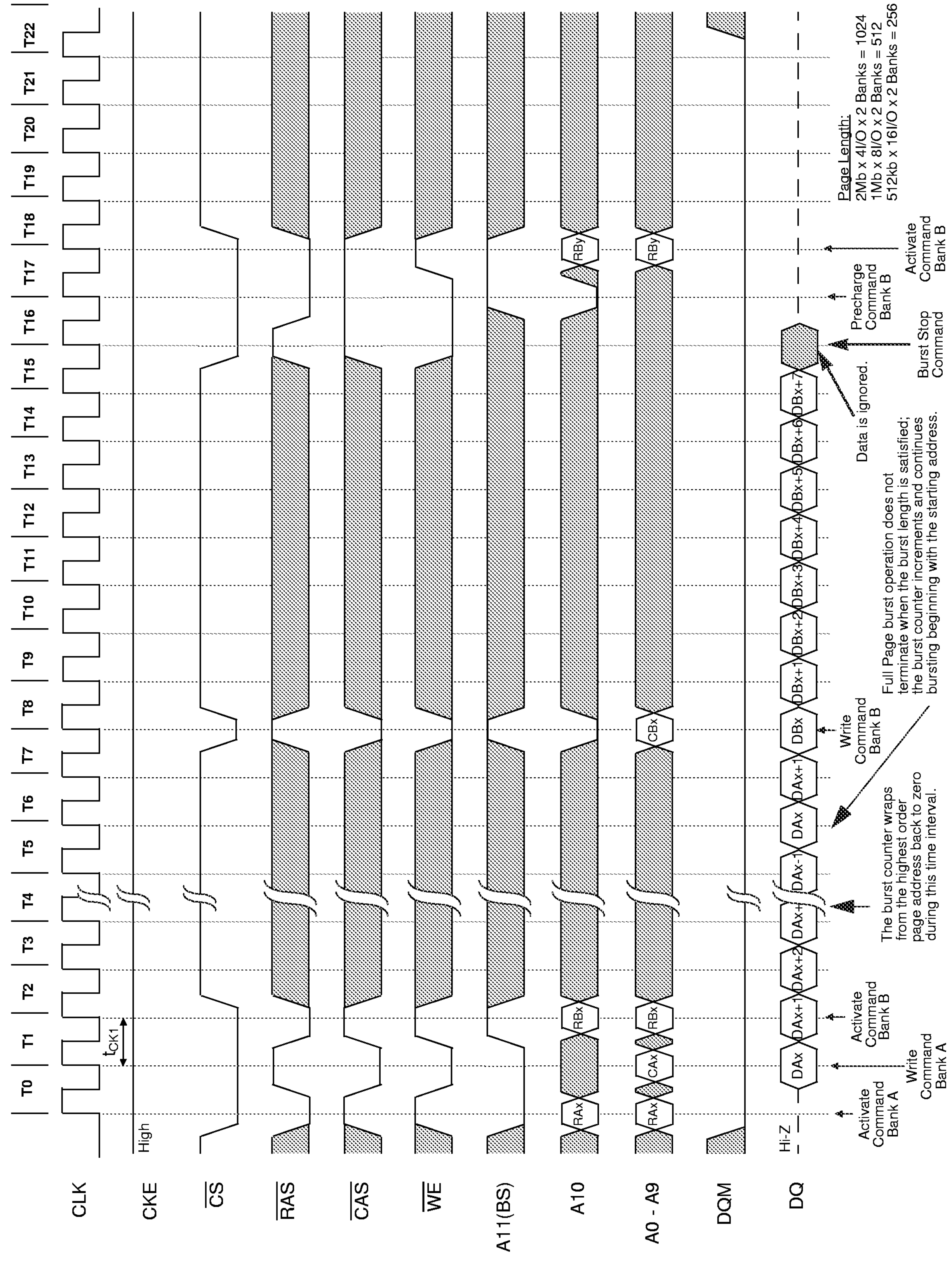
Full Page Read Cycle (2 of 2)

Burst Length = Full Page, CAS Latency = 2



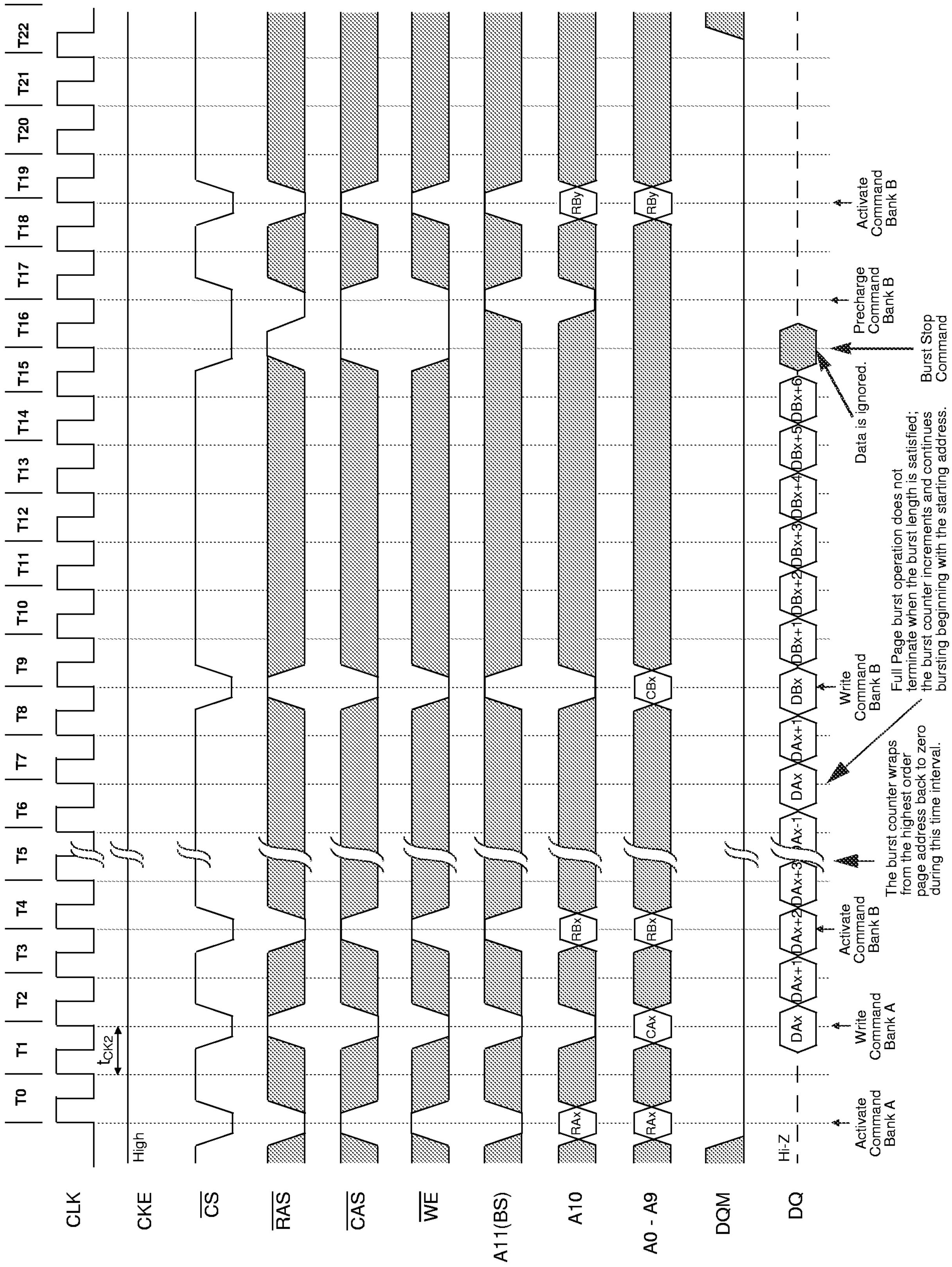
Full Page Write Cycle (1 of 2)

Burst Length = Full Page, CAS Latency = 1



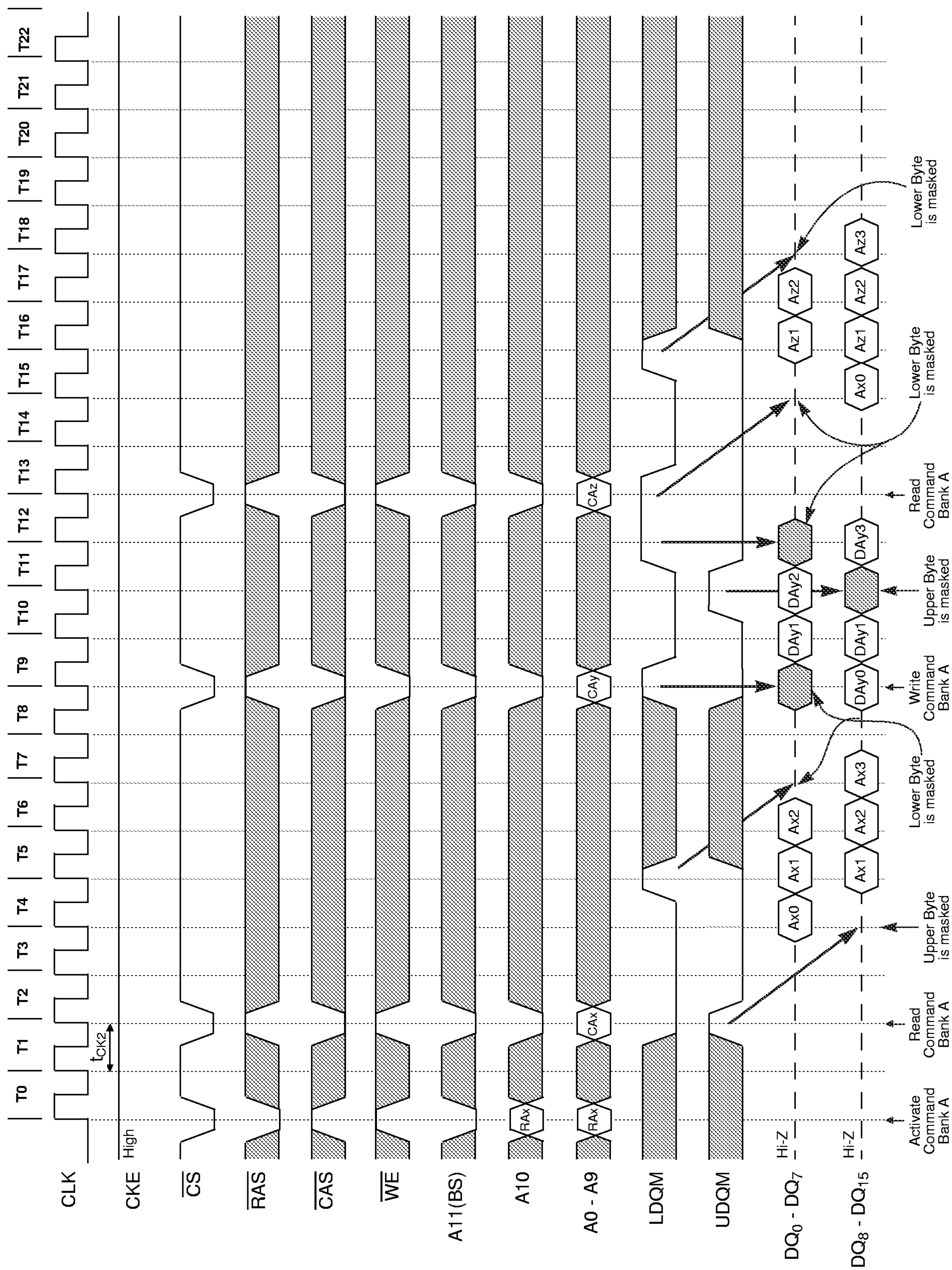
Full Page Write Cycle (2 of 2)

Burst Length = Full Page, CAS Latency = 2



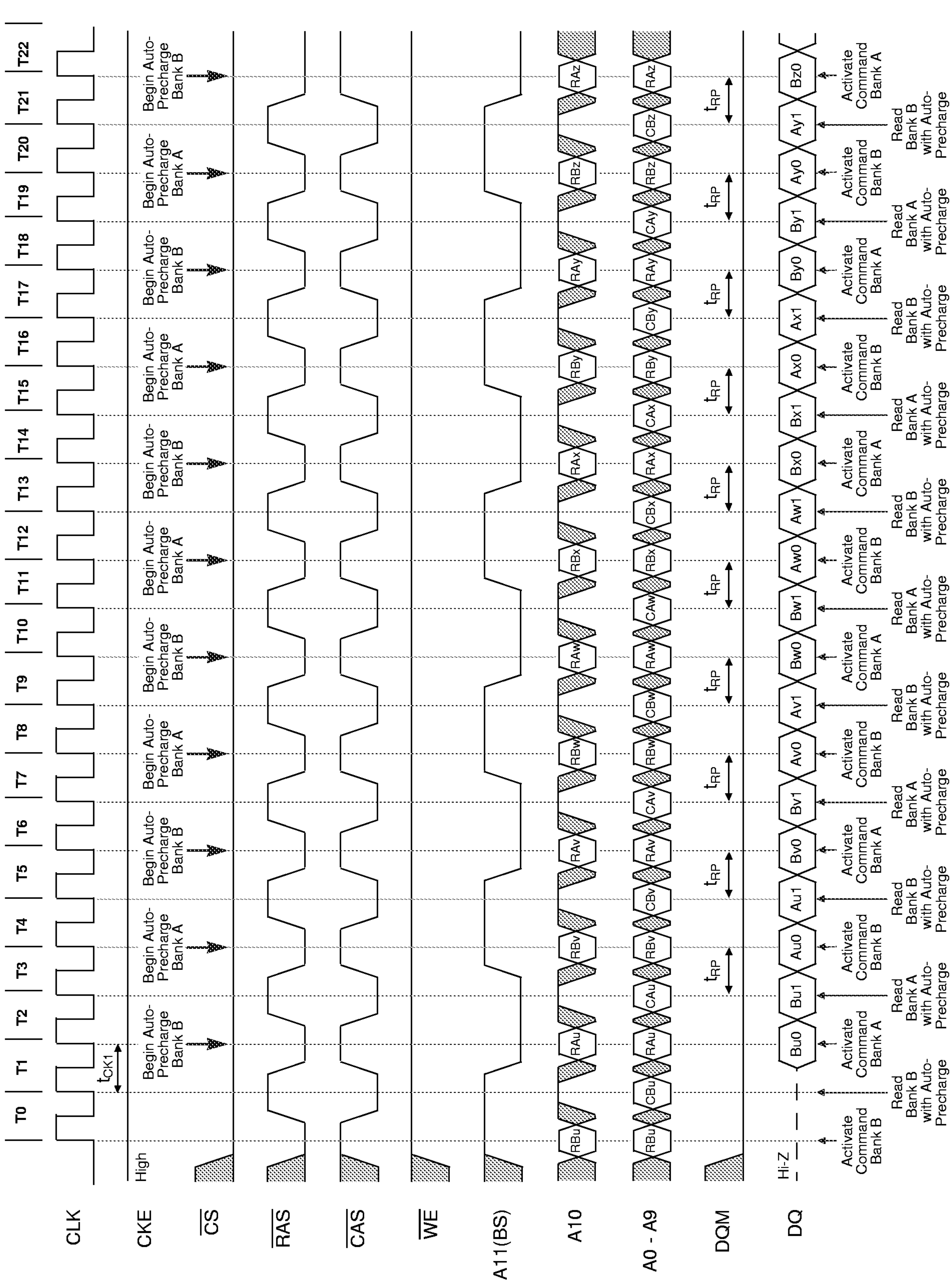
Byte Write Operation

Burst Length = 4, CAS Latency = 2



Random Row Read (Interleaving Banks)

Burst Length = 2, CAS Latency = 1



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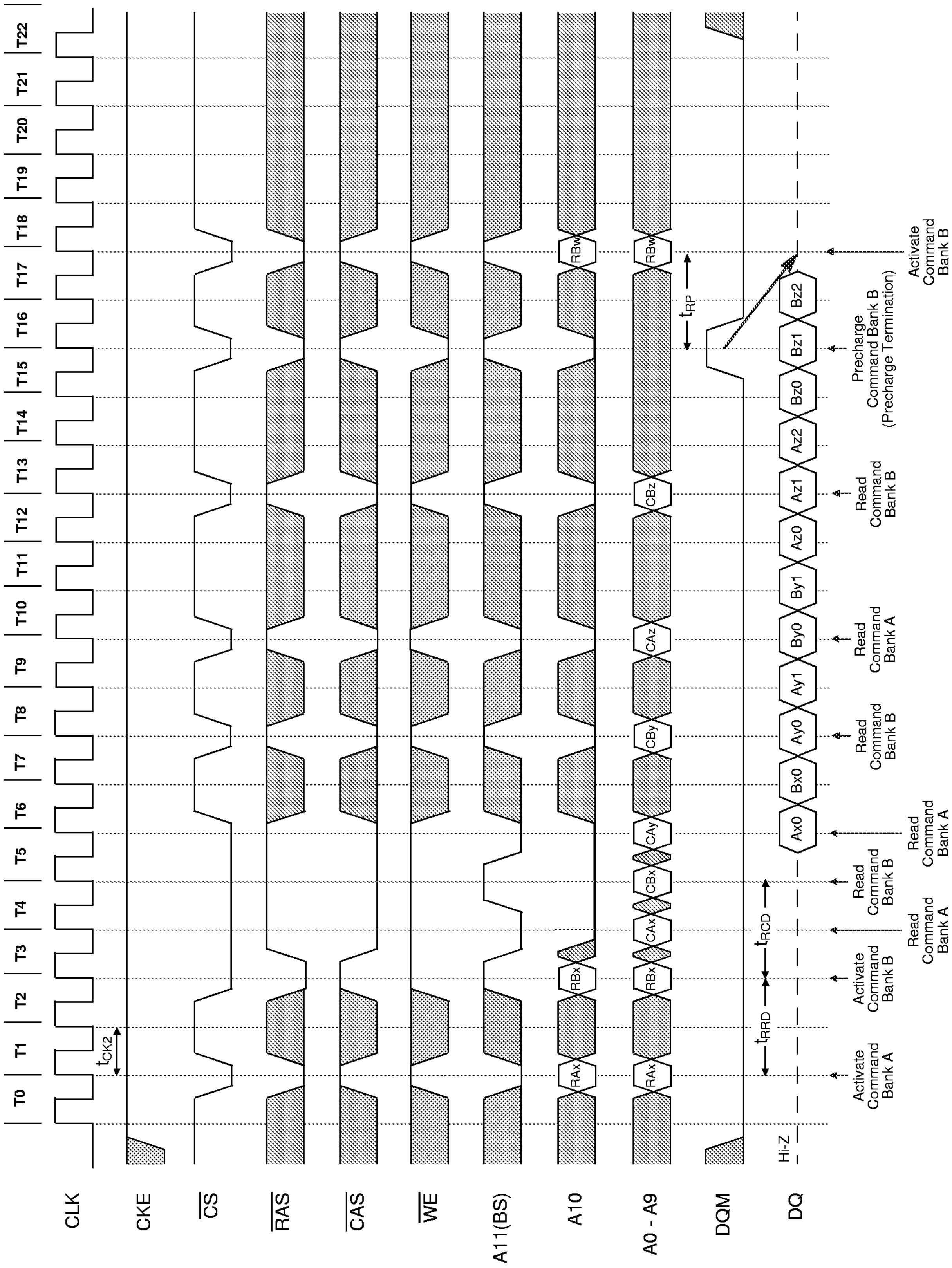
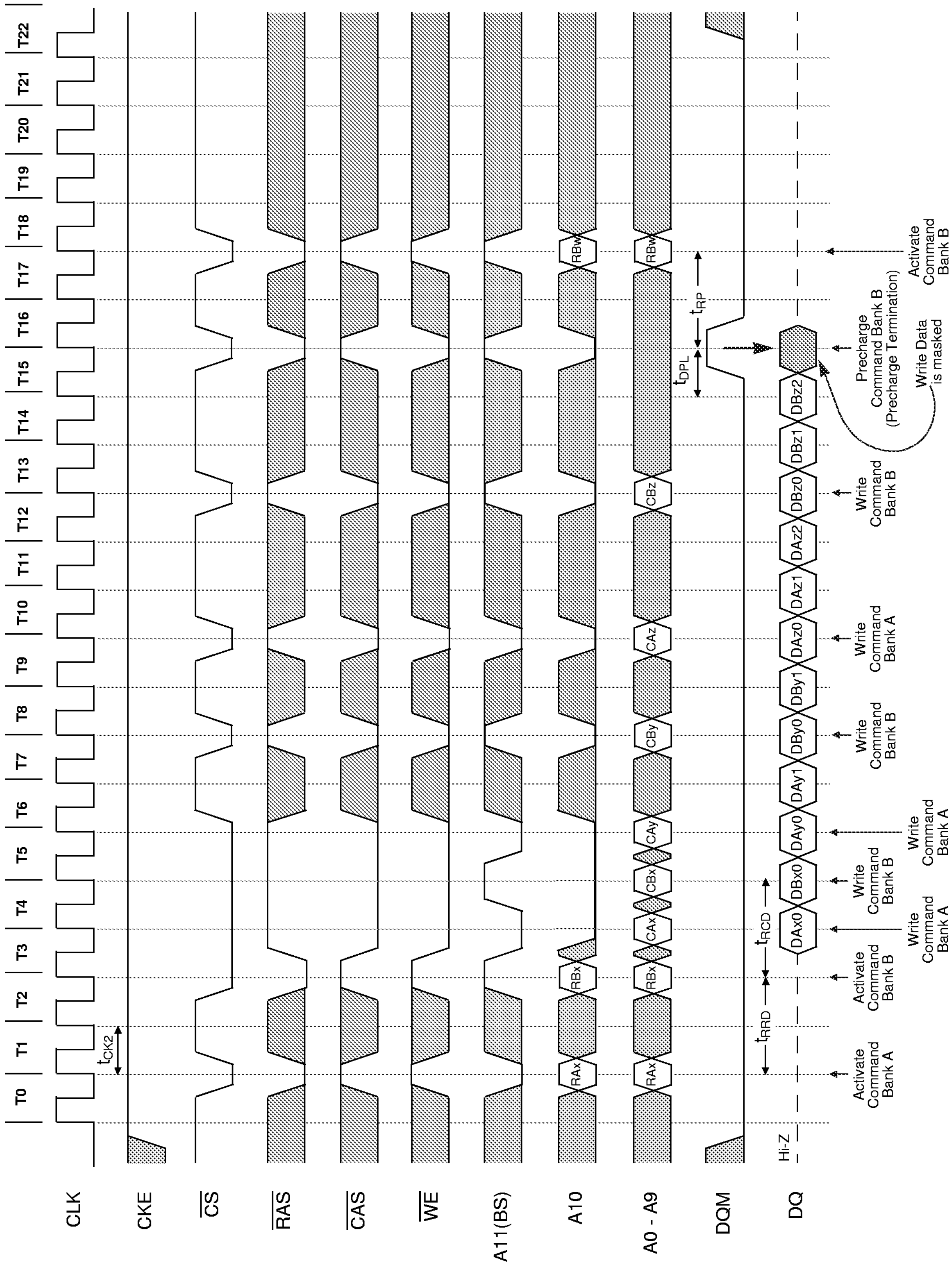
Full Page Random Column Read

Burst Length = Full Page, CAS Latency = 2



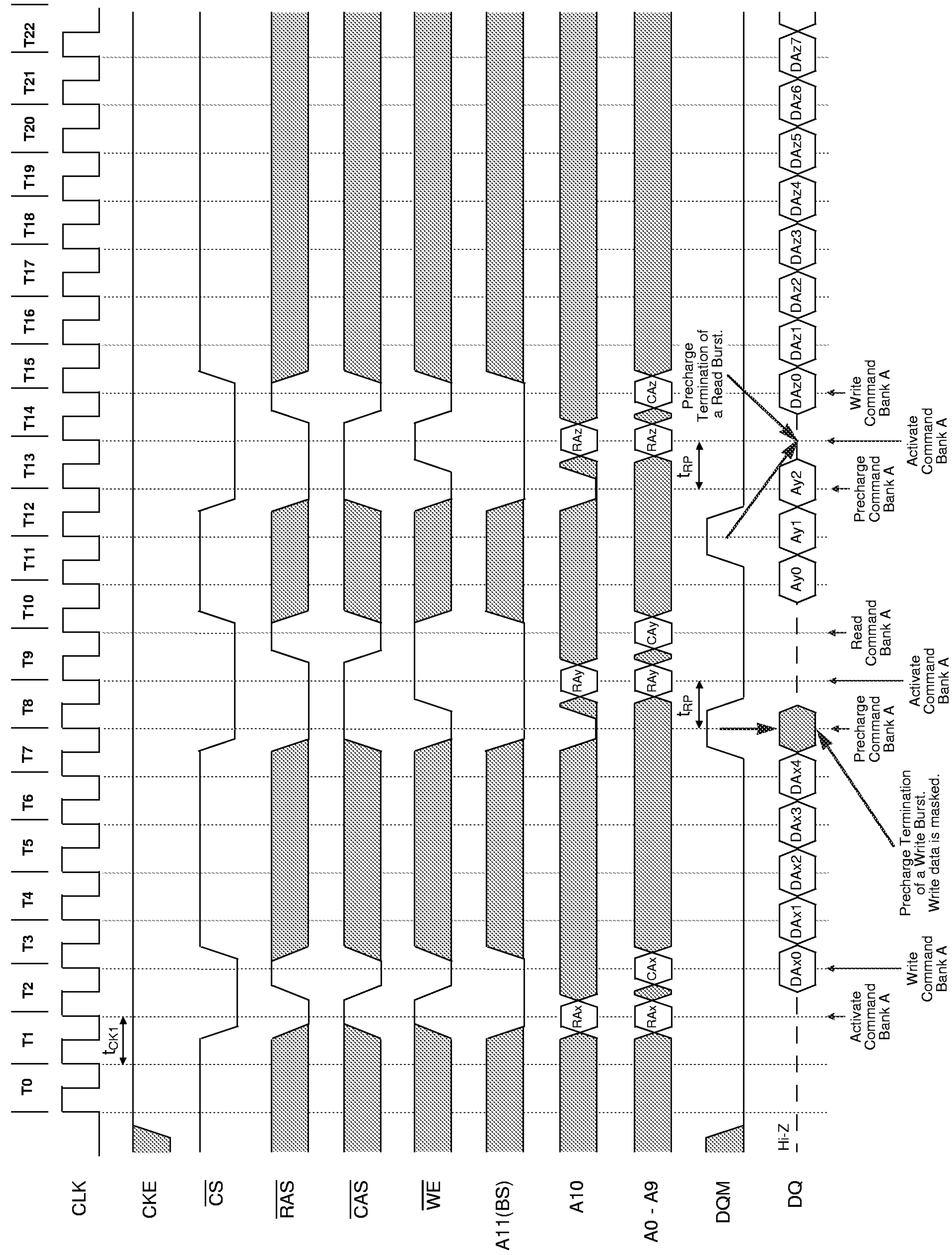
Full Page Random Column Write

Burst Length = Full Page, CAS Latency = 2



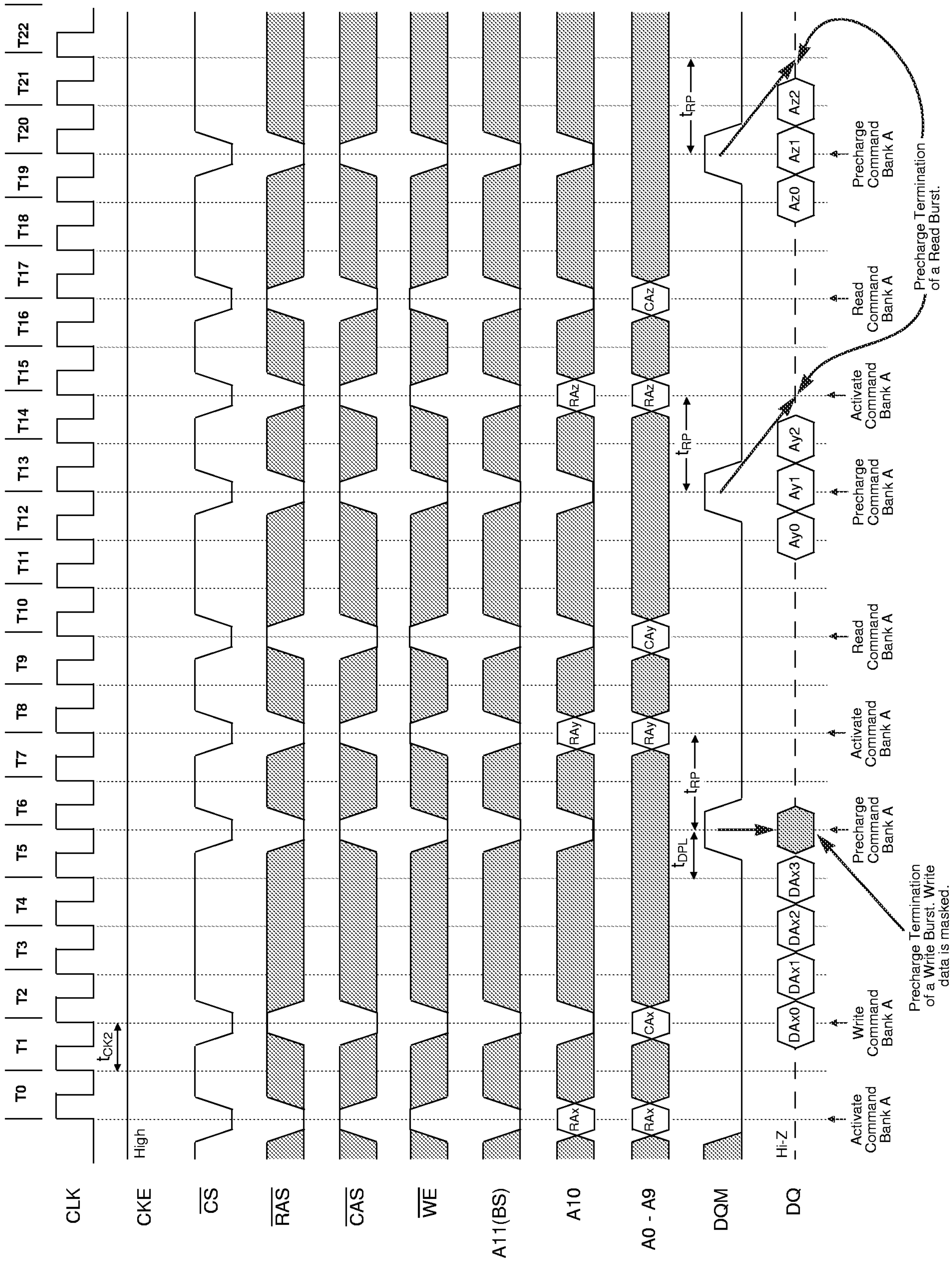
Precharge Termination of a Burst (1 of 2)

Burst Length = Full Page, CAS Latency = 1



Precharge Termination of a Burst (2 of 2)

Burst Length = 8 or Full Page, CAS Latency = 2



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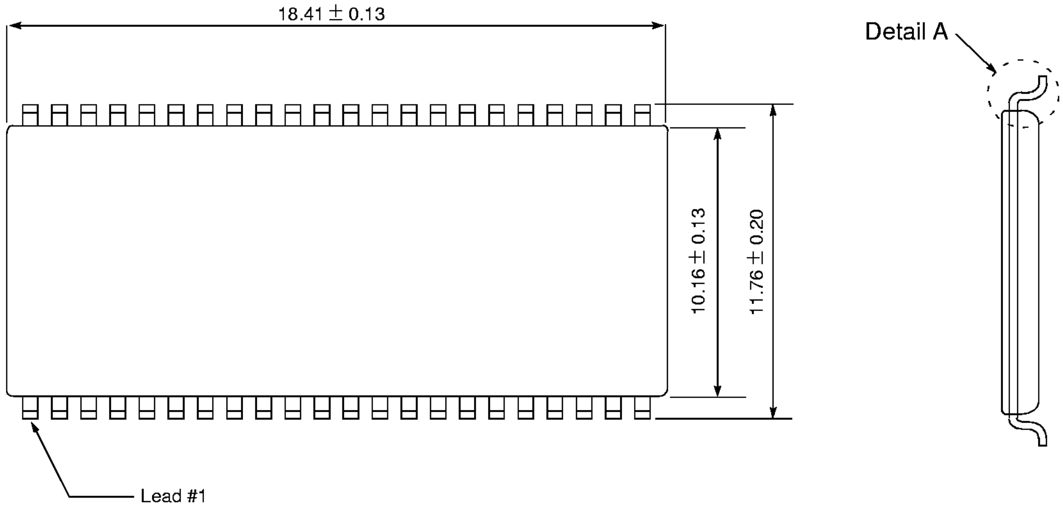
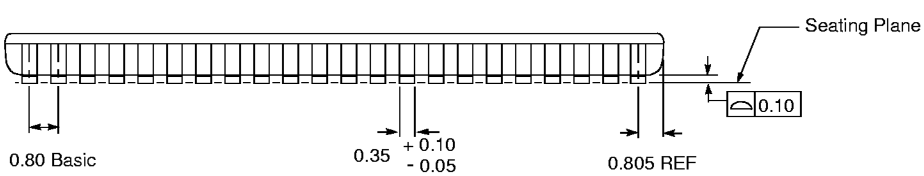
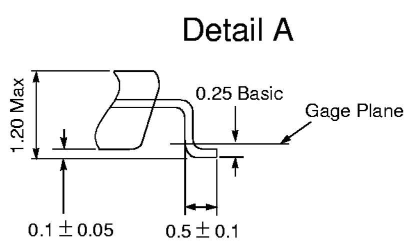
Mechanical Drawings

PACKAGE DIMENSIONS (400mil; 44 lead; Thin Small Outline Package)

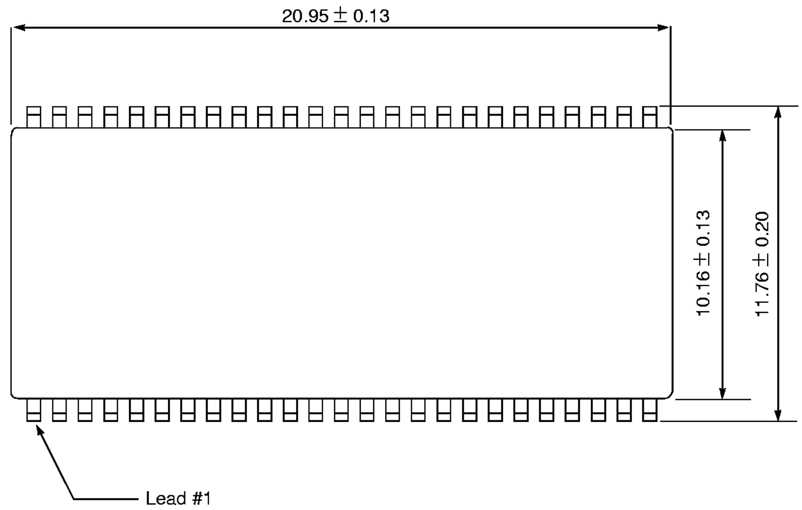


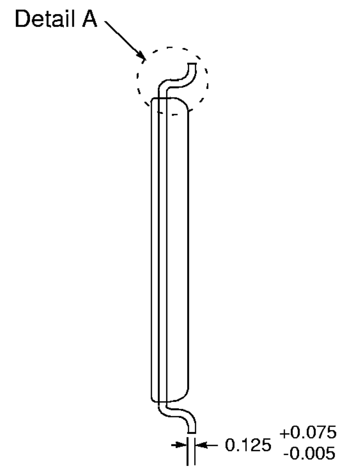


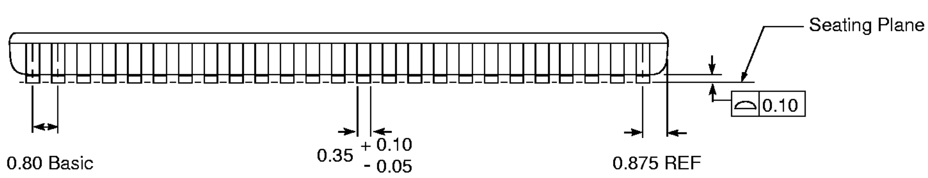


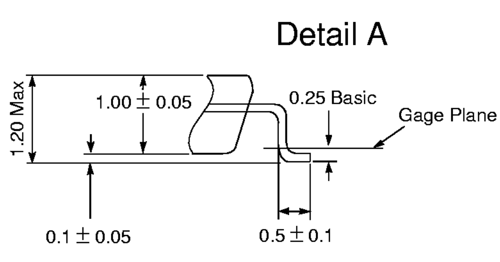
NOTE: All dimensions are in millimeters; Package Diagrams are not drawn to scale.

PACKAGE DIMENSIONS (400mil; 50 lead; Thin Small Outline Package)









NOTE: All dimensions are in millimeters; Package Diagrams are not drawn to scale.

Revision Log

Revision	Date	Summary Of Modification
1.0	7/10/97	Initial Release
1.1	1/27/98	Corrected Current State Truth Table. Modified some timing diagrams to show CL=3 timing. Split t_{HZ} timing spec into t_{HZ1} and t_{HZ2}.
1.2	2/12/98	Added -6ns speed grade and associated timing information. Deleted -12ns speed grade. Modified Icc Operating Current specifications. Added note to AC Characteristics on C_{LOAD} for -6ns speed grade. Added note to Timing Diagrams table of contents regarding CL=2 diagrams.
2.0	3/10/99	Edited for style and consistency. Modified Read Cycle table. Split t_{OH} timing spec into t_{OH1} and t_{OH2}. Added CL=1 timing diagram for AC Parameters for Read Timing. Updated electrical characterization data.

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Ordering Information

Part Number	CAS Latencies	I/O Width	I/O Type	Package	Power Supply	Maximum Operating Frequency (MHz)
SM2402T-6	1, 2, 3	x4	LVTTL, 2.5V	400mil Type II TSOP-44	3.3V	166
SM2403T-6	1, 2, 3	x8	LVTTL, 2.5V	400mil Type II TSOP-44	3.3V	166
SM2404T-6	1, 2, 3	x16	LVTTL, 2.5V	400mil Type II TSOP-50	3.3V	166
SM2402T-7.5	1, 2, 3	x4	LVTTL, 2.5V	400mil Type II TSOP-44	3.3V	133
SM2403T-7.5	1, 2, 3	x8	LVTTL, 2.5V	400mil Type II TSOP-44	3.3V	133
SM2404T-7.5	1, 2, 3	x16	LVTTL, 2.5V	400mil Type II TSOP-50	3.3V	133
SM2402T-10	1, 2, 3	x4	LVTTL, 2.5V	400mil Type II TSOP-44	3.3V	100
SM2403T-10	1, 2, 3	x8	LVTTL, 2.5V	400mil Type II TSOP-44	3.3V	100
SM2404T-10	1, 2, 3	x16	LVTTL, 2.5V	400mil Type II TSOP-50	3.3V	100

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