M5M4V16169RT-10,-12,-15

16MCDRAM:16M(1024K-WORD BY 16-BIT) CACHED DRAM WITH 16K (1024-WORD BY 16-BIT) SRAM

DESCRIPTION

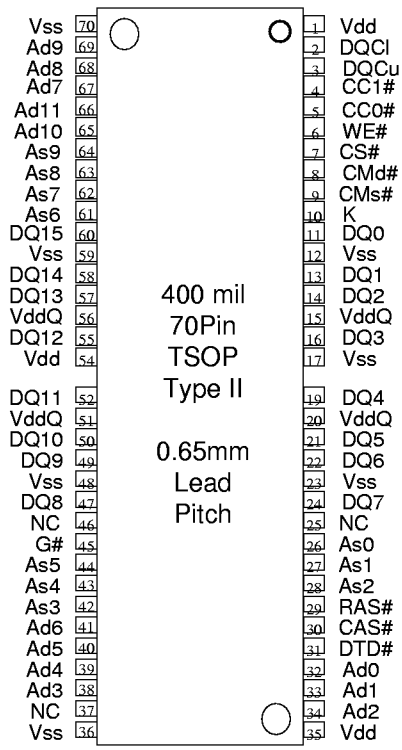
1. The M5M4V16169RT is a 16M-bit Cached DRAM which integrates input registers, a 1,048,576-word by 16-bit dynamic memory array and a 1024 - word by 16-bit static RAM array as a cache memory (block size 8x16) onto a single monolithic circuit. The block data transfer between the DRAM and the data transfer buffers (RB1/RB2/WB1/WB2) is performed in one instruction cycle, a fundamental advantage over the combination of conventional DRAM and SRAM cache.
2. The RAM is fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low cost are essential. The use of quadruple-layer polysilicon process combined with silicide and double layer aluminum wiring technology, a single-transistor dynamic storage stacked capacitor cell, and a six-transistor static storage cache cell provides high circuit density at reduced costs.

FEATURES

Type name	SRAM Access/cycle	DRAM Access/cycle	Power Dissipation (Typ)
M5M4V16169RT-10	10ns/10ns	54ns/80ns	DRAM: 460mW SRAM: 990mW
M5M4V16169RT-12	11ns/12ns	56ns/96ns	DRAM: 400mW SRAM: 860mW
M5M4V16169RT-15	12ns/15ns	65ns/120ns	DRAM: 330mW SRAM: 760mW

- 70-pin,400-mil TSOP (type Ⅱ) with 0.65mm lead pitch and 23.49mm package length.
- Multiplexed DRAM address inputs for reduced pin count and higher system densities.
- Selectable output operation (transparent / latched / registered) using set command register cycle.
- Single 3.3V +/- 0.3V Power Supply. (3.3V +/-0.15V for -10 part)
- 4096 refresh cycles every 64ms (Ad0 –> Ad11).
- Applicable for both direct-mapped and associative systems.
- Synchronous design for precise control with an external clock (K).
- Output retention by advanced mask clock (CMs#).
- All inputs/outputs low capacitance and LVTTL compatible.
- Asynchronous output enable (G#) for bus control.
- Separate DRAM and SRAM address inputs for fast SRAM access.
- Page Mode capability.
- Auto Refresh capability.
- Self Refresh capability.

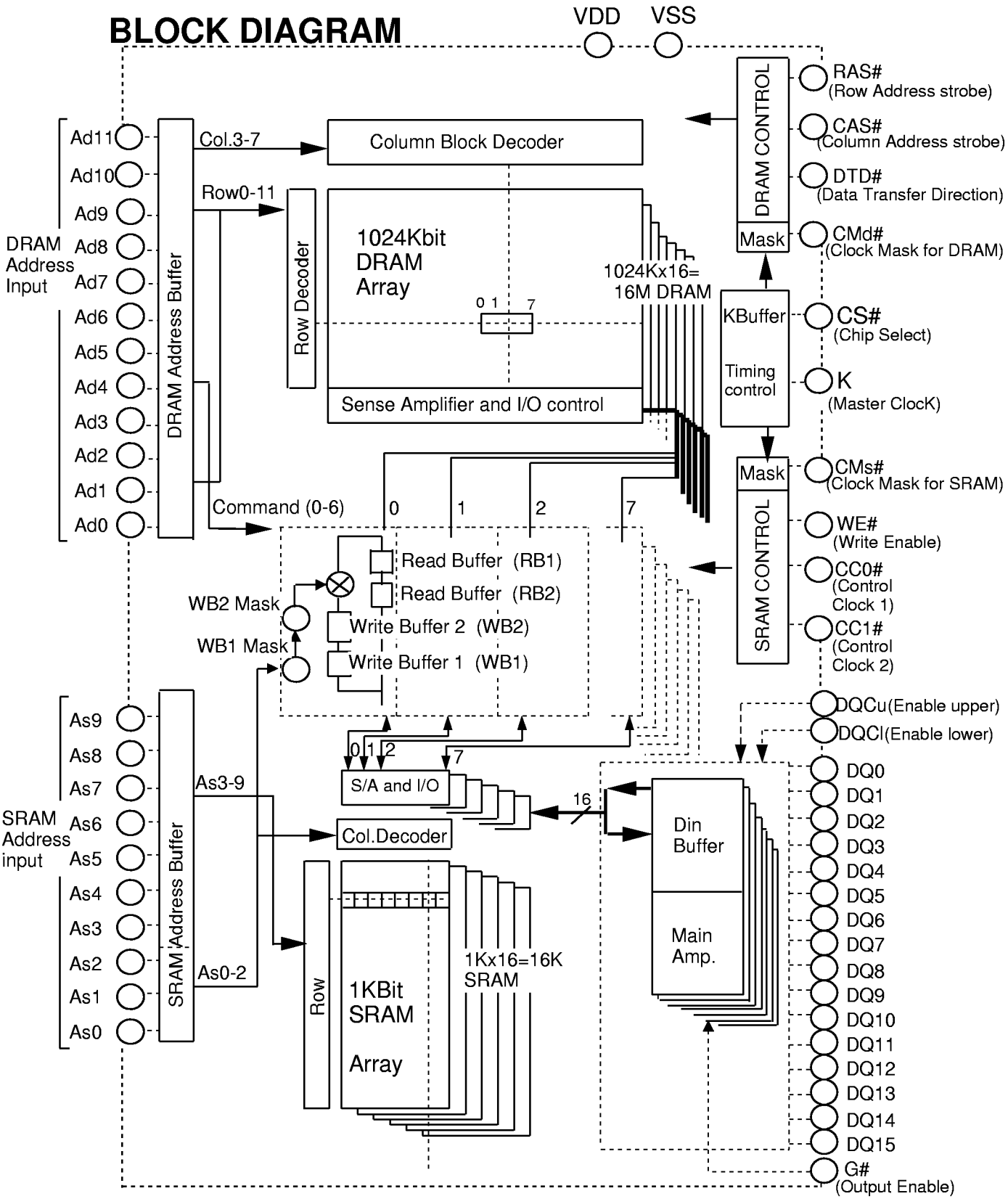
PIN CONFIGURATION (TOP VIEW)



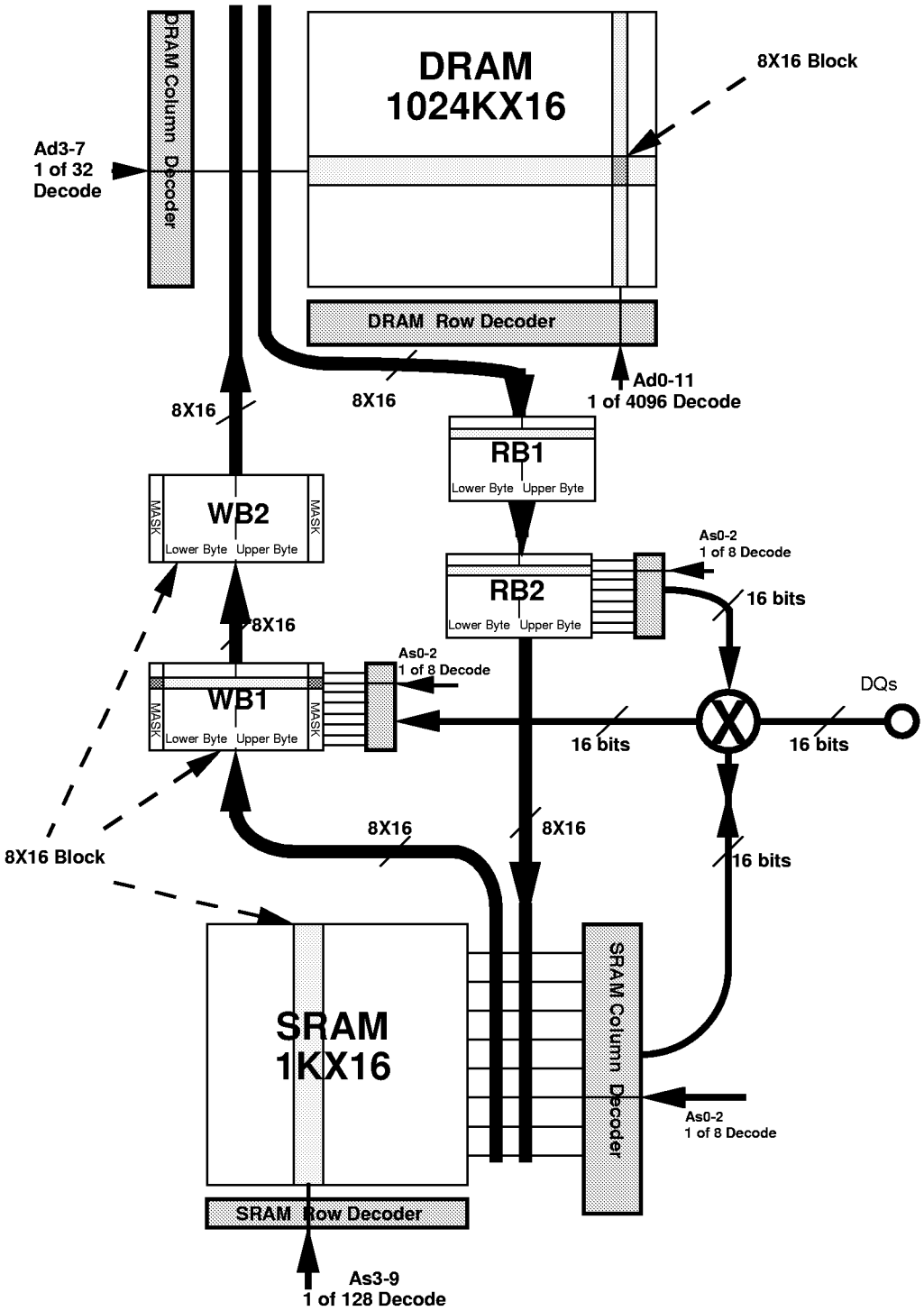
Package code:70P3S-M

K	: Master Clock
CS#	: Chip Select
CMd#	: DRAM Clock Mask
RAS#	: Row Addr. Strobe
CAS#	: Column Addr. Strobe
DTD#	: Data Transfer Direction
Ad	: DRAM Address
CMs#	: SRAM Clock Mask
CC0#,CC1#	: Control Clocks
WE#	: Write Enable
DQC(u/l)	: I/O Byte Control
As	: SRAM Address
G#	: Output Enable
DQ	: Data I/O
Vdd	: Power Supply
VddQ	: DQ Power Supply
Vss	: Ground
VssQ	: DQ Ground

BLOCK DIAGRAM



BLOCK DIAGRAM #2



FUNCTION TRUTH TABLE

Mnemonic CODE		SRAM					As (SRAM address)	DRAM				Ad (DRAM address)			
	CS#	Previous CMs#	CC0#	CC1#	DQC (u/l)	WE#	As0-9	Previous CMd#	RAS#	CAS#	DTD#	Ad0-11	Ad2	Ad1	Ad0
NOP	H	H	X	X	X	X	X	H	X	X	X	X			
SPD	X	L	X	X	X	X	X	X	X	X	X	X			
DES	L	H	H	H	X	X	X	X	X	X	X	X			
SR (10)	L	H	H	L	H/L (11)	H	As0-9	X	X	X	X	X			
SW (10)	L	H	H	L	H/L (11)	L	As0-9	X	X	X	X	X			
BRT	L	H	L	H	L	H	As3-9	X	X	X	X	X			
BWT	L	H	L	H	L	L	As3-9	X	X	X	X	X			
BRTR (10)	L	H	L	H	H/L (11)	H	As0-9	X	X	X	X	X			
BWTW (10)	L	H	L	H	H/L (11)	L	As0-9	X	X	X	X	X			
BR (10)	L	H	L	L	H/L (11)	H	As0-2 (2)	X	X	X	X	X			
BW (10)	L	H	L	L	H/L (11)	L	As0-2 (2)	X	X	X	X	X			
DPD	X	X	X	X	X	X	X	L	X (1)	X (1)	X (1)	X			
DNOP	L	X	X	X	X	X	X	H	H	H	X	X			
DRT	L	X	X	X	X	X	X	H	H	L	H	Ad3-7 (2) (Col.Block)	0	0	0
DWT1	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	0	0
DWT1R	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	0	1
DWT2	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	1	0
DWT2R	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	1	1
ACT	L	X	X	X	X	X	X	H (9)	L	H	H	Ad0-11 (Row Add.)			
PCG	L	X	X	X	X	X	X	H	L	H	L	X			
ARF	L	X	X	X	X	X	X	H (7)	L	L	H	X			
SRF	L	X	X	X	X	X	X	H (8)	L	L	H	X			
SCR	L	X	X	X	X	X	X	H	L	L	L	Command			

NOTES

1) For the DPD function, the RAS#, CAS# and DTD# inputs are DON'T CARE except for the L,L,H combination (Respectively).
2) The unused addresses must be set to Low.
3) Use New: If BW or BWT or BWTW is initiated the same cycle as DWT1 or DWT1R, new data is loaded into the buffer and transferred to DRAM.
4) Clear 1 or 2 Transfer Mask Bits (as addressed by As0-2 and DQCU/L).
5) Actual number of bits transfer depends on the state of the DTBW Mask and the DQCU/DQCL inputs.
Note: If DQC(U/L) is Low, the corresponding DQ(s) is(are) disabled (Input and Output Buffer). SR,SW,BR and BW cycles with DQCU and DQCL Low result in a Deselect SRAM operation.
6) Following a DWT1 or DWT1R cycle, the entire WB1 Transfer Mask is Set (i.e. , data can no longer be transferred from WB1 to DRAM. Succeeding Buffer-Writes or Buffer Write Transfers will Clear Mask bits.
7) CMd# during current cycle must be High (see timing diagram for Auto-Refresh).
8) CMd# during current cycle must be Low (see timing diagram for Self-Refresh).
9) A RAS only refresh can be accomplished by issuing an ACT followed by PCG. (tRC must be observed)
10) These functions can be used with Burst Mode.
11) When DQCU is Low, DQ 15-8 are in a high Z state. When DQCL is Low DQ 7-0 are in a high Z state. See DQCU/L Pin Description for more detail.

FUNCTION TRUTH TABLE

Data Transfer Buffers					DQ pin		Function	
Write Buffers		Xfer Masks						
WB1	WB2	WB1 Mask	WB2 Mask	Read Buffer 1,2	Din	Dout		
–	–	–	–	–	–	Hi-Z	No OPeration	
–	–	–	–	–	–	Suspend	SRAM Power Down& Data retention	No operation
–	–	–	–	–	–	Hi-Z	Deselect SRAM	No operation
–	–	–	–	–	–	Valid	SRAM Read	SRAM->DO
–	–	–	–	–	Valid	Hi-Z	SRAM Write	DIN->SRAM
–	–	–	–	Use	–	Hi-Z	Buffer Read Xfer	RB->SRAM
Load	–	Clear Mask	–	–	–	Hi-Z	Buffer Write Xfer	SRAM->WB1
–	–	–	–	Use	–	Valid	Buffer Read Xfer & Read	RB->SRAM->DO
Load	–	Clear Mask	–	–	Valid	Hi-Z	Buffer Write Xfer & Write	DIN->SRAM->WB1
–	–	–	–	Use	–	Valid	Buffer Read	RB->DO
Load	–	Clear 1 (4) or 2 bits	–	–	Valid	Hi-Z	Buffer Write	DIN->WB1
–	–	–	–	–	–	–	DRAM Power Down	No operation
–	–	–	–	–	–	–	DRAM No OPeration	No operation
–	–	–	–	Load	–	–	DRAM Read Xfer	DRAM->RB1->RB2
Use	Load/ Use	Use (6)	Load/ Use	–	–	–	DRAM Write Xfer1	(3) WB1->WB2->DRAM
Use	Load/ Use	Use (6)	Load/ Use	Load	–	–	DRAM Write Xfer1 & Read	WB1->WB2-> (3) DRAM->RB1->RB2
–	Use	–	Use	–	–	–	DRAM Write Xfer2	WB2->DRAM
–	Use	–	Use	Load	–	–	DRAM Write Xfer & Read	WB2->DRAM-> RB1->RB2
–	–	–	–	–	–	–	DRAM Activate	Page Call
–	–	–	–	–	–	–	DRAM Precharge	
–	–	–	–	–	–	–	Auto Refresh	
–	–	–	–	–	–	–	Self Refresh Entry	
–	–	–	–	–	–	–	Set Command Register	

Function	Data Transferred (max)
Din --> SRAM	8/16 bits (5)
Din --> WB1	8/16bits (5)
SRAM --> WB1	128 bits (8X16bit-block)
WB1 --> WB2	128 bits (8X16bit-block)
WB2 --> DRAM	128 bits (8X16bit-block)
WB2 -> RB1	128 bits (8X16bit-block)
DRAM -> RB1	128 bits (8X16bit-block)
RB1 --> RB2	128 bits (8X16bit-block)
RB2 --> Dout	8/16 bits (5)
RB2 --> SRAM	128 bits (8X16bit-block)

DO: Data Out
DIN: Data In
WB1: Write Buffer 1
WB2: Write Buffer 2
RB1: Read Buffer 1
RB2: Read Buffer 2

Footnotes on previous page.

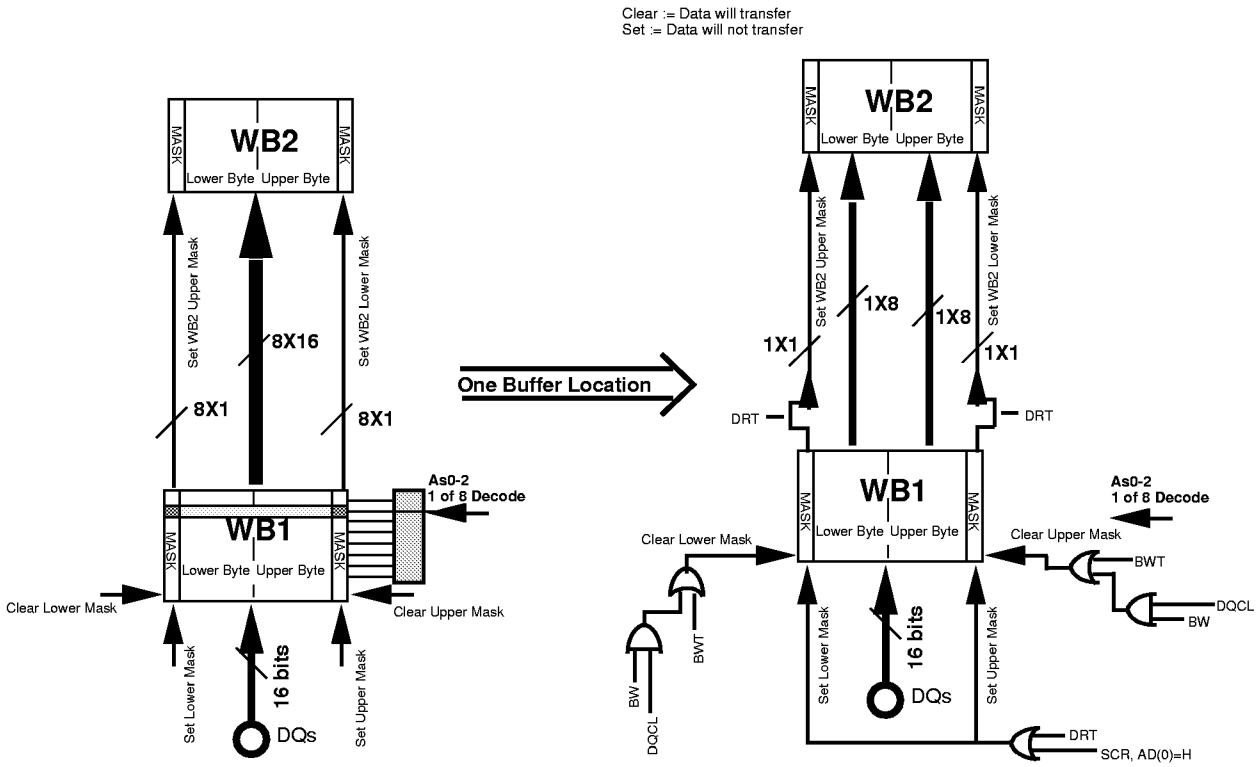
Detail of Write Buffer Transfer Masks:

Write Buffer 1 (WB1) and Write Buffer 2 (WB2) both have a transfer mask associated with them. These masks when not set or "cleared" will allow data that has been written to WB1 to pass to WB2, and from WB2 to the DRAM. When the mask is "set" the data in the write buffer is not allowed to be transferred to WB2 or to the DRAM.

Write Buffer 1 mask:
The transfer mask has two masking bits associate with each of the eight words of data that can be written to the buffer. The two bits per word are associated with DQCU and DQCL. If DQCU or DQCL is used, to mask the I/O while writing to the buffer, the corresponding mask bit is set for the 8-bits not being written and cleared for those that are being written. Otherwise if DQCU/L are not used to mask the I/O during a buffer write both bits associated with the buffer write address are cleared. The mask bits that are cleared will allow the data written to their corresponding address to pass to the WB2 during a DRT or a DRTR. At the same time the data is transferred the contents of WB1 mask is transferred to the WB2 mask.

The mask associated with WB1 is cleared during a buffer write (BW), buffer write transfer (BWT), or buffer write transfer write (BWTW). In the case of the BWTW all bits are cleared except those associated with the the buffer address. The two bits that correspond to the buffer address are set according to DQCU and DQCL. The mask is set with a dram read transfer (DRT), dram read transfer read (DRTR), or an SCR with Ad(0) = H.

Write Buffer 2 mask:
The WB2 mask is set from the state of the WB1 mask when a DRT or a DRTR occurs. The mask data from the WB1 is held in the WB2 mask until another DRT or DRTR occurs. If a bit is set in the WB2 mask the data will not be transferred to the DRAM. If the bit is cleared the data will be allowed to transfer to the DRAM.



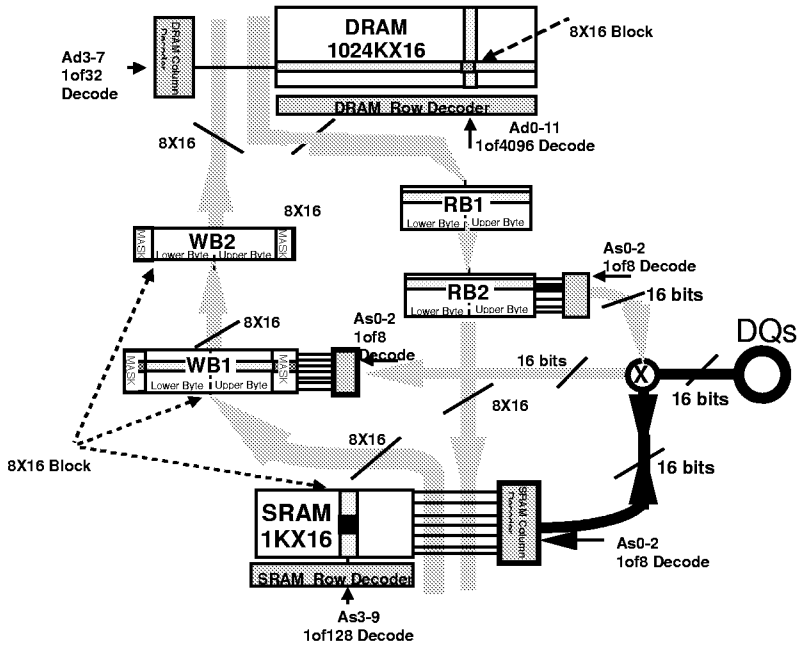
PIN DESCRIPTIONS(1)

K	Input	Master Clock Provides the fundamental timing and the internal clock frequency for the CDRAM. All external timing parameters (with the exception of G# in read cycle and CMd# in Self refresh cycle) are specified with respect to either the rising or falling edge of K.
CMd#	Input	DRAM Clock Mask controls the operation of the internal DRAM master clock (K). When CMd# is Low at the rising edge of K, the internal DRAM master clock (K) for the following cycle is ceased and input stages are powered-off, resulting in a DRAM Power Down.
RAS#	Input	Row Address Strobe is used in conjunction with Master clock K (depending on the states of CMd#, CAS#, and DTD#) to activate the DRAM (latching the Row Address lines and accessing 1 of 4096 rows), initiate a DRAM precharge cycle, perform a DRAM Read or Write Transfer, DRAM Write Transfer & Read, set the command registers, start an Auto-Refresh cycle, enter a Self-Refresh cycle,create a DRAM NOP cycle, or power down the DRAM.
CAS#	Input	Column Address Strobe is used in conjunction with the Master Clock K to latch the Column addresses. When preceded by RAS# in a DRAM access cycle, CAS# initiates a DRAM Write Transfer (WB1/2 -> DRAM, if DTD#=L), DRAM Write Transfer & Read (WB1/2 -> DRAM -> RB, if DTD#=L) or DRAM Read Transfer (DRAM -> RB, if DTD#=H), depending on the state of DTD# (see DTD# pin description).
DTD#	Input	Data Transfer Direction controls DRAM-to-RB(read) / WB-to-DRAM (write) direction. If preceded by a RAS# low cycle, both CAS# and DTD# low (on the rising edge of K) initiate a DRAM Write Transfer cycle. If DTD# stays High with the above conditions, a DRAM Read Transfer cycle results. DTD# can also initiate DRAM Activate, DRAM Precharge, Auto-Refresh, Set-Command Register, and Self Refresh cycles.
Ad0-Ad11	Input	DRAM Address Lines are Multiplexed to reduce pin count. Ad0-Ad11 (@ RAS=low,CAS=high,DTD=high, K=Rising edge) specify the Row Address of the DRAM to activate and refresh the selected page and Ad3-Ad7 (@ RAS=high,CAS=low,K=Rising edge) specify the Block Address of the DRAM. In addition, Ad0-Ad2 (@ RAS=high,CAS=low, K=Rising edge) specify the transfer operation of the DRAM . Also Ad0-Ad11 (@RAS=low,CAS=low, DTD=low, K=Rising Edge) are used as the command in set command register cycle.
CS#	Input	The Chip Select controls the operation of the CDRAM. When CSd#=H at the rising edge of K and the previous CMd# or CMs# is high, the chip is in No Operation mode.
CMs#	Input	SRAM Clock Mask controls the operation of the internal SRAM master clock (Ks). When CMs# is asserted at a rising edge of K, the internal SRAM master clock for the following cycle is suspended, resulting in the power down of the SRAM portion of the circuit, including the Sense Amps. CMs# can also be used to retain output data during SRAM power-down.

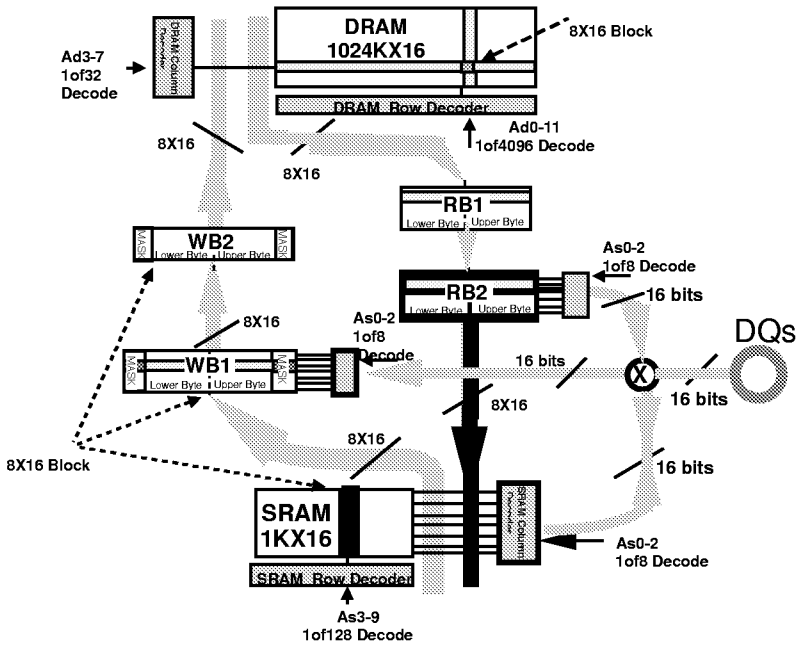
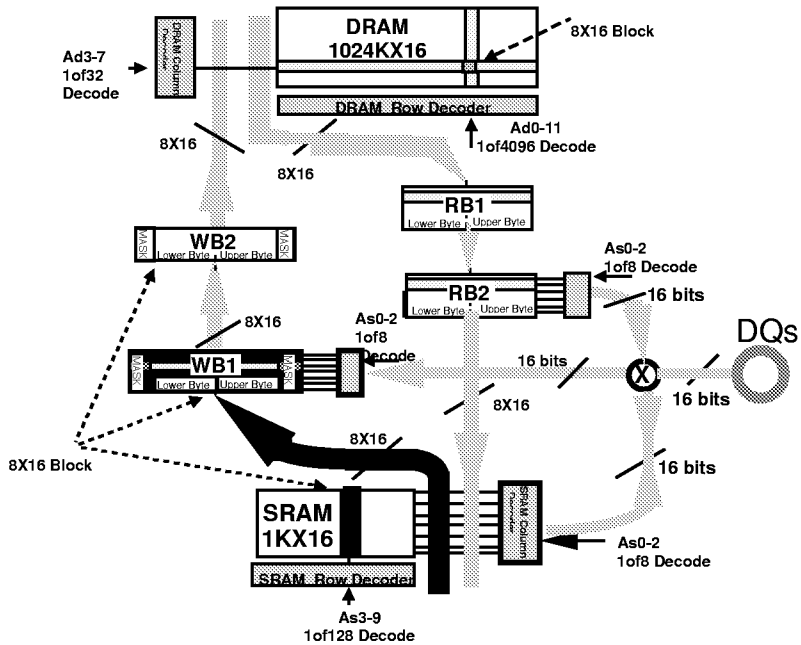
PIN DESCRIPTIONS(2)

DQCu,DQCl	Input	DQCu/l are I/OByte control signals. If G#=Low, DQCu/l have a control of output impedence: DQCu controls upper DQs (DQ8-15) & DQCl controls lower DQs (DQ0-7). DQCu/l also control both input data during SRAM Writes or Buffer Writes and transfer mask during Buffer Writes. (WB1 transfer Mask for each byte is written (bits are cleared) during Buffer Writes depending on DQCu/l inputs.)
WE#	Input	Write Enable controls SRAM and Buffer read and write operations. A high on the WE# pin causes either a Buffer Read, SRAM Read, Buffer Read Transfer and/or a Buffer Read Transfer & Read to occur (depending on the state of the CC0# and CC1# bits). A low on the WE# pin causes either a Buffer Write, SRAM Write, Buffer Write Transfer and/or a Buffer Write Transfer & Write to occur (depending on the state of the CC0# and CC1# inputs)
CC0#,CC1#	Inputs	The Control Clock Inputs control SRAM and Buffer operations. CC0# is Low for all Buffer Writes, Reads, and Transfers, and High for all other SRAM operations. CC1# is high for all Buffer Read Transfers and Buffer Write Transfers .
As0-As9	Inputs	SRAM Addresses are non-multiplexed, and access 1024 - 16-bit words (configured as 128 Rows X 8 Columns X 16 Bits, where the Block Size is 8 X 16) in the SRAM array. As0-As2 select word address within a block, and As3-As9 select the SRAM row(block).
G#	Input	The Output Enable is an asynchronous input. G#=high forces the outputs to high impedence.
DQ0-DQ15	Inputs / Outputs	Output operation is either transparent, latched, or registered depending on the state of the command register. The Data Lines for the CDRAM are asynchronously controlled by G#.

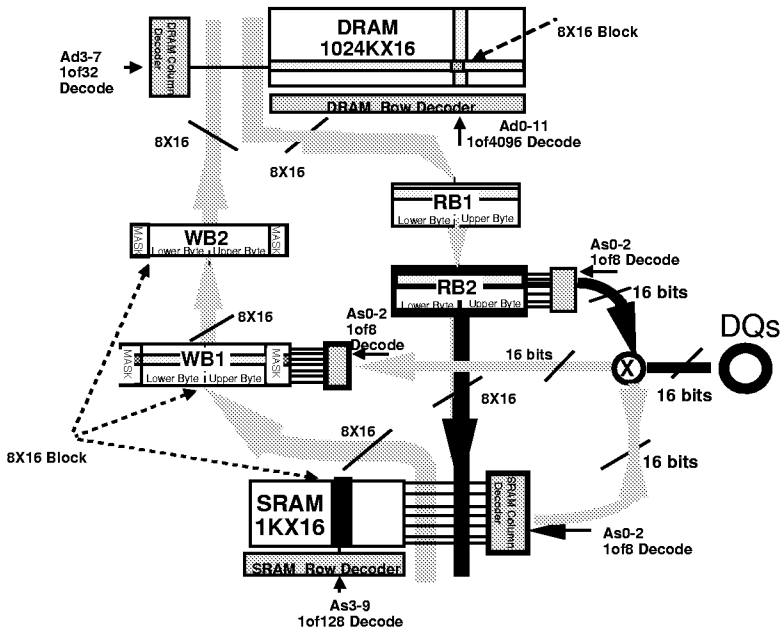
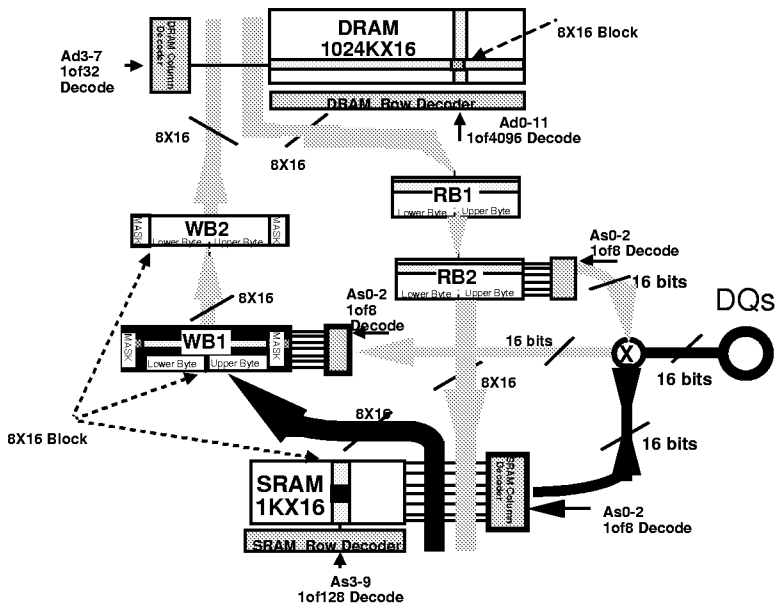
MODE DESCRIPTIONS (1)

NOP	No Operation. Outputs are high-impedance. All input buffers remain active.
SRAM Power-Down	If CMs#=Low at the rising edge of K, the SRAM enters SRAM Power Down at the next rising edge of K. During this mode, the internal SRAM K clock becomes inactive. The Output Buffers remain enabled and are controlled by G#. All input buffers of SRAM clocks and SRAM addresses are inactive.
Deselect SRAM	All transfer functions and input/output operations to and from the SRAM and Buffer are disabled. This cycle is useful for output impedence control (Hi-Z,Low-Z) without G#. Output buffers are active during this cycle for registered output mode control.
SRAM Read	Data is read from the SRAM to the I/O pins. Addresses As0-As9 are used to select the data to be read. As3-As9 decode the SRAM Row (=Block), and As0-As2 decode (1 of 8) the 16-bit word. DQCu and DQCl control the impedence (High-Z/Low-Z) of the upper and lower bytes, respectively.
SRAM Write	Data is written from the I/O pins to the SRAM. Addresses As0-As9 are used to select the location to be written. As3-As9 decode the SRAM Row (=Block), and As0-As2 decode (1of8) the 16-bit word to be written. DQCu and DQCl control Upper and Lower byte writes, respectively. 

MODE DESCRIPTIONS (2)

Buffer Read Transfer	Data is transferred from the Read Buffer (RB2) to the SRAM. Addresses As3-9 select the SRAM row to which the 8X16 bit block is to be written. Addresses As0-As2 must be set low. 
Buffer Write Transfer	Data is transferred from the SRAM to the Write-Buffer1 (WB1). Addresses As3-As9 decode the SRAM Row (=8X16 bit block) to be transferred. Addresses As0-As2 must be set low. The Buffer Write Transfer cycle "clears" all transfer mask bits in the WB1 Mask (allowing all data to be transferred in a successive DRAM Write Transfer cycle). 

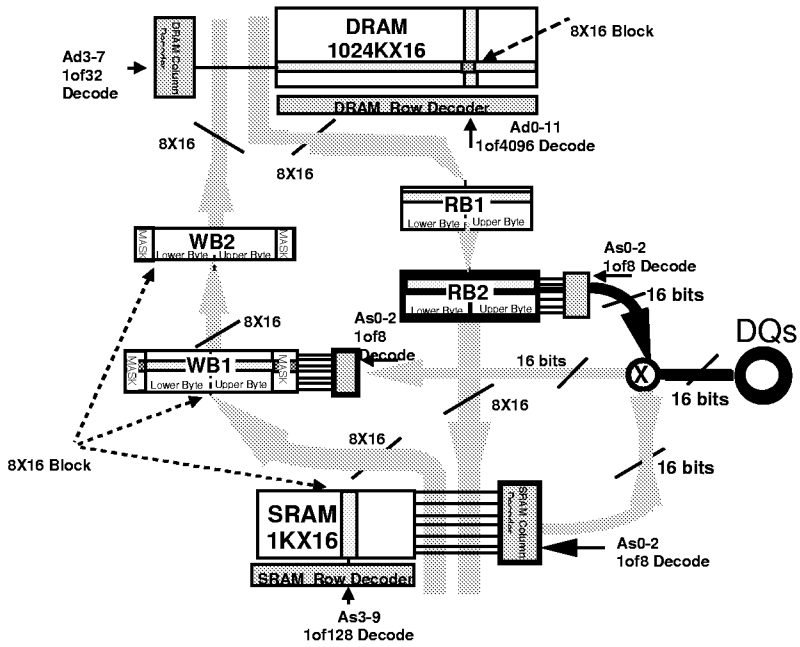
MODE DESCRIPTIONS (3)

Buffer Read Transfer & SRAM Read	Data is transferred from the Read Buffer (RB2) to the SRAM, and simultaneously, data (16 bit word) is read from the RB to the I/O pins. Addresses As3-9 select the SRAM Row to which the 8X16 bit block is to be written. Addresses As0-As2 decode the 16-bit word to be read. 
Buffer Write Transfer & SRAM Write	Data is first written from the I/O pins to SRAM as decoded by As0-As9. Then, the SRAM Row (=Block) decoded by As3-As9 is transferred to the Write-Buffer1 (WB1). The Buffer Write Transfer cycle "clears" all transfer mask bits in the WB1 Mask (allowing all data to be transferred in a successive DRAM Write Transfer cycle). DQCu and DQCl control upper and lower byte writes respectively, however all transfer mask bits in the WB1 are cleared. 

MODE DESCRIPTIONS (4)

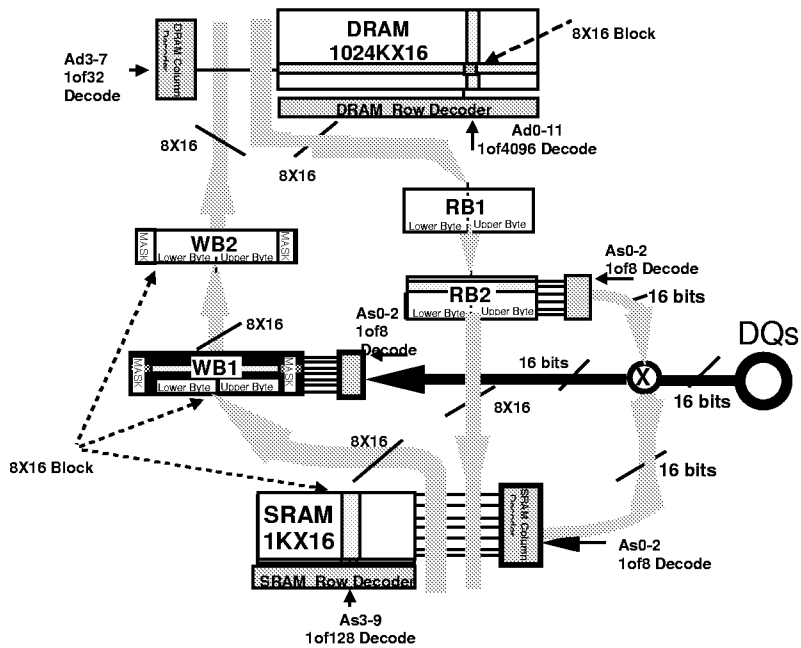
Buffer Read

Data is read from the Read Buffer (RB2) to the I/O pins. Addresses As0-As2 are used to select (1 of 8) the 16-bit word to be read. Addresses As3-As9 must be set low for this operation.

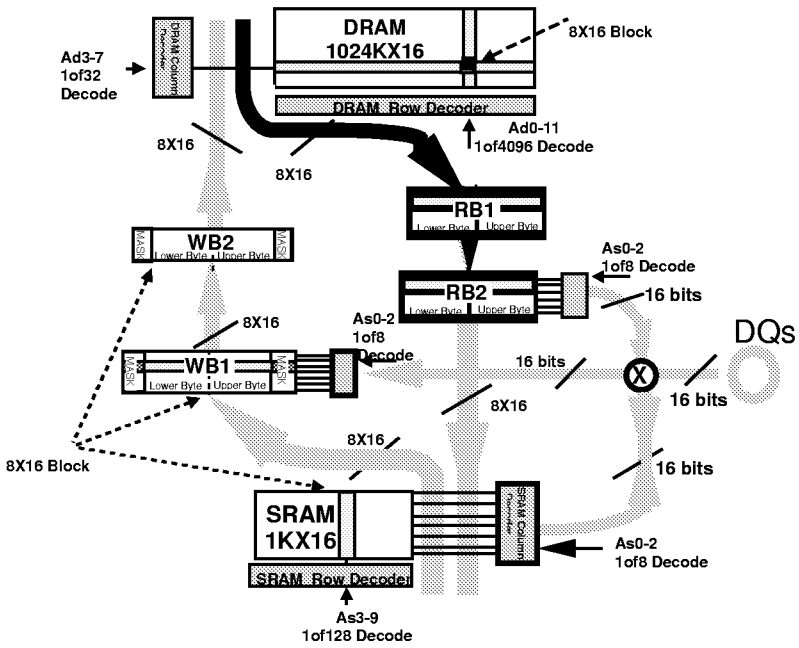


Buffer Write

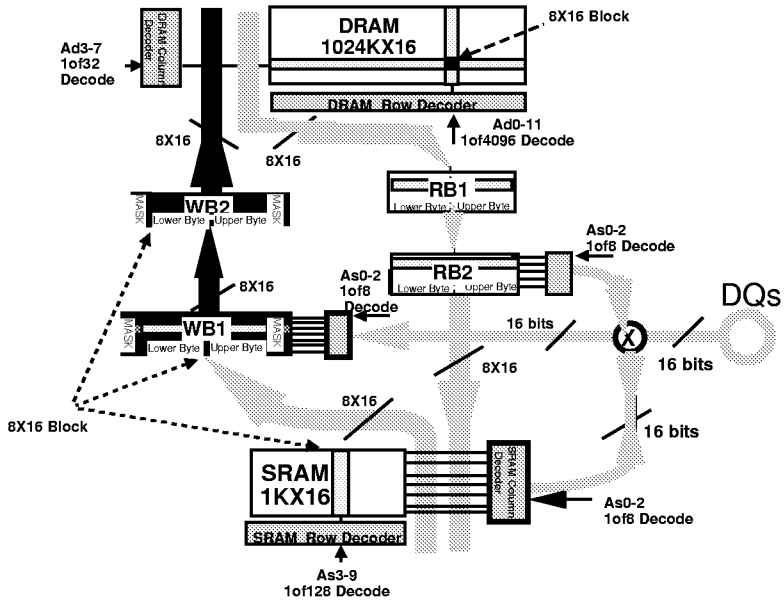
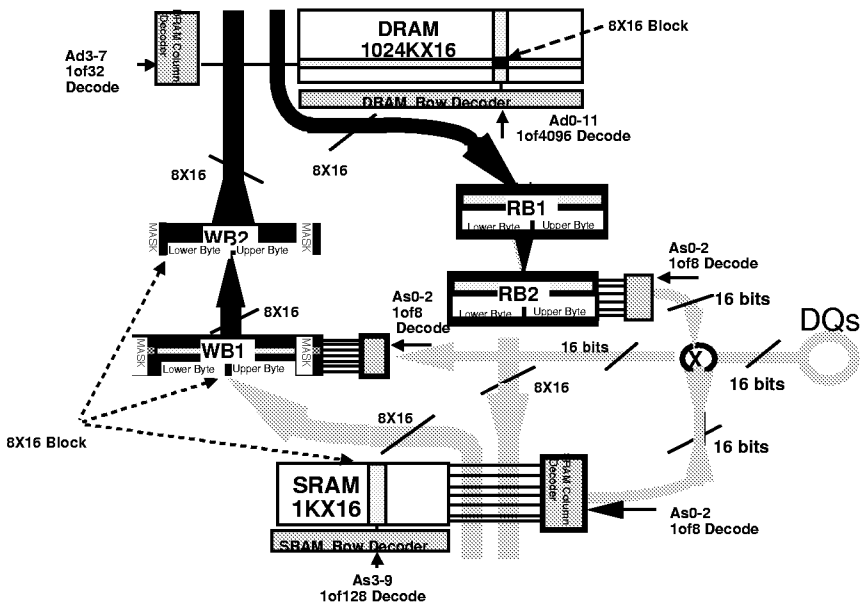
Data is written from the I/O pins to the Write-Buffer1. Addresses As0-A2 are used to select (1of8) the 16-bit word to be written. Addresses As3-As9 must be set low for this operation. The transfer mask bits associated with the Upper and Lower bytes are cleared in the WB1 Mask. DQCu and DQCl control Upper and Lower byte writes (and associated tranfer mask bits), respectively.



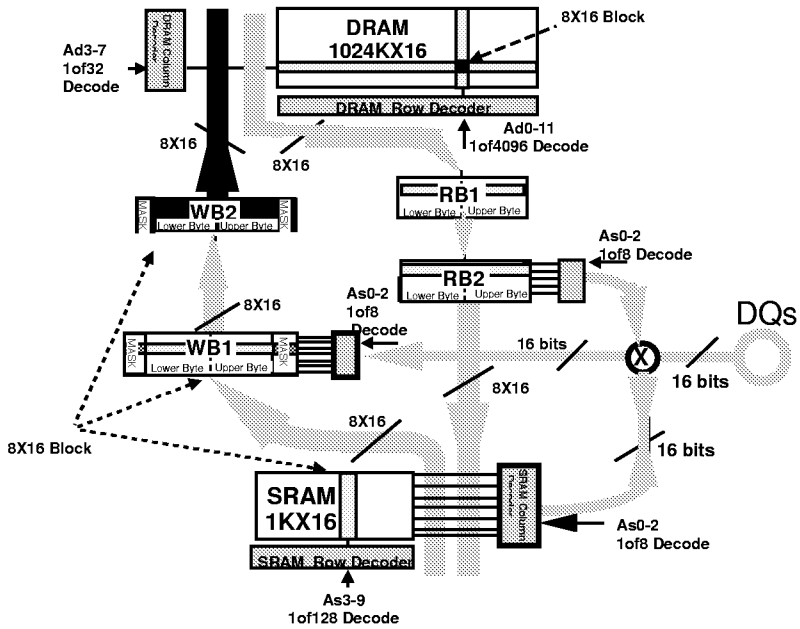
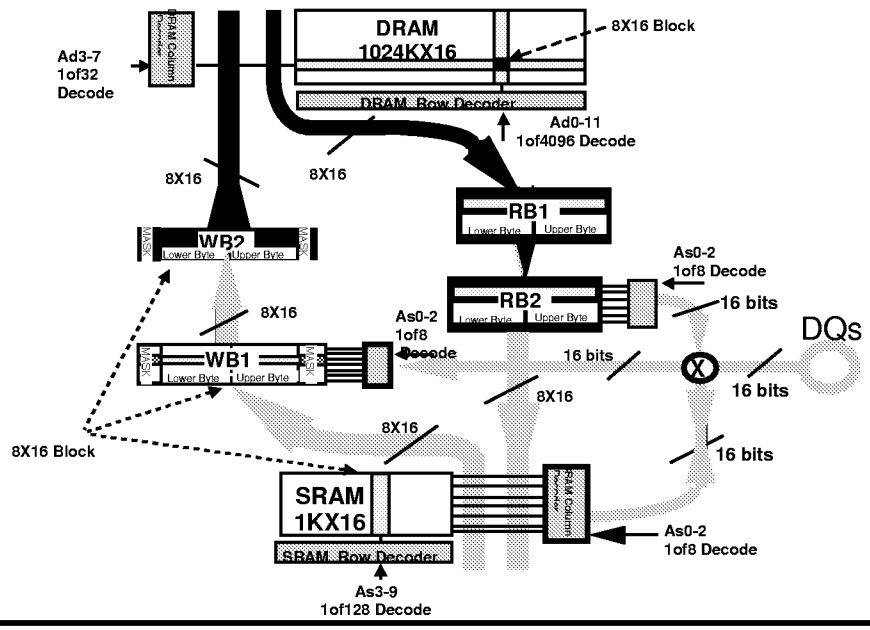
MODE DESCRIPTIONS (5)

DRAM Power-Down	If CMd#=Low at the rising edge of K, the DRAM enters DRAM Power Down at the next rising edge of K. During this mode, the internal DRAM K clock becomes inactive. Also all input buffers of DRAM clocks and DRAM addresses are inactive. Note that the latency of DRAM Read Transfer cycle is not counted up in this cycle.
DRAM NOP	The DNOP cycle is used when no other DRAM operations are desired, holding the DRAM in its present (precharge/activate) state.
DRAM Read Transfer	A Block (8X16) is transferred from the DRAM to the Read Buffer (RB1/RB2) as specified by Addresses Ad3-Ad7. Addresses Ad8-Ad11 must be set to Low. After the Latency Period (specified in the Access Latency Table) new data will be present in the Read Buffers. Prior to the Latency timeout, old data will be present in RB2. (Notes 1,2,4) 

MODE DESCRIPTIONS (6)

DRAM Write Transfer1	Data (8X16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad11 must be set to Low. The Mask present in WB1 is also transferred to WB2 and controls the data written to the DRAM. After data has been transferred from WB1, the entire WB1 Mask is Set. (Notes 3,4) 
DRAM Write Transfer1 & Read	Data (8X16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad11 must be set to Low. The Mask present in WB1 is also transferred to WB2 and controls the data written to the DRAM. The block to which the data is written in the DRAM is simultaneously transfered to the Read Buffers. (Notes 2,3,4) 

MODE DESCRIPTIONS (7)

DRAM Write Transfer2	Data (8X16 Block) is transferred from WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad11 must be set to Low. The WB2 Mask controls the data written to the DRAM. With the DWT2 function, the WB2 data and WB2 Mask remain unchanged. (Note 4) 
DRAM Write Transfer2 & Read	Data (8X16 Block) is transferred from WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad11 must be set to Low. The WB2 transfer mask controls the data written to the DRAM. With the DWT2 function, the WB2 data and WB2 transfer mask remain unchanged. The block to which the data is written in DRAM is simultaneously transferred to the Read Buffers. (Notes 1,2,4) 

MODE DESCRIPTIONS (8)

DRAM Activate	Addresses are latched from the Ad0-Ad11 inputs by the rising edge of K. Internally, a DRAM row is selected (Page Call) in preparation for a DRAM Read or Write Transfer cycle. A DRAM Precharge cycle must separate all DRAM Activate cycles.
DRAM Precharge	Internally, the active DRAM row is deselected (completing the refresh process) and page-mode is disabled. The DRAM is precharged prior to another DRAM Activate cycle.
DRAM Auto-Refresh	Internally, a DRAM row is selected and refreshed (as addressed by an internal, self-incrementing counter), followed by an internally generated Precharge cycle. The Auto refresh cycle can be implemented only if the DRAM is in Precharge state (i.e., a Precharge or Auto-Refresh cycle occurred more recently than an Acitvate cycle). After an Auto refresh cycle the DRAM is in left in a Precharged state. DRAM Auto-Refresh is similar to a CAS-Before-RAS (CBR) mode in standard DRAMs.
DRAM Self Refresh	All clock buffers are suspended, and CMd# asynchronously controls Self Refresh (CMd# rising edge initiates exit from Self Refresh). During Self Refresh, device enters a low power mode, the DRAM is automaticaly refreshed during this mode. A DNOP must be performed after exiting Self Refresh mode.
Set Command Register	When SCR is initiated,the addresses present on the Ad0-Ad11 DRAM Address pins determine the DRAM Read/Write Transfer Latency, the Output Mode (transparent / latched / registered), and WB1 transfer mask mode (set-all/ no change). No DRAM operation is executed in this cycle. Refer to the SCR truth table for legal address values. During SCR cycle and the following 3 clock cycles(totally 4 clock cycles), only NOP,DNOP or DPD are allowed in DRAM portion and only NOP,DES or SPD are done in SRAM portion. The set commands are valid at least after the above 4 clocks later and the previous function is not guaranteed to work if it has not been completed.(i.e. DRT ,DWT1&R,DWT2&R and SR,BR and BRTR with registered output mode.)

Notes:
1) This function is performed in a latency period specified in the access latency table.
2) After the latency period (specified in the access latency table) new data will be present in the read buffers. Prior to the latency timeout, old data will be present in RB1/RB2.
3) After data has been transferred from WB1, the entire WB1 mask is set.
4) Valid Ad0-Ad2 addresses are shown in the FUNCTION TRUTH TABLE..

Power-On sequence

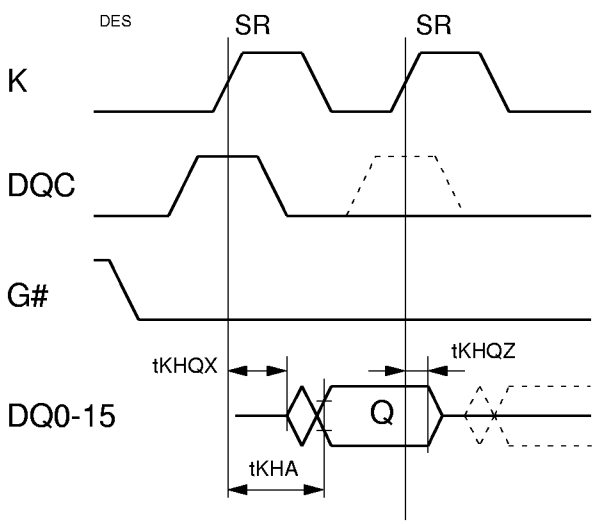
Before starting normal operation, the following power on sequence is necessary.

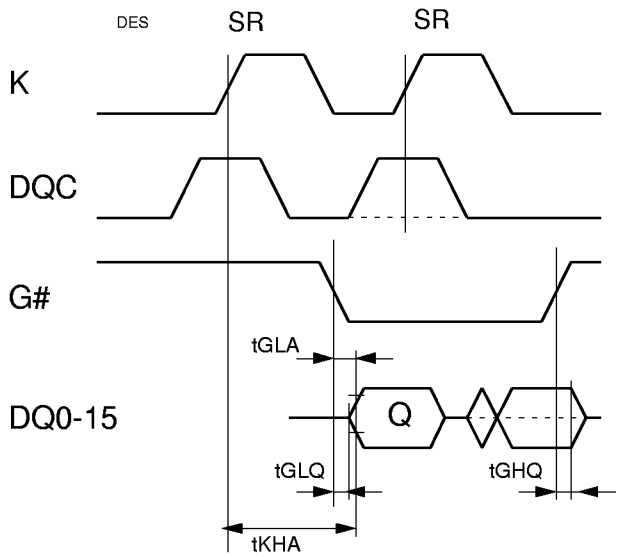
1) Apply power and maintain stable power (pause) for 500us. When power is applied the DQ pins assume a Hi-Z state and remainin this condition until an SRAM or Buffer read operation is performed.
2) Perform a precharge (PCG) operation.
3) After tRP, perform 8 auto refresh commands (ARF) with adequate interval (tRC).
4) Issue concurrent set command register (SCR) and deselect (DES) to initilize the mode register.

After this sequence, the RAM is in idle state and ready for normal operation.
Note that DNOP / DPD and DES / SPD or NOP command will be the stand-by command for the above power sequence.

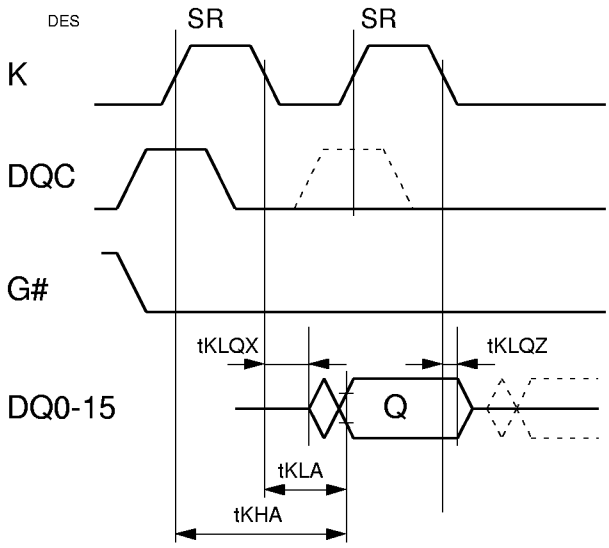
Output Operations

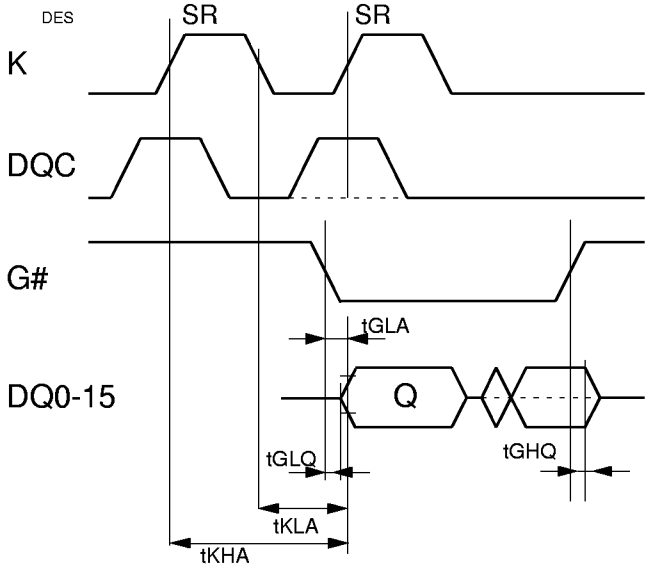
Transparent



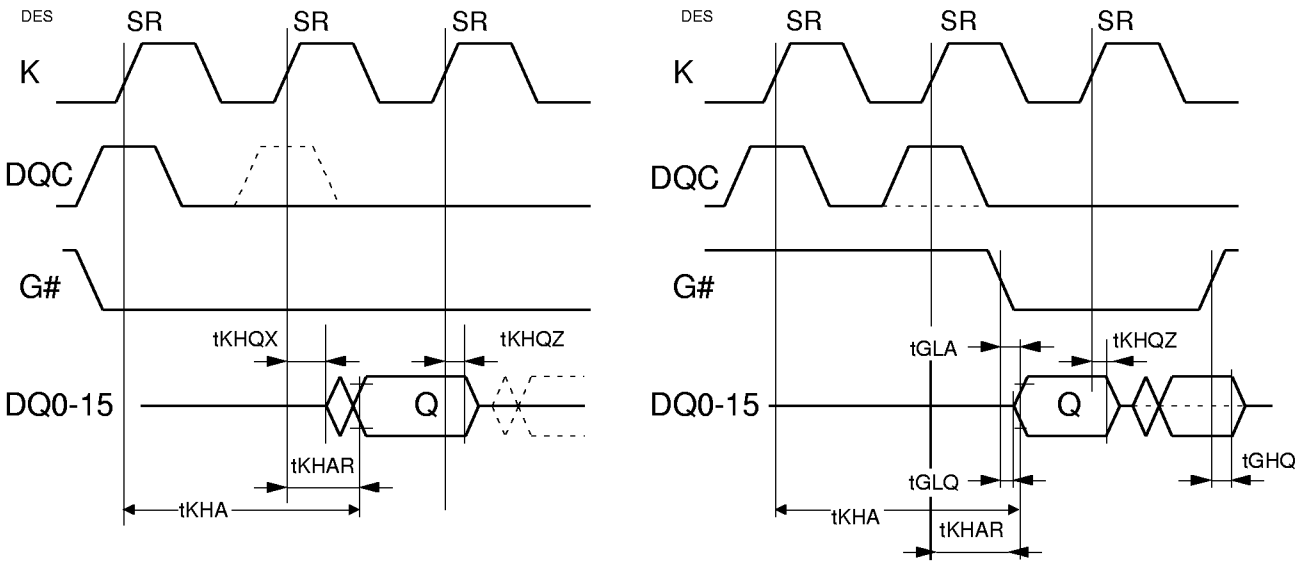


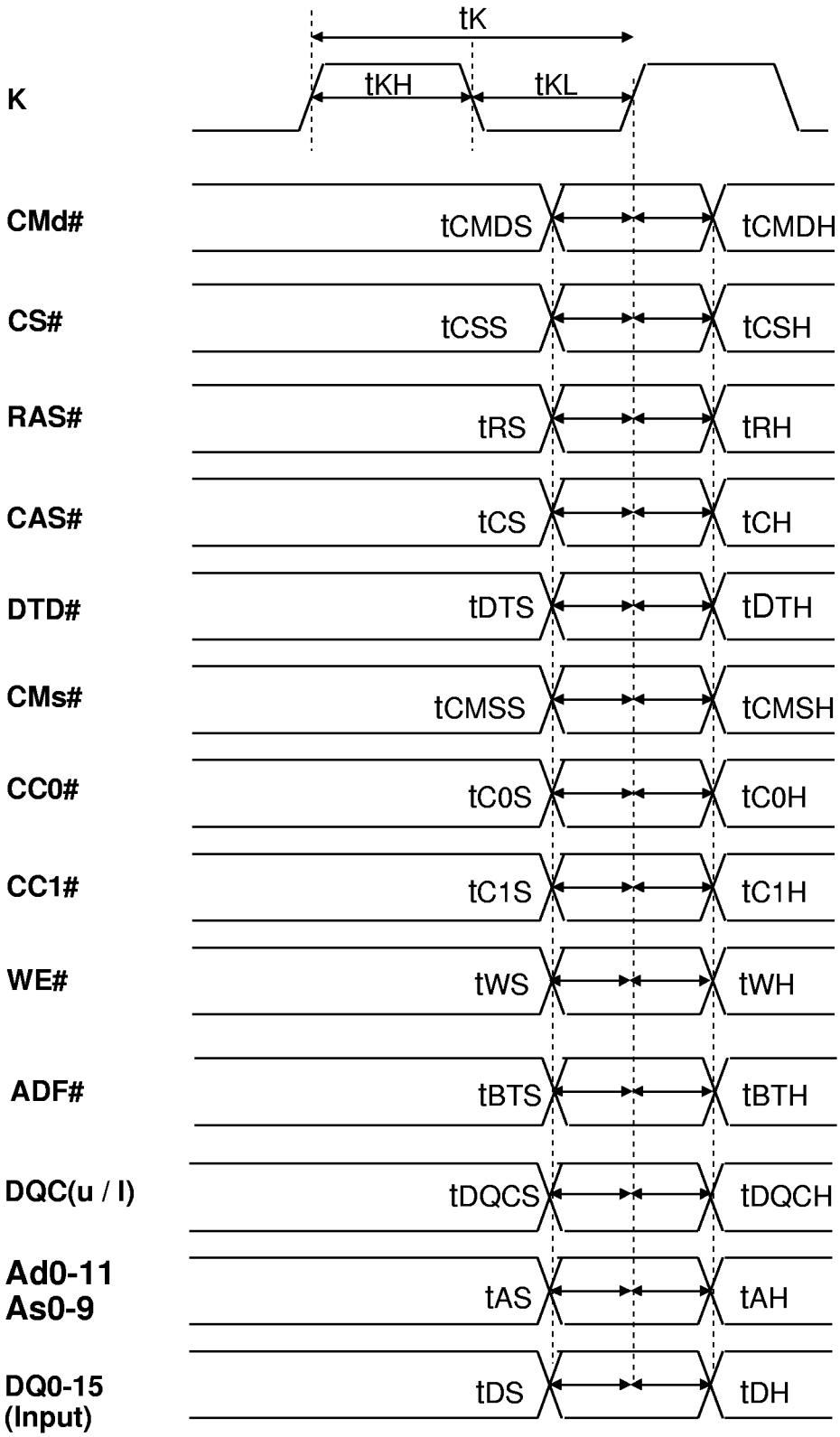
Latched





Registered


DES
SR
SR
SR
K
DQC
G#
tKHQX
tKHQZ
DQ0-15
Q
tKHAR
tKHA
DES
SR
SR
SR
K
DQC
G#
tGLA
tKHQZ
DQ0-15
Q
tGHQ
tGLQ
tKHA
tKHAR


tK
K
tKH
tKL
CMd#
tCMDS
tCMDH
CS#
tCSS
tCSH
RAS#
tRS
tRH
CAS#
tCS
tCH
DTD#
tDTS
tDTH
CMs#
tCMSS
tCMSH
CC0#
tC0S
tC0H
CC1#
tC1S
tC1H
WE#
tWS
tWH
ADF#
tBTS
tBTH
DQC(u / l)
tDQCS
tDQCH
Ad0-11
As0-9
tAS
tAH
DQ0-15
(Input)
tDS
tDH

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	With respect to Vss	–0.5 ~ 4.6	V
VI	Input Voltage		–0.5 ~ 4.6	V
VO	Output Voltage		–0.5 ~ 4.6	V
IO	Output Current		50	mA
Pd	Power Dissipation		1000	mW
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		–65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max	
Vdd	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
$V_{IH(A)}$	High-level Input Voltage address inputs	2.0		Vdd+0.3	V
$V_{IH(C)}$	High-level Input Voltage clock inputs	2.0		Vdd+0.3	V
$V_{IH(DQ)}$	High-level Input Voltage DQ inputs	2.0		3.6	V
V_{IL}	Low-level Input Voltage all inputs	–0.3		0.8	V

CAPACITANCE

(Ta=0~70°C, Vdd=3.3±0.3V for -12 and -15, Vdd=3.3V±0.15V for -10
Vss=0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits (MAX)	Unit
$C_{I(A)}$	Input Capacitance, Address pin	VI=Vss	5	pF
$C_{I(C)}$	Input Capacitance, Clock pin	f=1MHz	7	pF
$C_{I/O}$	Input Capacitance, I/O pin	VI=25mVrms	8	pF

AVERAGE SUPPLY CURRENT from Vcc

(Ta=0~70°C, Vdd=3.3±0.3V for -12 and -15, Vdd=3.3V±0.15V for -10
Vss=0V, unless otherwise noted)

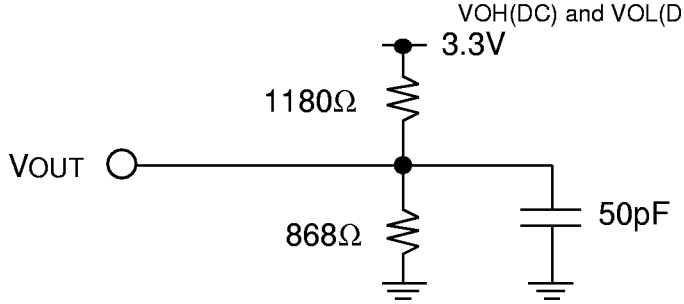
Symbol	Condition	Limits (MAX)			Unit
		-10	-12	-15	
IccS	Average supply current of SRAM operating, tK=min. DRAM=DPD output open data input=H or L	300	260	230	mA
IccD	Average supply current of DRAM operating, tRC=min. SRAM=SPD	140	120	100	mA
IccD(PG)	Average supply current of DRAM page-mode tPC=min. SRAM=SPD	180	150	120	mA
Icc(STN1)	LVTTL standby, tK=min, DRAM=DNOP & SRAM=DES, or NOP all input=stable. output open data input=H or L	75	65	55	mA
Icc(STN2)	CMOS standby, tK=min, DRAM=DNOP & SRAM=DES, or NOP all input=stable. output open data input=H or L	45	40	35	mA
Icc(PD)	CMOS Power Down current, CMd#=CMs#=L,tK=min.	5	5	5	mA
Icc(SRF)	CMOS Self Refresh current, CMd#=CMs#=L,tK=∞	1	1	1	mA

AC OPERATING CONDITIONS AND CHARACTERISTICS

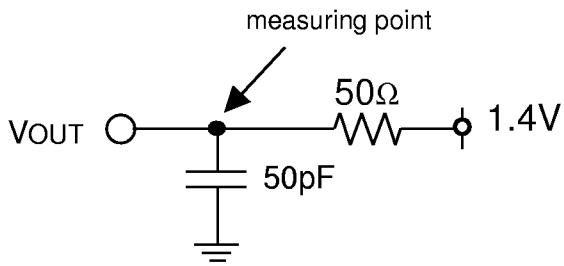
(Ta=0~70°C, Vdd=3.3±0.3V for -12 and -15, Vdd=3.3V±0.15V for -10
Vss=0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Unit
			Min.	Max	
VOH(DC)*	High-level Output Voltage (DC)	IOH= –2mA	2.4	-	V
VOL(DC)*	Low-level Output Voltage (DC)	IOL= +2mA	-	0.4	V
VOH(AC)*	High-level Output Voltage (AC)	50Ω serial termination	1/2 Vcc	-	V
VOL(AC)*	Low-level Output Voltage (AC)	50Ω serial termination	-	1/2 Vcc	V
IOZ	Off-state Output Current	Q floating VO=0 ~ VddQ	–10	10	µA
II	Input Current	VIH=0 ~ VddQ+0.3V	–10	10	µA

* VOH(AC) and VOL(AC) are the reference levels for AC measurements.
VOH(DC) and VOL(DC) are the final levels the outputs reach.



DC Condition
(VOH min , VOL max)



AC Condition
(Access Time)

TIMING REQUIREMENTS (CLK pulse, input signals setup / hold time to CLK edge)

(Ta=0~70°C, Vdd=3.3±0.3V for -12 and -15, Vdd=3.3V±0.15V for -10
Vss=0V, unless otherwise noted)

Input Pulse Levels: 0 to 3.0V

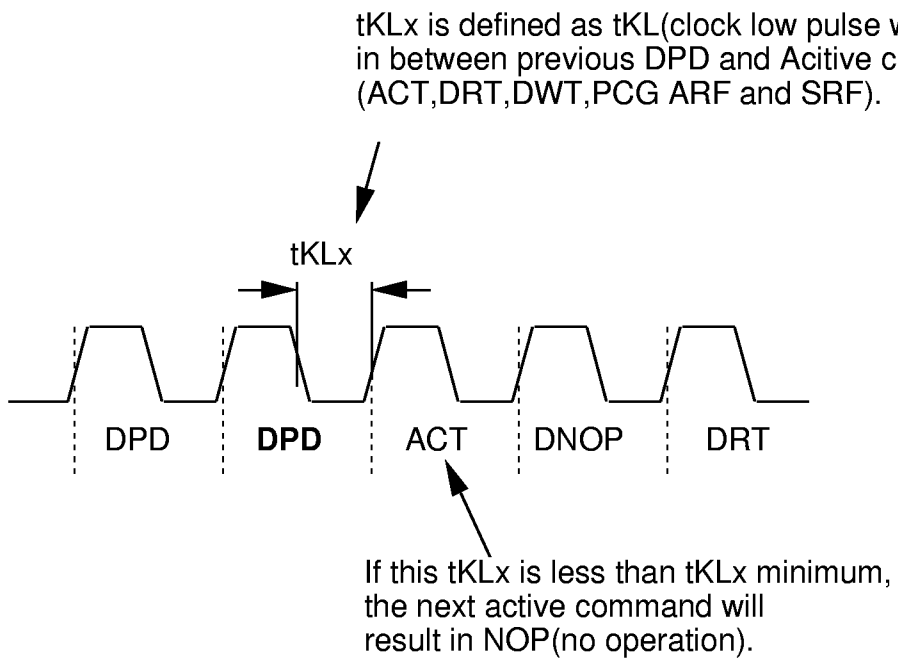
Input Timing Measurement Reference Level: 1.5V

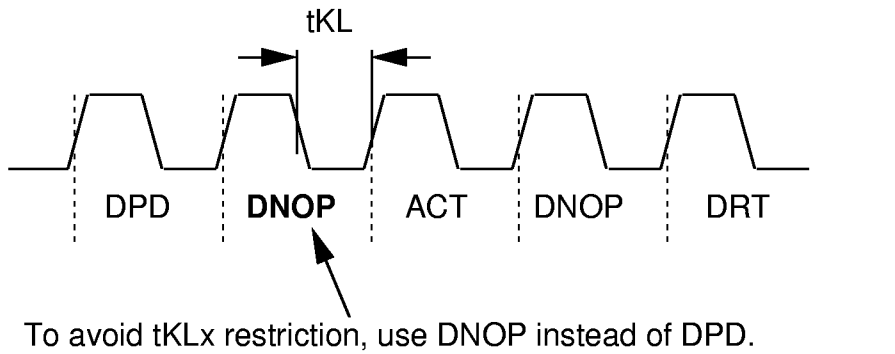
Input Rise/Fall Time: 2ns

Symbol	Parameter	Limits						Unit
		-10		-12		-15		
		Min.	Max	Min.	Max	Min.	Max	
tK	Clock Cycle Time	10		12		15		ns
tKH	Clock High Pulse Width	4		4		4		ns
tKL*	Clock Low Pulse Width	4		4		4		ns
tCMDS	Setup Time for CMd#	4		4		4		ns
tCMDH**	Hold Time for CMd#	1		1		1		ns
tRS	Setup Time for RAS#	4		4		4		ns
tRH**	Hold Time for RAS#	1		1		1		ns
tCS	Setup Time for CAS#	4		4		4		ns
tCH**	Hold Time for CAS#	1		1		1		ns
tDTS	Setup Time for DTD#	4		4		4		ns
tDTH**	Hold Time for DTD#	1		1		1		ns
tCMSS	Setup Time for CMs#	4		4		4		ns
tCMSH**	Hold Time for CMs#	1		1		1		ns
tWS	Setup Time for WE#	4		4		4		ns
tWH**	Hold Time for WE#	1		1		1		ns
tC0S	Setup Time for CC0#	4		4		4		ns
tC0H**	Hold Time for CC0#	1		1		1		ns
tC1S	Setup Time for CC1#	4		4		4		ns
tC1H**	Hold Time for CC1#	1		1		1		ns
tAS	Setup Time for Address	4		4		4		ns
tAH**	Hold Time for Address	1		1		1		ns
tDS	Setup Time for DIN	4		4		4		ns
tDH**	Hold Time for DIN	1		1		1		ns
tDQCS	Setup Time for DQC	4		4		4		ns
tDQCH**	Hold Time for DQC	1		1		1		ns
tCSS	Setup Time for CS#	4		4		4		ns
tCSH**	Hold Time for CS#	1		1		1		ns

*Note:Please refer to next page.
**Note:tH min. of 1.0ns is guaranteed at 3.0V to 3.45V. Otherwise 2.0ns. (3.0V to 3.6V)

*Note : tKLx between previous DPD and Acitive command(ACT,DRT,DWT,PCG ARF and SRF) is 7.0ns minimum, otherwise it is 4.0ns minimum. If this tKLx is less than tKLx minimum, the next active command will result in NOP(no operation).





TIMING REQUIREMENTS (Read, Write, Refresh)

(Ta=0~70°C, Vdd=3.3±0.3V for -12 and -15, Vdd=3.3V±0.15V for -10
Vss=0V, unless otherwise noted)

Input Pulse Levels: 0 to 3.0V
Input Timing Measurement Reference Level: 1.5V
Input Rise/Fall Time: 2ns

Symbol	Parameter	Limits						Unit
		-10		-12		-15		
		Min.	Max	Min.	Max	Min.	Max	
tREF	Refresh Cycle Time		64		64		64	ms
tRP	Precharge Time	30		36		40		ns
tRCD	Delay Time, Add Strb. Row to Col.	24		24		30		ns
tRC*	DRAM Activate-Read Cycle Time	80		96		120		ns
tWC*	DRAM Activate-Write Cycle Time	80		96		120		ns
tPC	Page Cycle Time	20		24		30		ns
tRAS	Activate Time	50	10,000	60	10,000	70	10,000	ns
tRASP	Page mode Activate Time	50	100,000	60	100,000	70	100,000	ns
tRWL	Write to Precharge Lead Time	15		15		15		ns
tRSH	Read to Precharge Hold Time	10		12		15		ns

*Note: When tRP and tRAS = Min. values, tRC and tWC = tRP + tRAS.

TIMING PARAMETER-CLK TABLE

Version	-10				-12				-15			
Freq. (MHz)	100.0		50.0		83.3		41.7		66.6		33.3	
	Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max
tREF		6.40M		3.20M		5.33M		2.67M		4.27M		2.13M
tRP	3		2		3		2		3		2	
tRCD	3		2		2		1		2		1	
tRC	8		5		8		5		8		4	
tWC	8		5		8		5		8		4	
tPC	2		1		2		1		2		1	
tRAS	5	1000	3	500	5	833	3	417	5	667	3	333
tRASP	5	10000	3	5000	5	8333	3	4167	5	6667	3	3333
tRWL	2		1		2		1		1		1	
tRSH	1		1		1		1		1		1	

Note: Value of K can be determined by integer≥(timing parameter/tCLK) for any clock frequency.

SWITCHING CHARACTERISTICS

(Ta=0~70°C, Vdd=3.3±0.3V for -12 and -15, Vdd=3.3V±0.15V for -10
Vss=0V, unless otherwise noted)

Symbol	Parameter	Limits						Unit
		-10		-12		-15		
		Min.	Max	Min.	Max	Min.	Max	
tCBF	Buffer-Fill from DRAM Read Transfer		20		20		20	ns
tKHA	Access Time from K-High Edge		10		11		12	ns
tKHQX	Output Active Time from K-High Edge	2		2		3		ns
tKHQZ	Output Disable Time from K-High Edge	2	8	2	8	3	8	ns
tKLA	Access Time from K-Low Edge		10		11		12	ns
tKLQX	Output Active Time from K-Low Edge	2		2		3		ns
tKLQZ	Output Disable Time from K-Low Edge	2	8	2	8	3	8	ns
tKHAR	Access Time from K-High Edge		7		7.5		8	ns
tKHQXR	Output Active Time from K-High Edge	2		2		3		ns
tKHQZR	Output Disable Time from K-High Edge	2	8	2	8	3	8	ns
tGLA	Access Time from G#-Low Edge		7		7.5		8	ns
tGLQ	Output Active Time from G#-Low Edge	2		2		3		ns
tGHQ	Output Disable Time from G#-High Edge	2	7	2	7	3	7	ns

ACCESS LATENCY (Minimum)

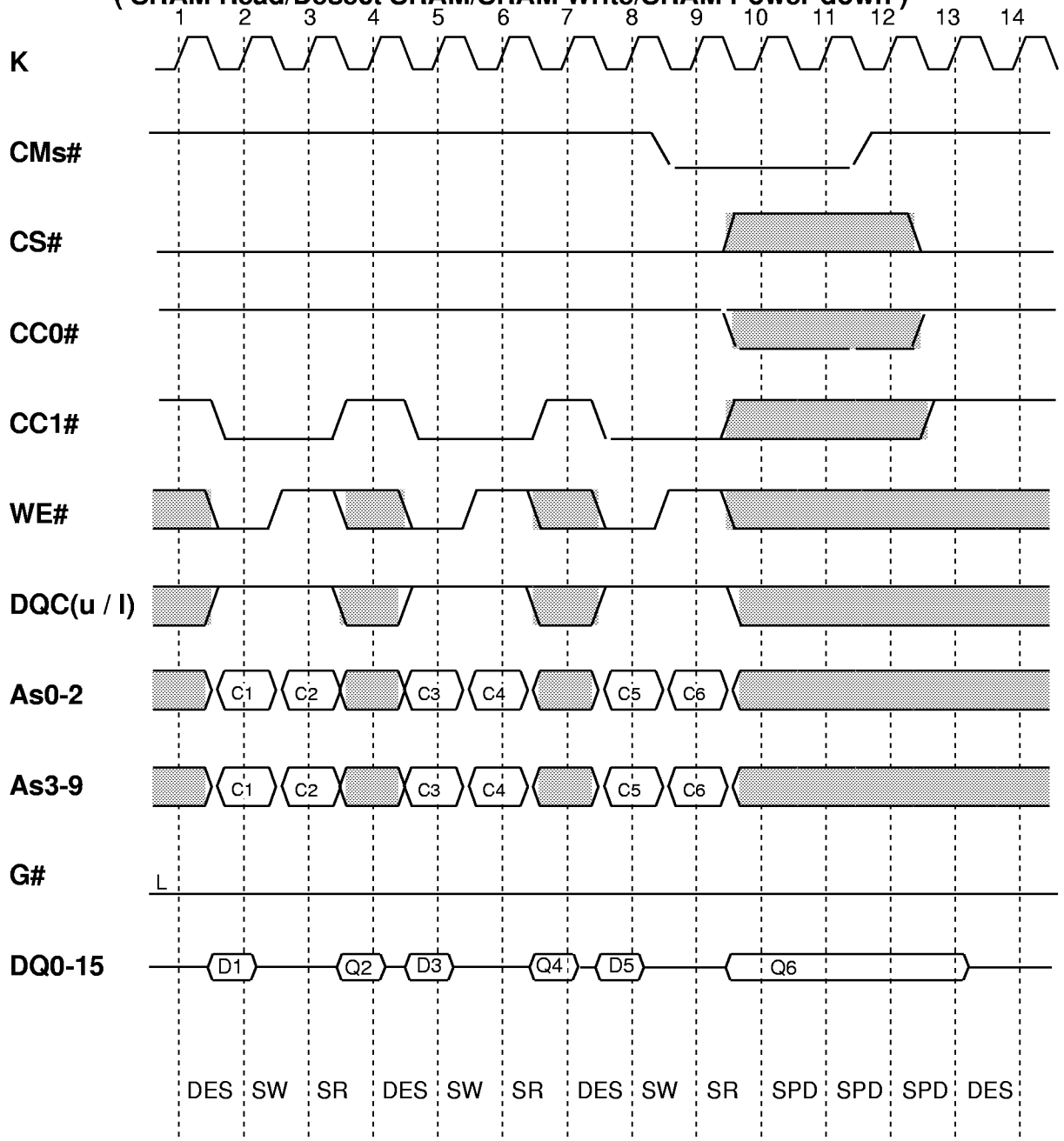
TIMING PARAMETER-CLK TABLE

Version	-10		-12		-15	
Freq. (MHz)	100.0	50.0	83.3	41.7	66.6	33.3
	Max	Max	Max	Max	Max	Max
tRAC*	6	4	5	3	5	3
tCAC**	3	2	3	2	3	2
tRCD	3	2	2	1	2	1
tCBF	2	1	2	1	2	1
tKHA	1	1	1	1	1	1
tKLA	1	1	1	1	1	1
tKHAR	1	1	1	1	1	1
tGLA	1	1	1	1	1	1

tRAC* =tRCD+tCBF+tKHA
tCAC**=tCBF+tKHA
Note: Value of K can be determined by integer≥(timing parameter/tCLK) for any clock frequency.

non-G# controlled Write & Read (DES control)

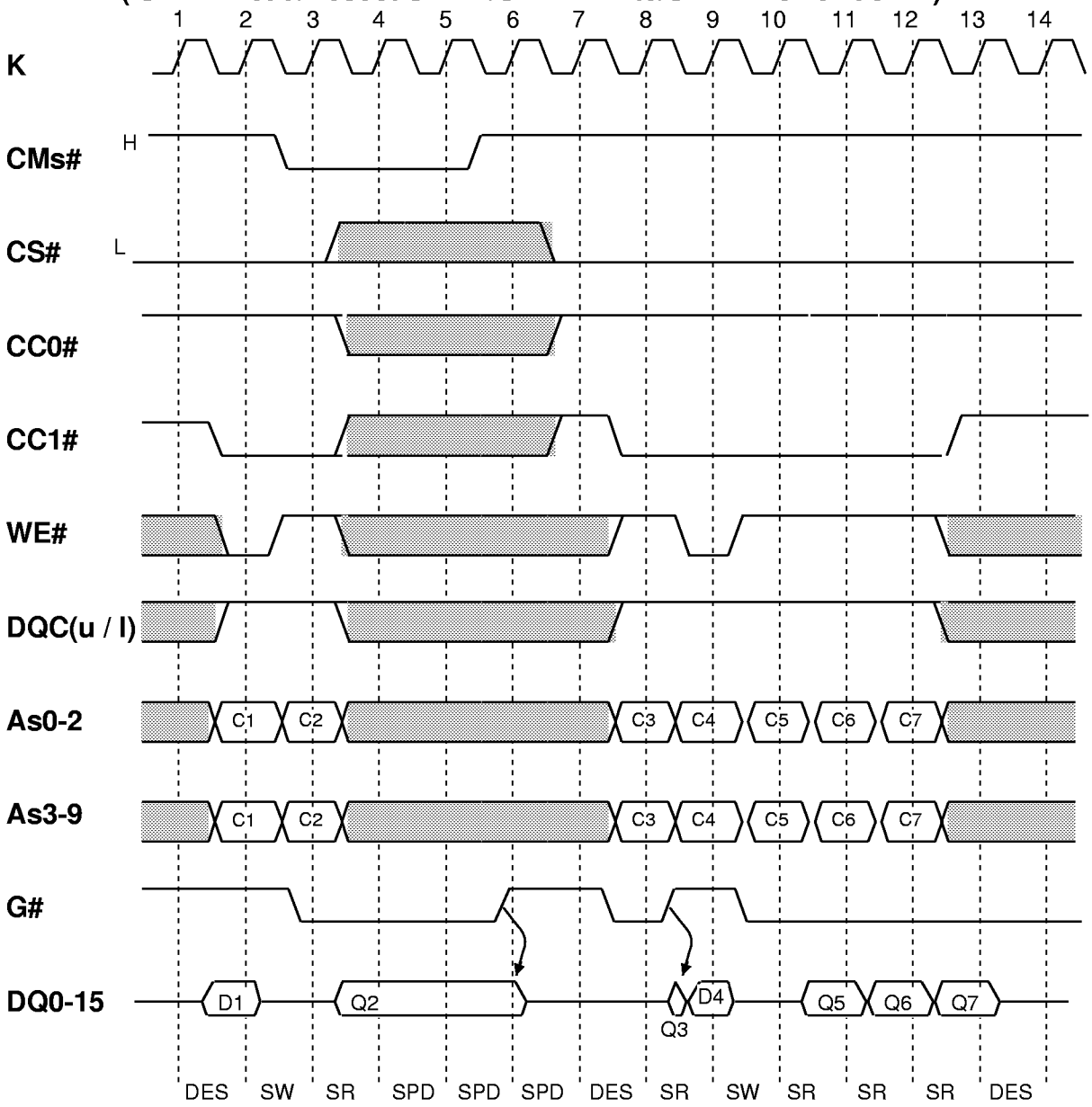
(SRAM Read/Desect SRAM/SRAM Write/SRAM Power-down)



Note : Output is transparent. DRAM operation can be freely performed.

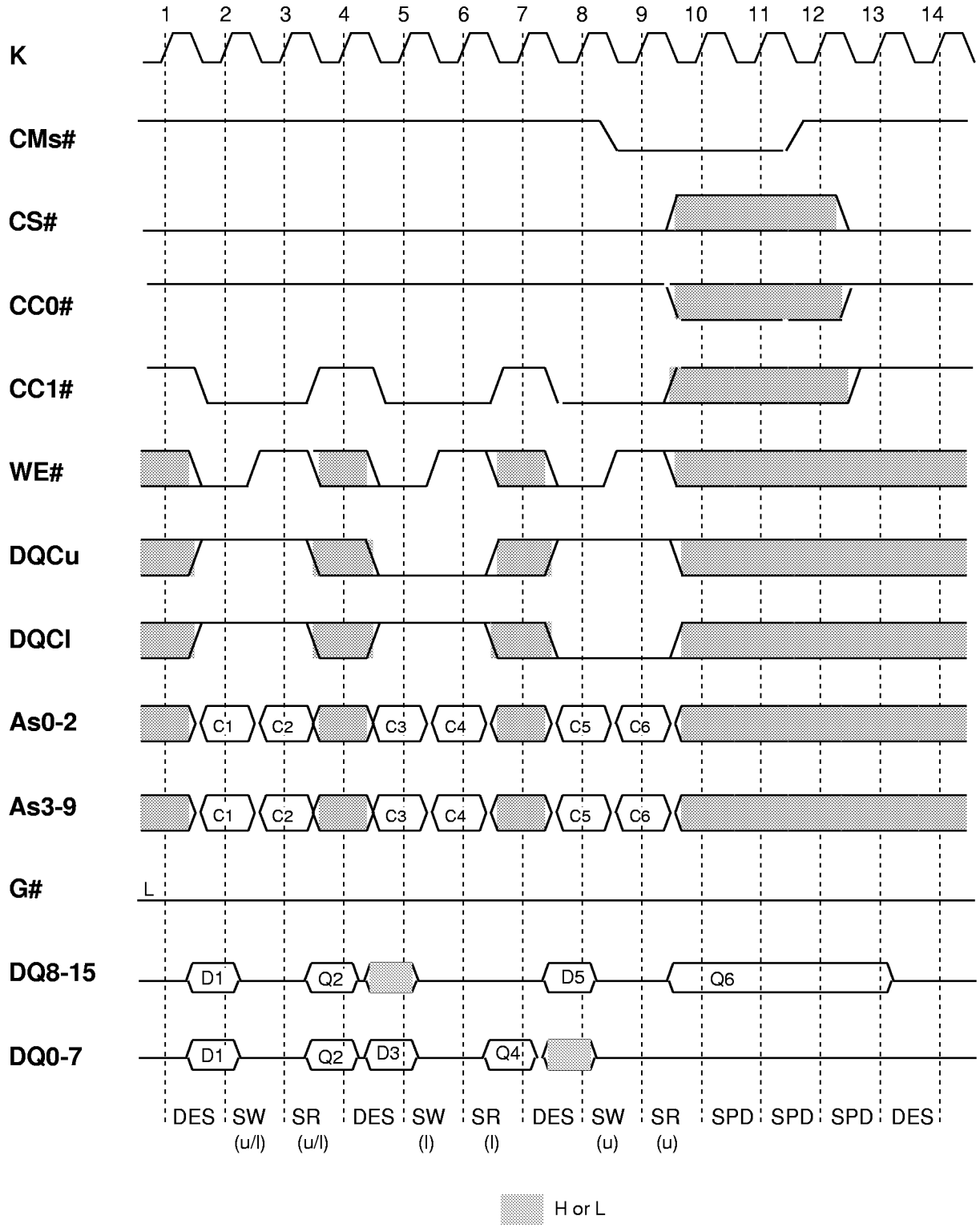
G# controlled Write & Read

(SRAM Read/Desect SRAM/SRAM Write/SRAM Power-down)



Note : Output is transparent. DRAM operation can be freely performed.

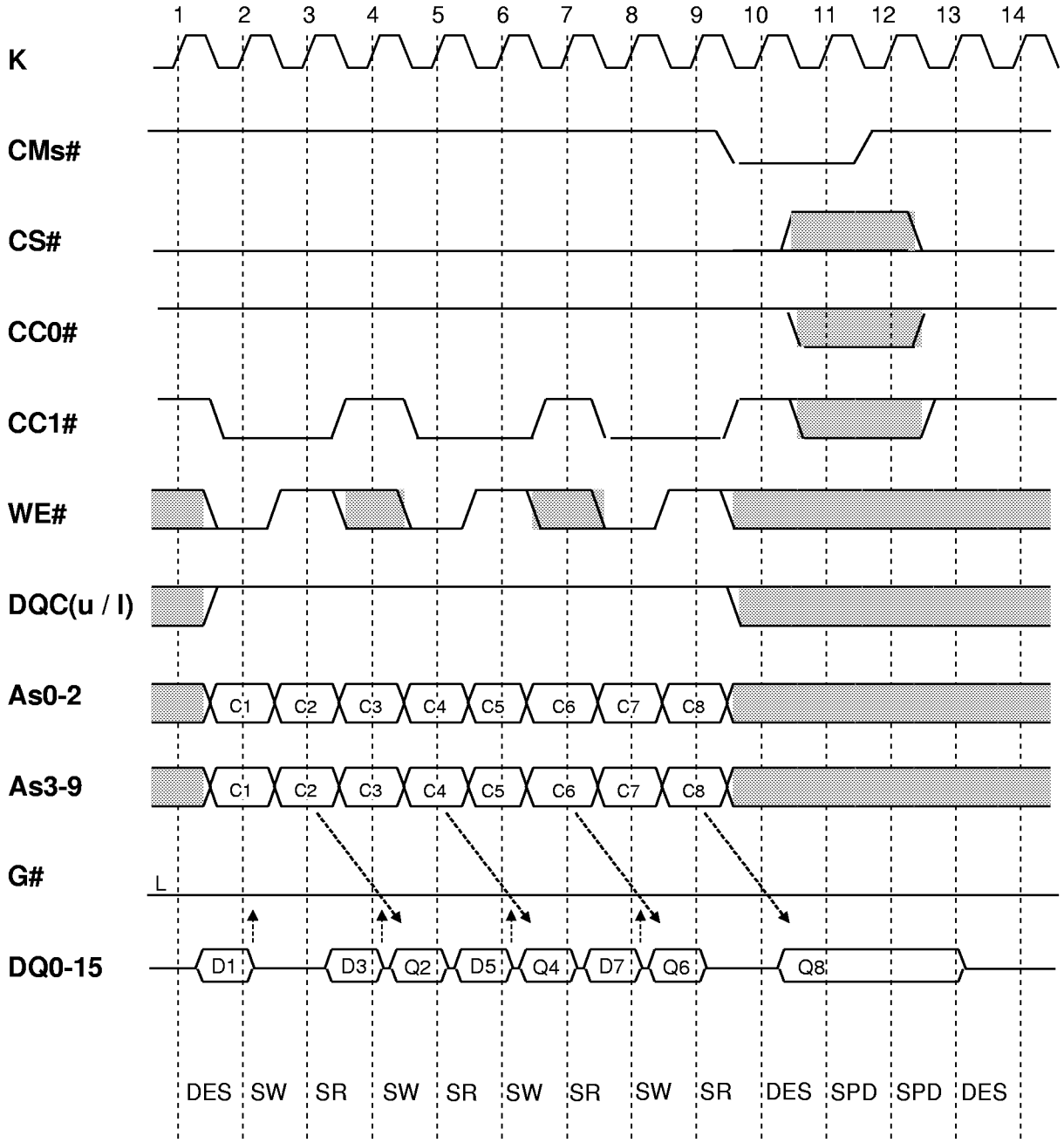
DQC controlled Write & Read
(SRAM Read/Desect SRAM/SRAM Write/SRAM Power-down)



Note : Output is transparent.

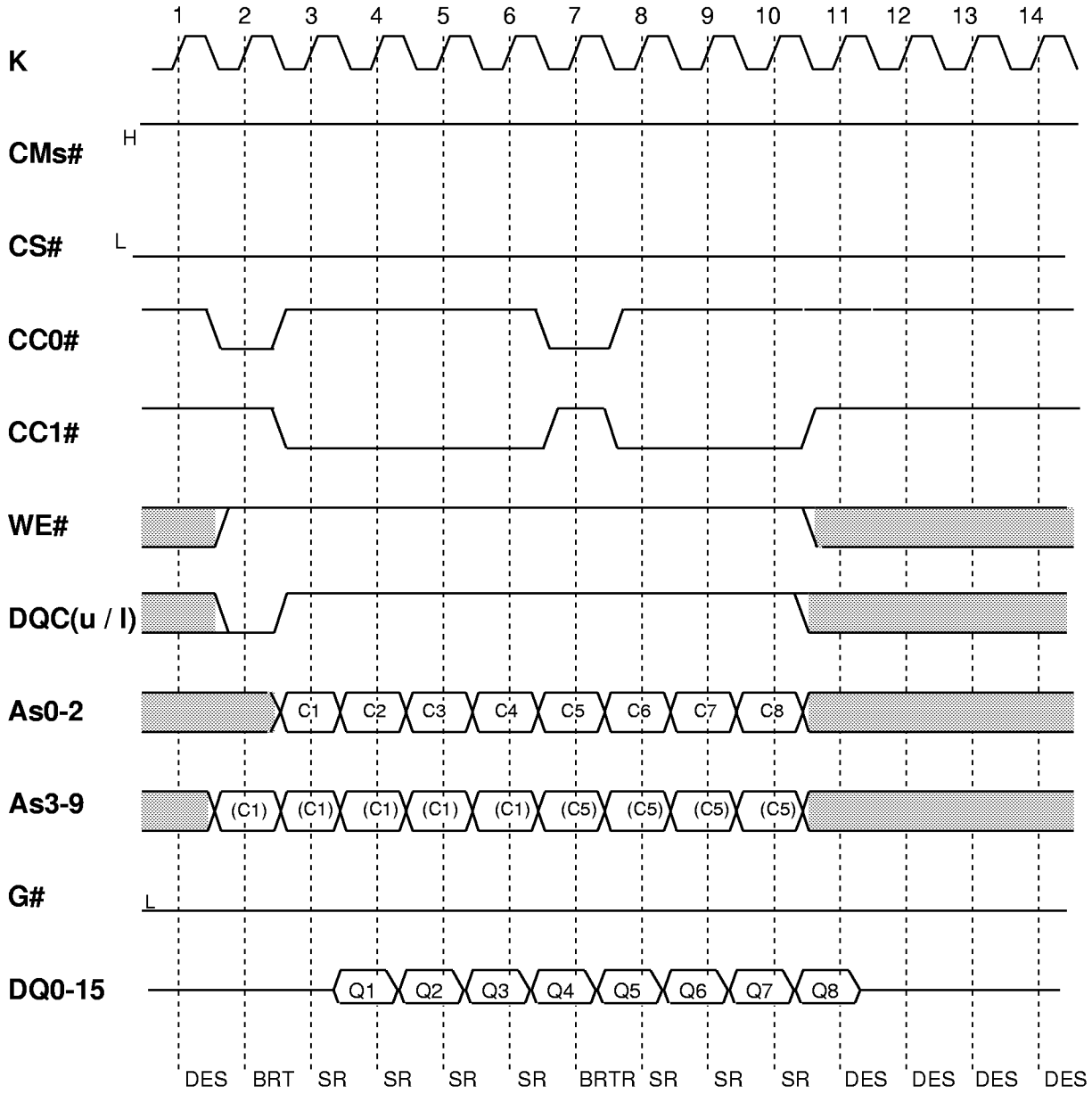
DRAM operation can be freely performed.

Registered Output control
(SRAM Read/Desect SRAM/SRAM Write/SRAM Power-down)



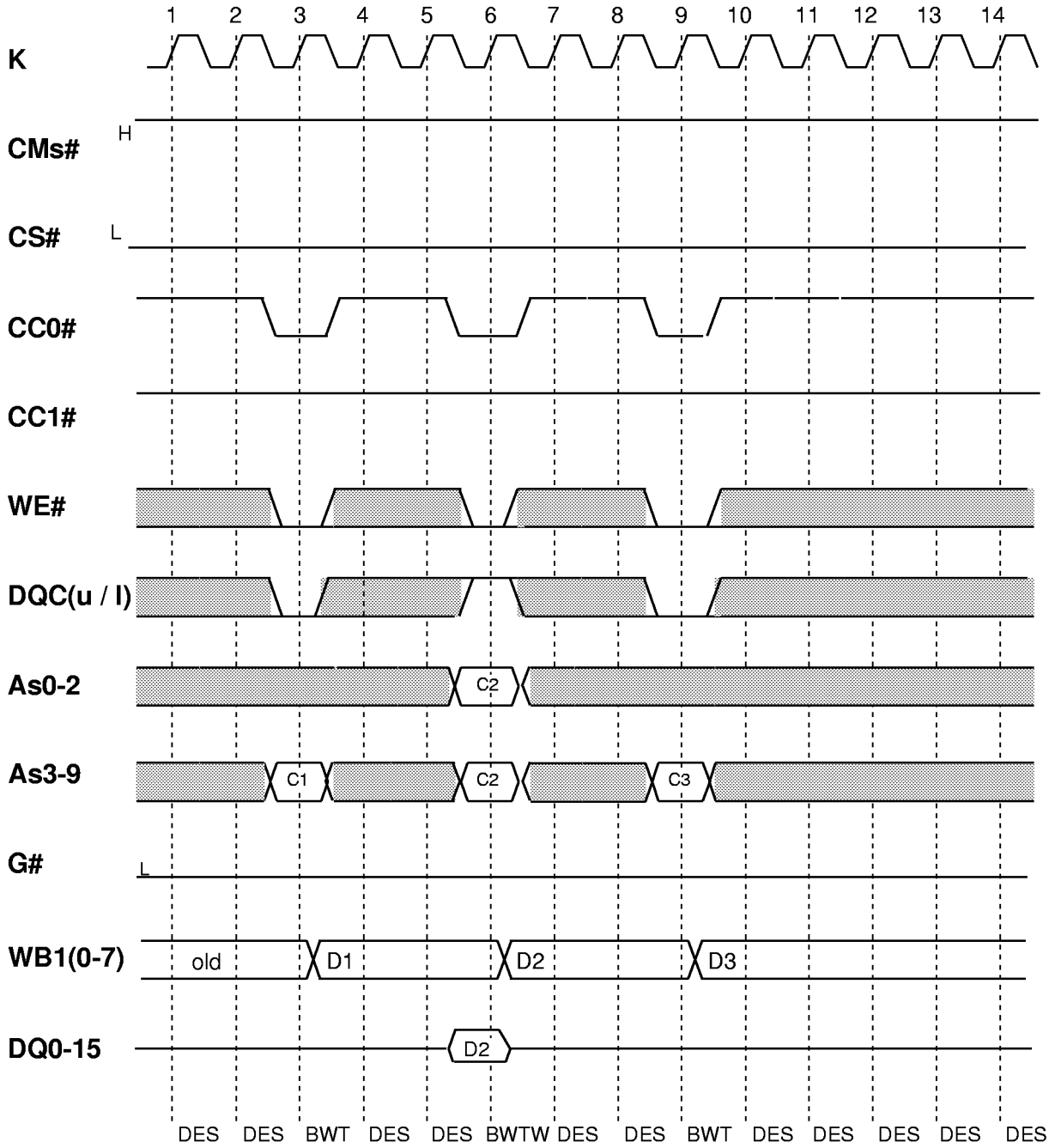
Note : Output is registered. DRAM operation can be freely performed.

Buffer Read Transfer (RB → SRAM)
Buffer Read Transfer & SRAM Read (RB → SRAM → Output)



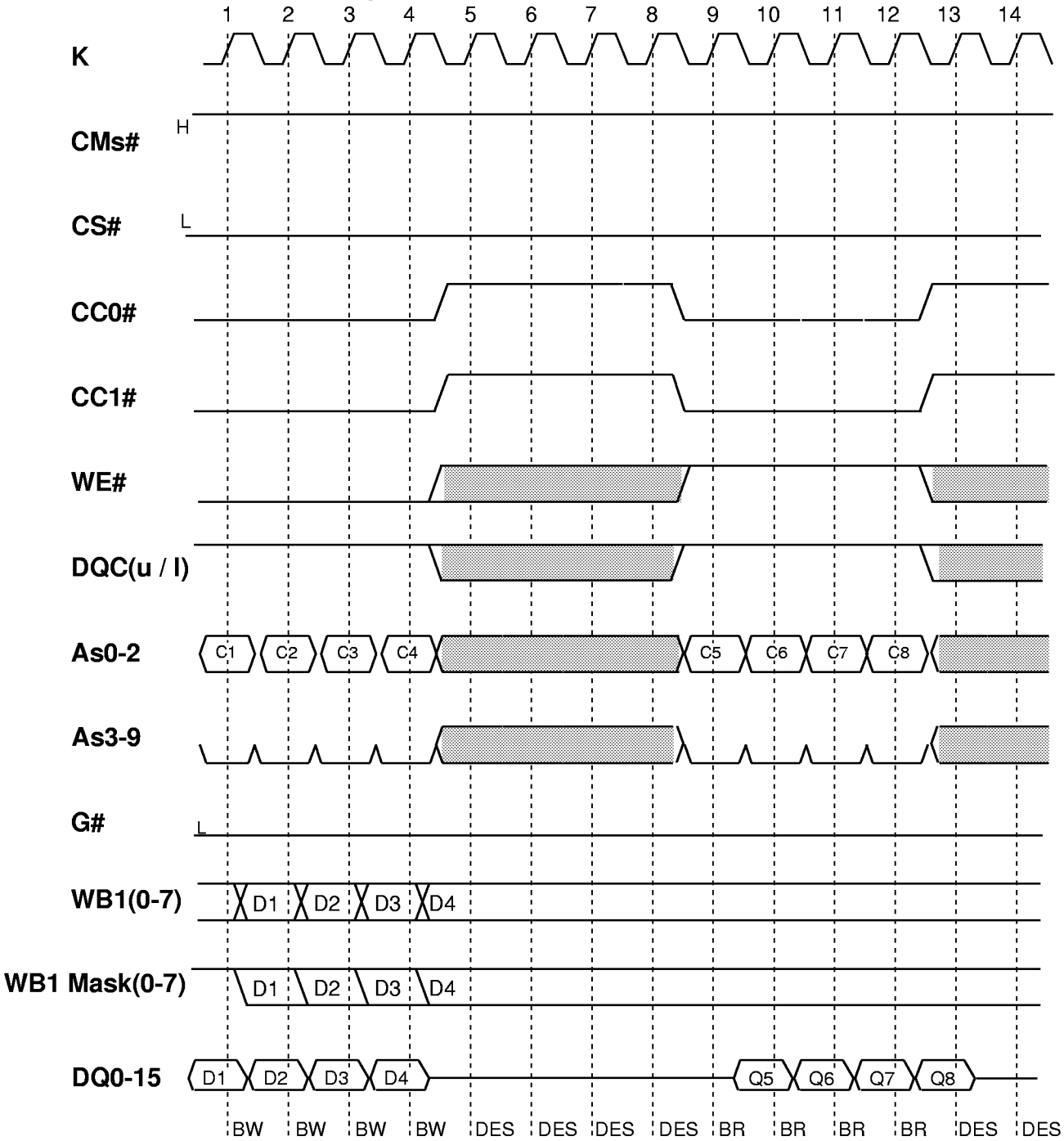
Note : Output is transparent. DRAM operation can be freely performed.

Buffer Write Transfer (SRAM→WB1)
Buffer Write Transfer & SRAM Write (Input→SRAM→WB1)



Note : Output is transparent. DRAM operation can be freely performed.

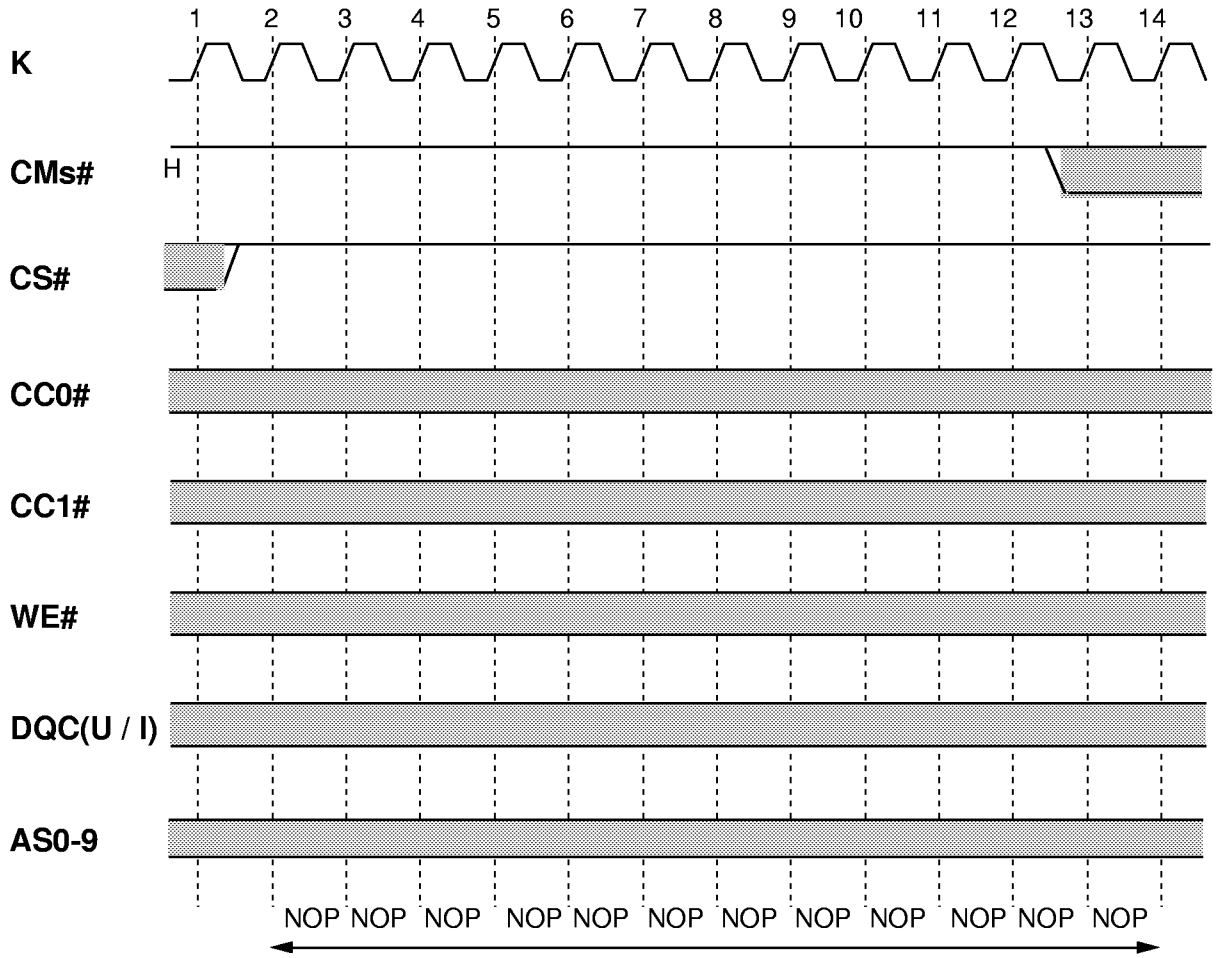
Buffer Write (Input →WB1)
Buffer Read (RB →Output)



Note : Output is transparent.

DRAM operation can be freely performed.

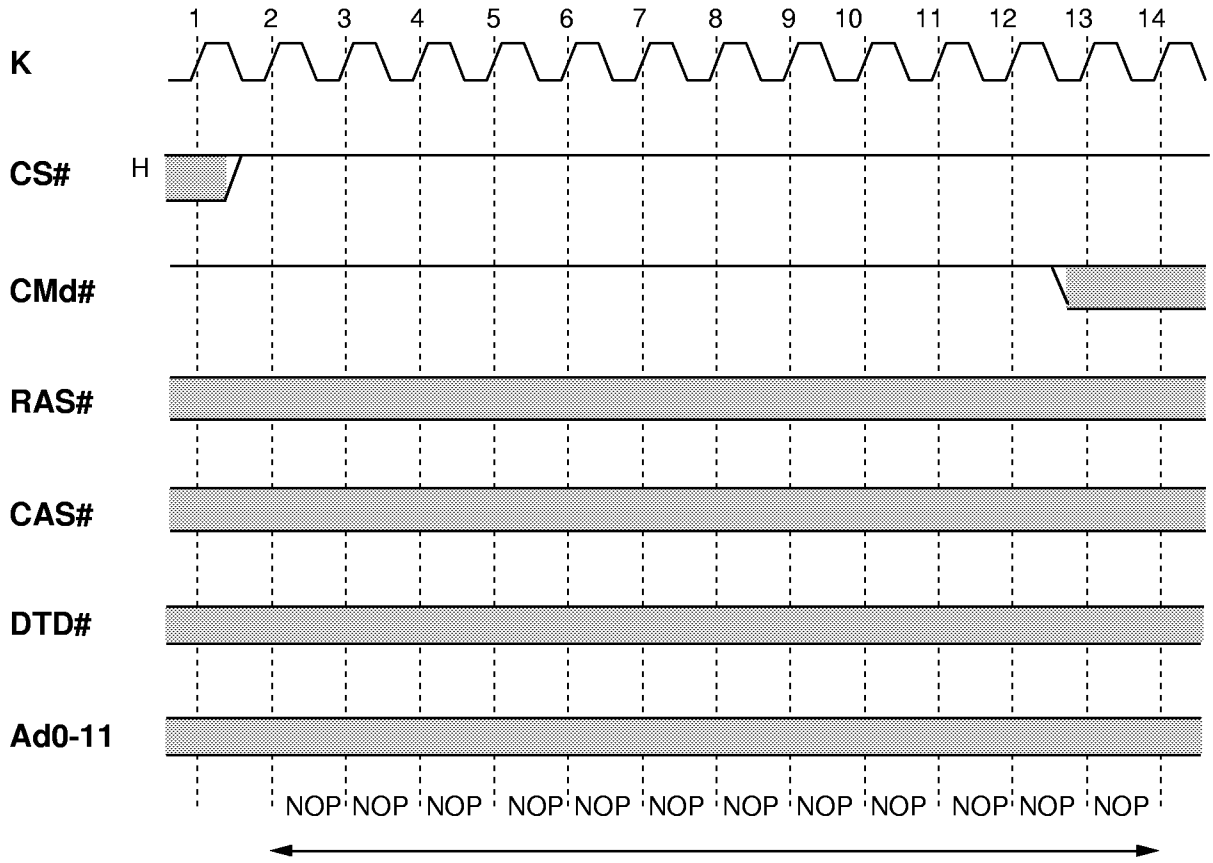
NO - Operation of SRAM



NO-Operation Mode

DPD operation can be freely performed.

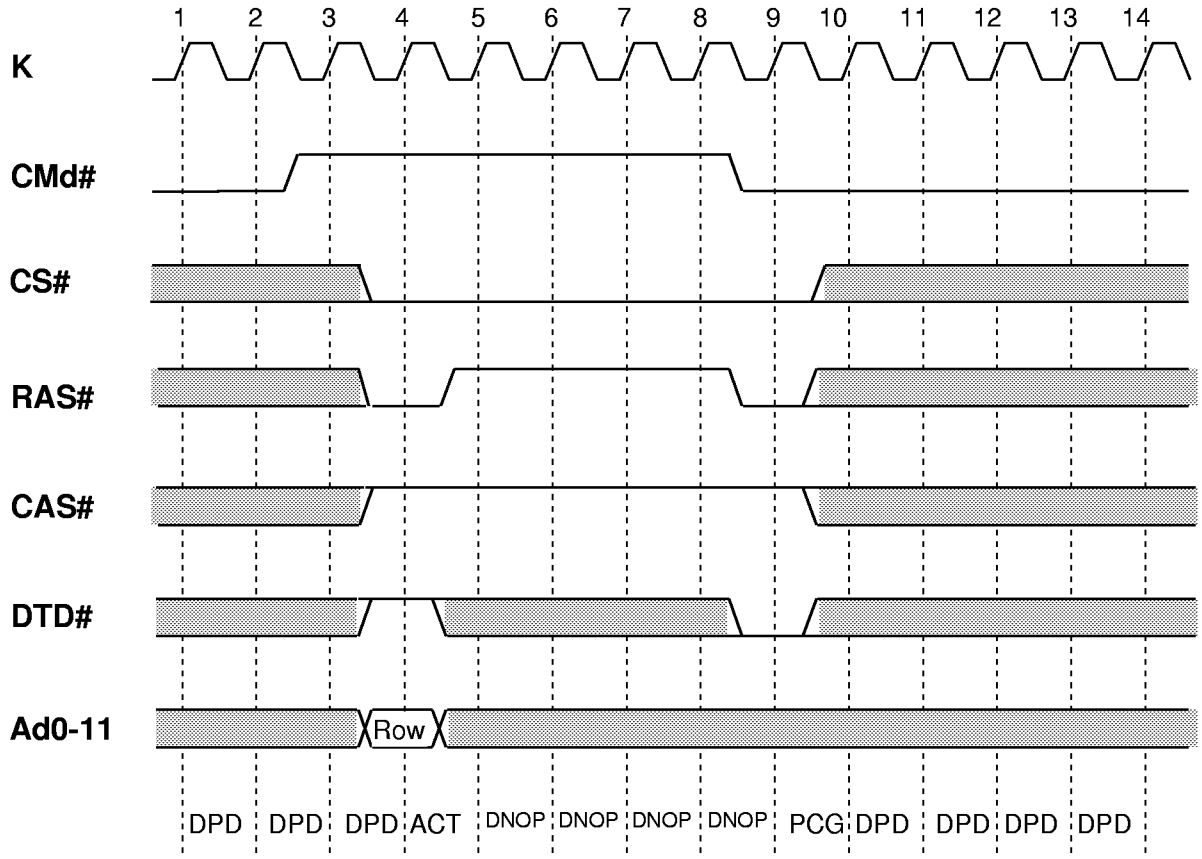
NO - Operation of DRAM



NO-Operation Mode

SPD operation can be freely performed.

DRAM Power Down / DRAM Activate / DRAM Precharge

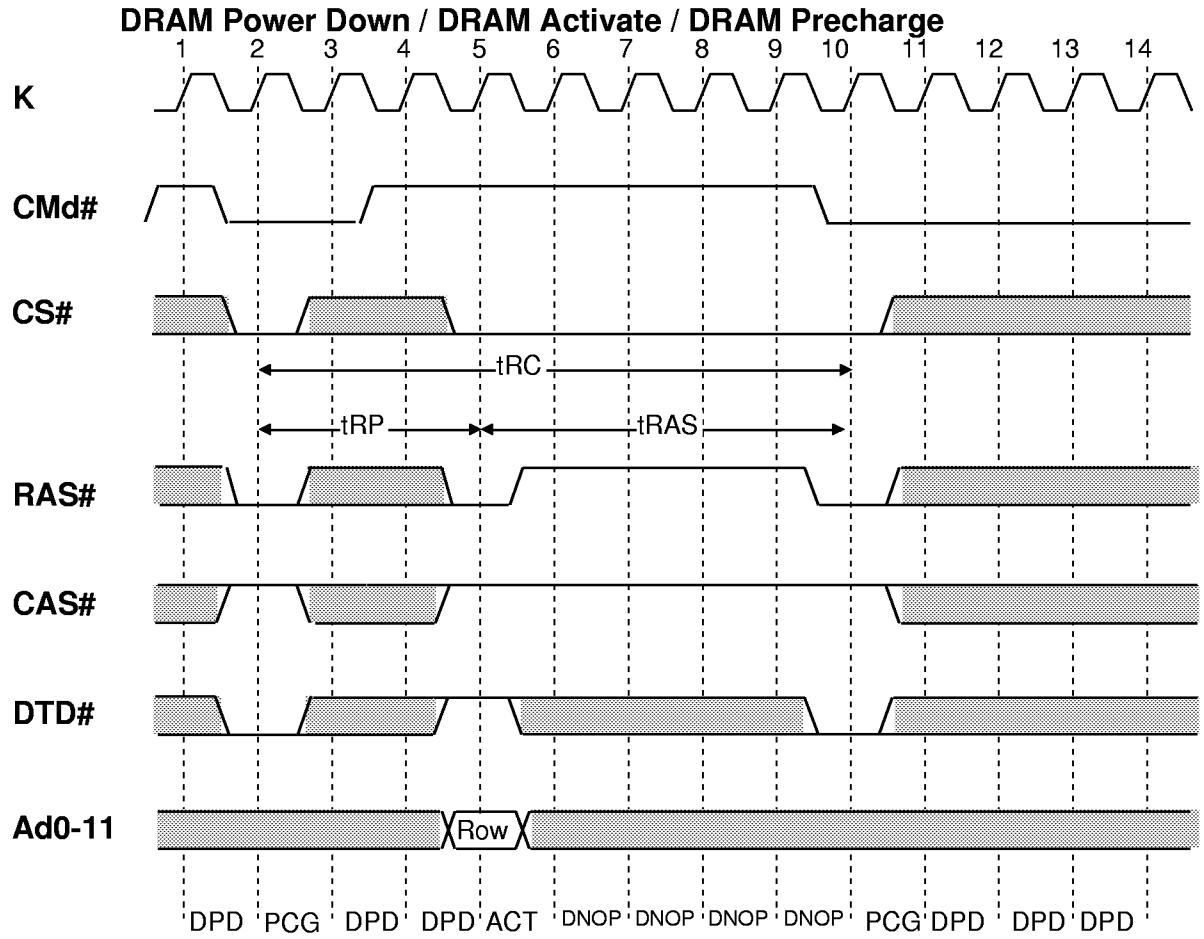


CMs#
CC0#
CC1#
WE#
DQC(u/l)
G#
As0-9
DQ0-15

SRAM operation can be freely performed.

DPD is recommended during no operation to save power.

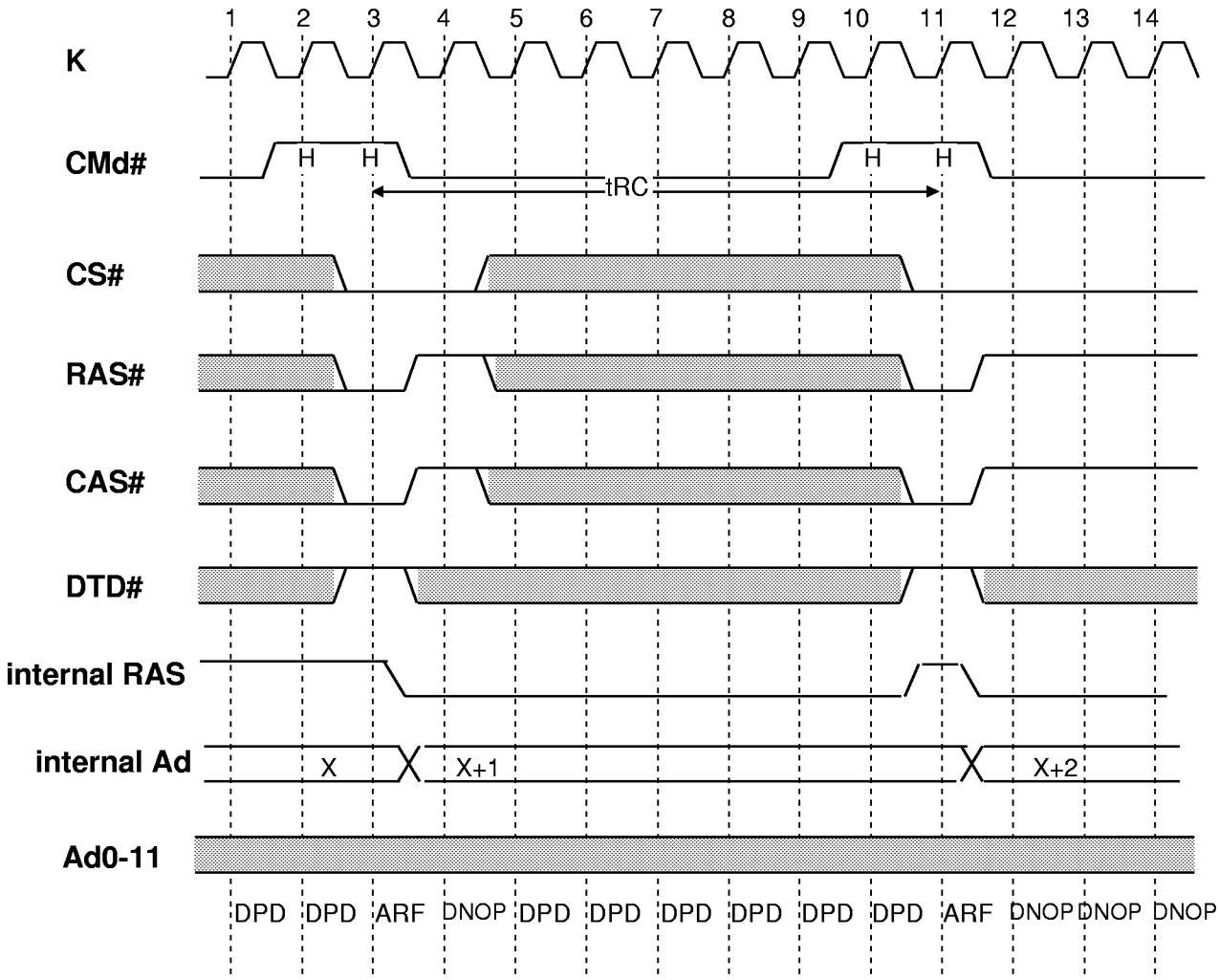
RAS only Refresh cycle



CMs#
CC0#
CC1#
WE#
DQC(u/l)
G#
As0-9
DQ0-15

SRAM operation can be freely performed.

DRAM Auto Refresh

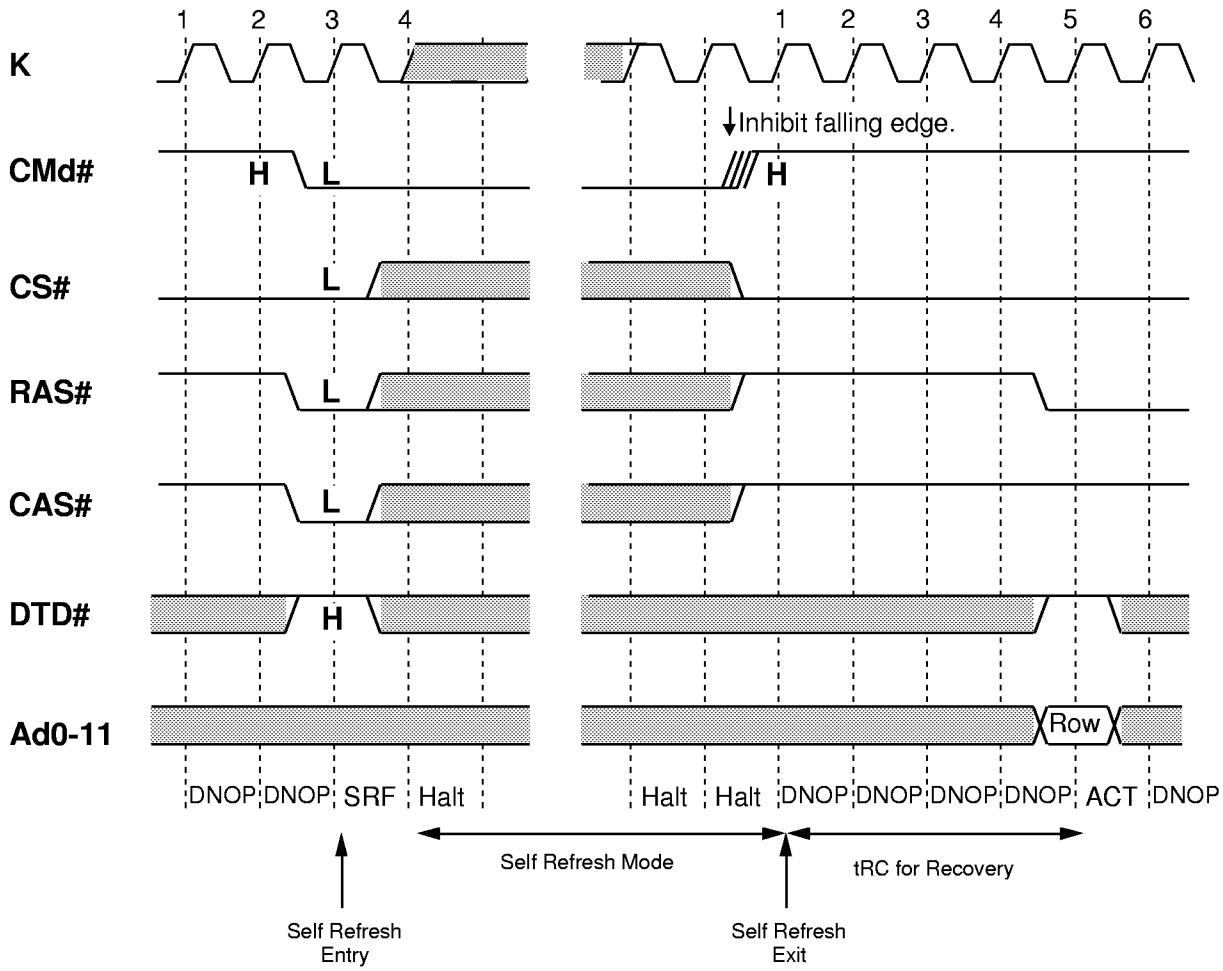


CMs#
CC0#
CC1#
WE#
DQC(u/l)
G#
As0-9
DQ0-15

Note: DRAM must be in Precharge state prior to Auto-Refresh cycle.
All DRAM commands except for NOP,DNOP and DPD can be set after tRC delay from the ARF command .

SRAM operation can be freely performed.

DRAM Self Refresh

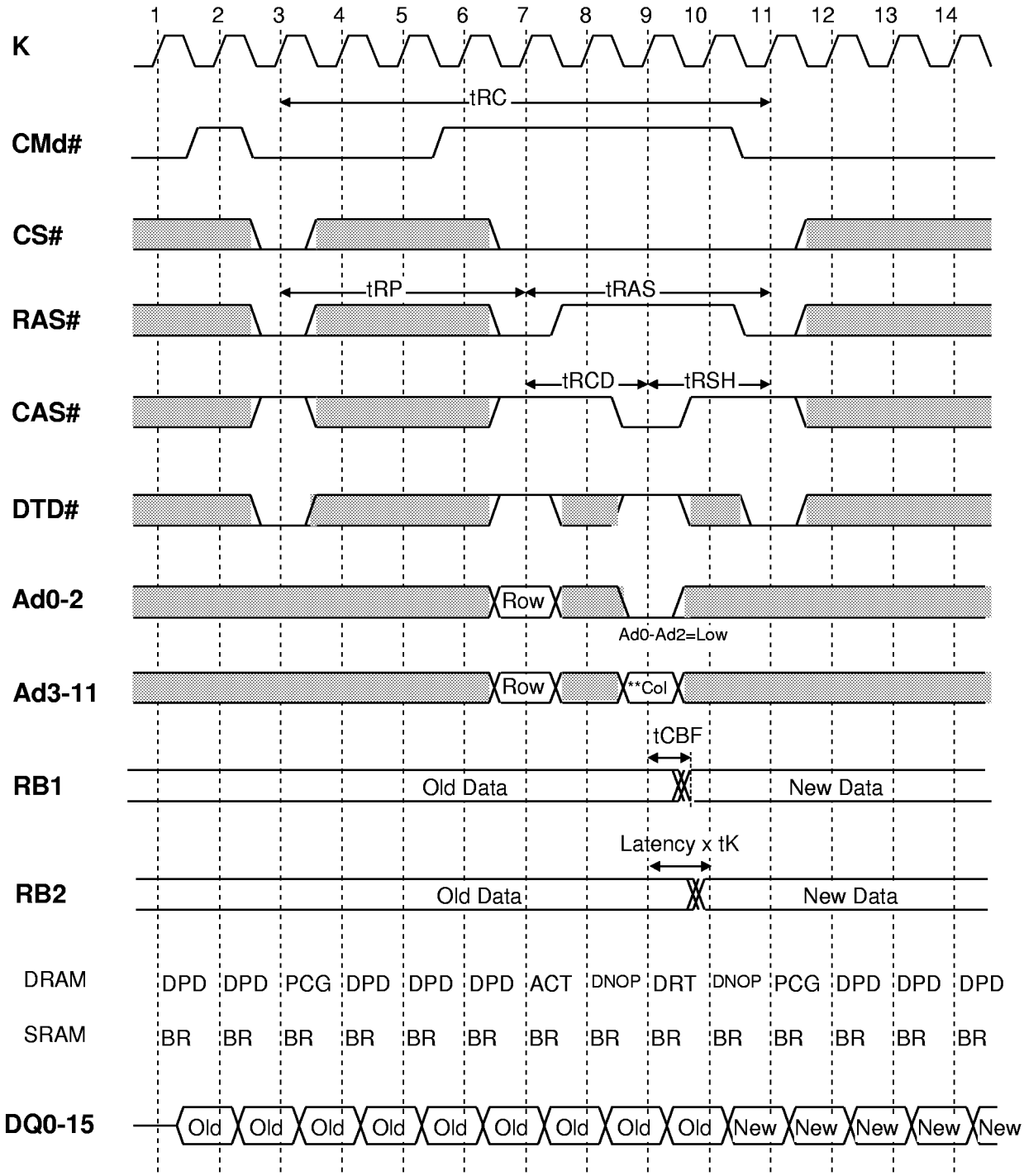


Self Refresh Entry: (Note: DRAM must be in Precharge state prior to Self-Refresh Entry)
Previous CMd#=H, Present CMd#=L, CS#=RAS#=CAS#=L, DTD#=H
(CMd# must remain low to maintain Self Refresh).

Self Refresh Exit (in order):
a) resume K clock
b) CMd#=H
c) Wait tRC for recovery
d) Resume normal operation

SRAM operation can be freely performed.

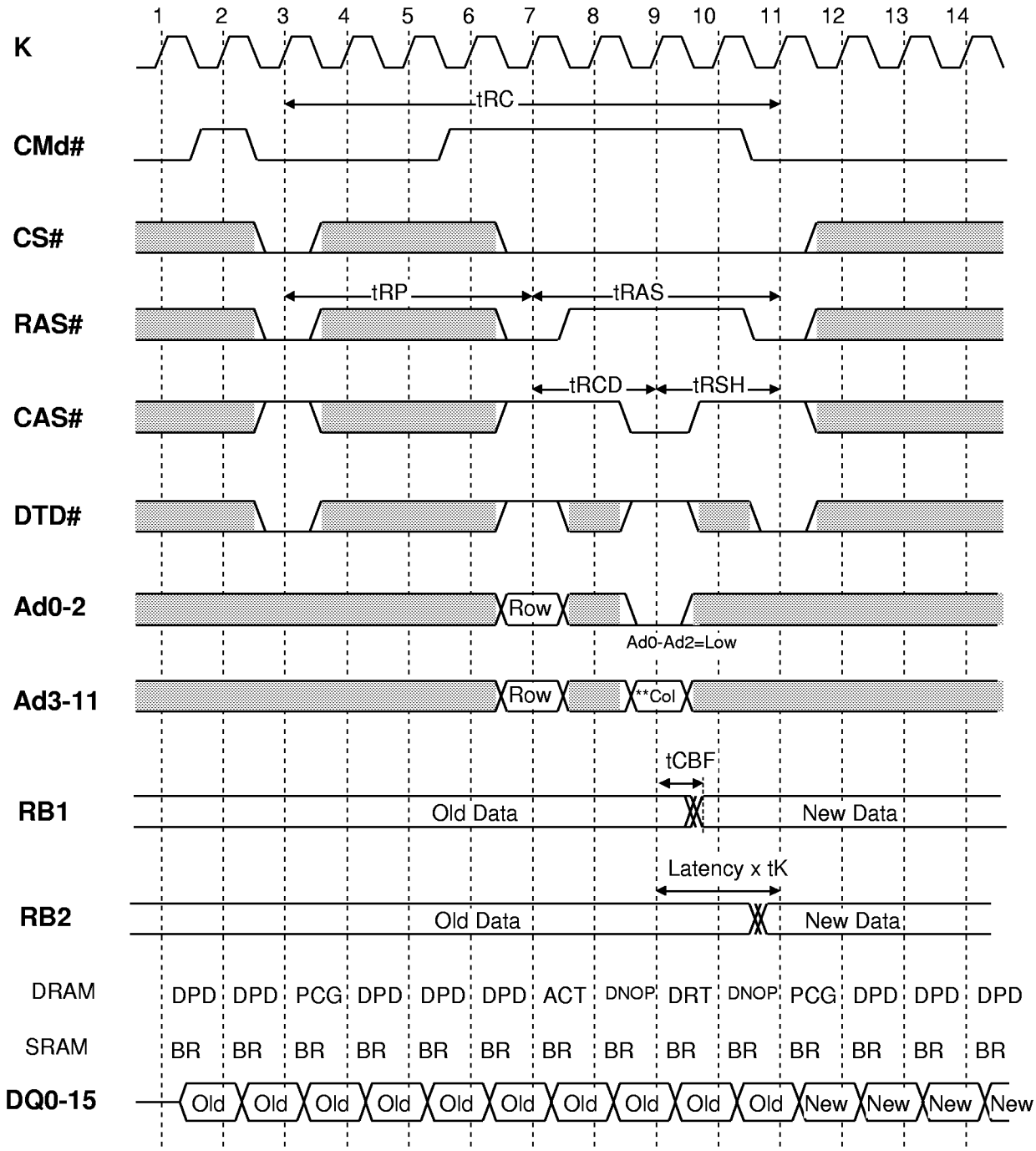
DRAM Read Transfer (DRAM -> RB) Latency set=1



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

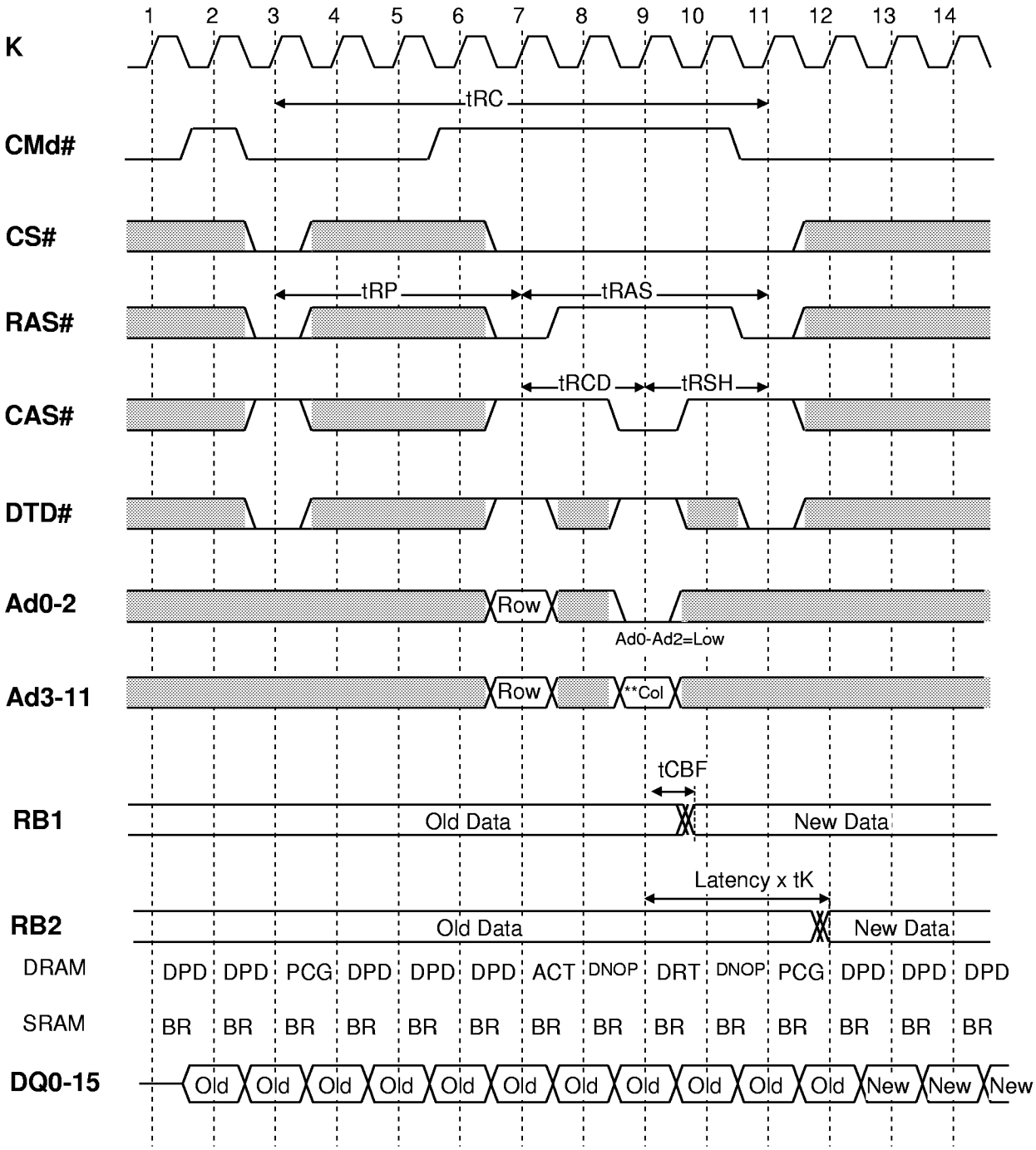
DRAM Read Transfer (DRAM -> RB) Latency set=2



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

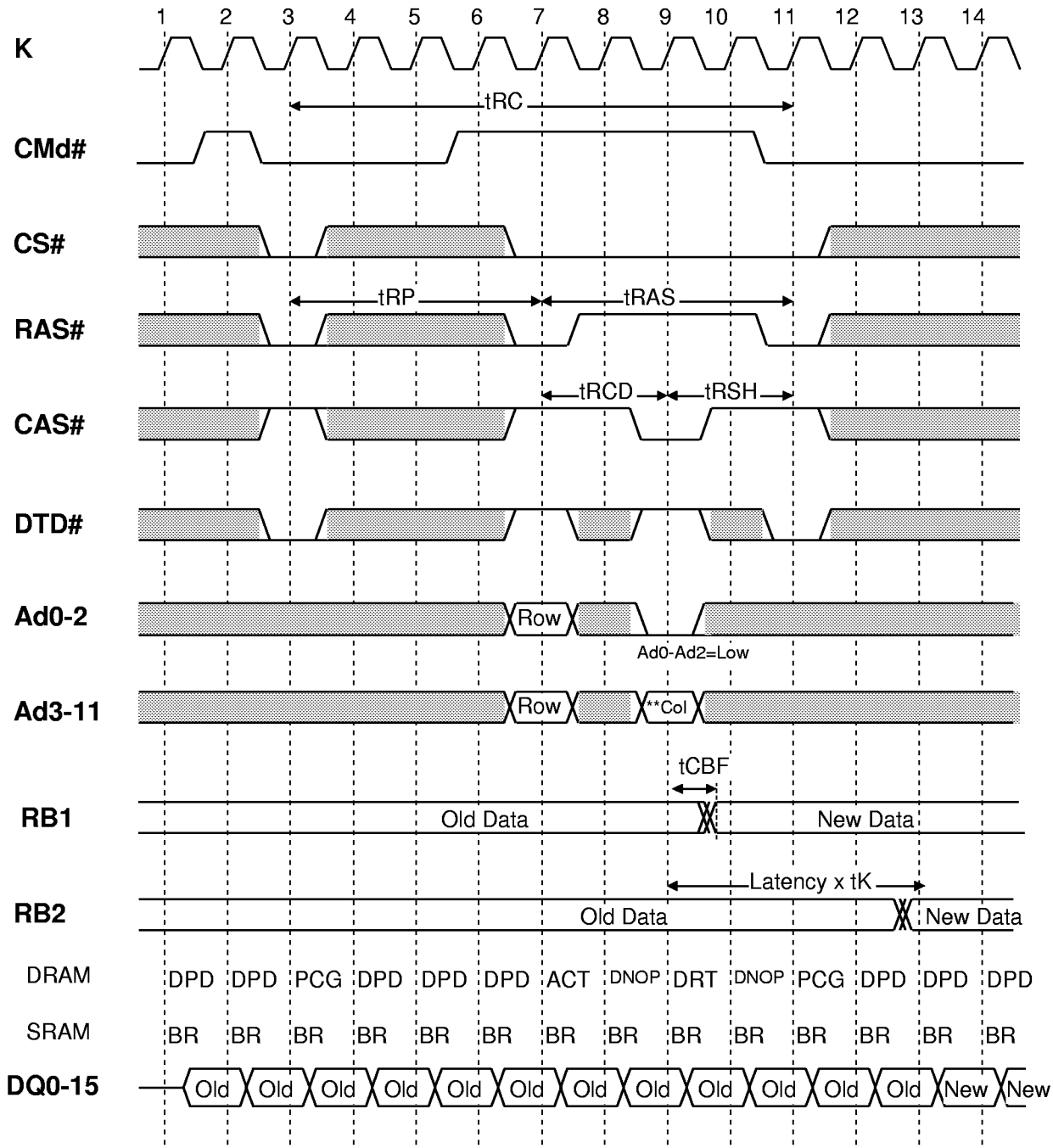
DRAM Read Transfer (DRAM -> RB) Latency set=3



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

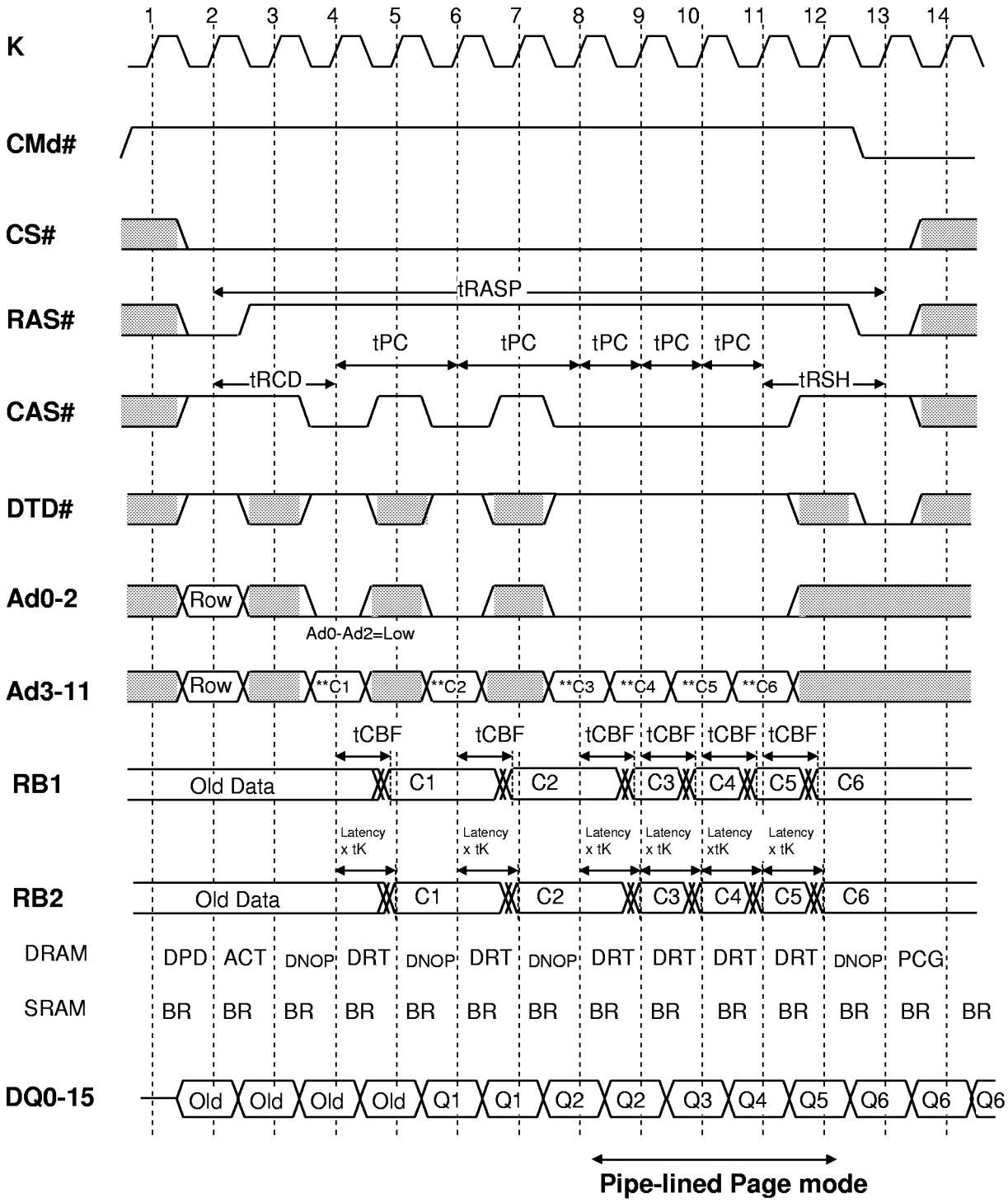
DRAM Read Transfer (DRAM -> RB) Latency set=4



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

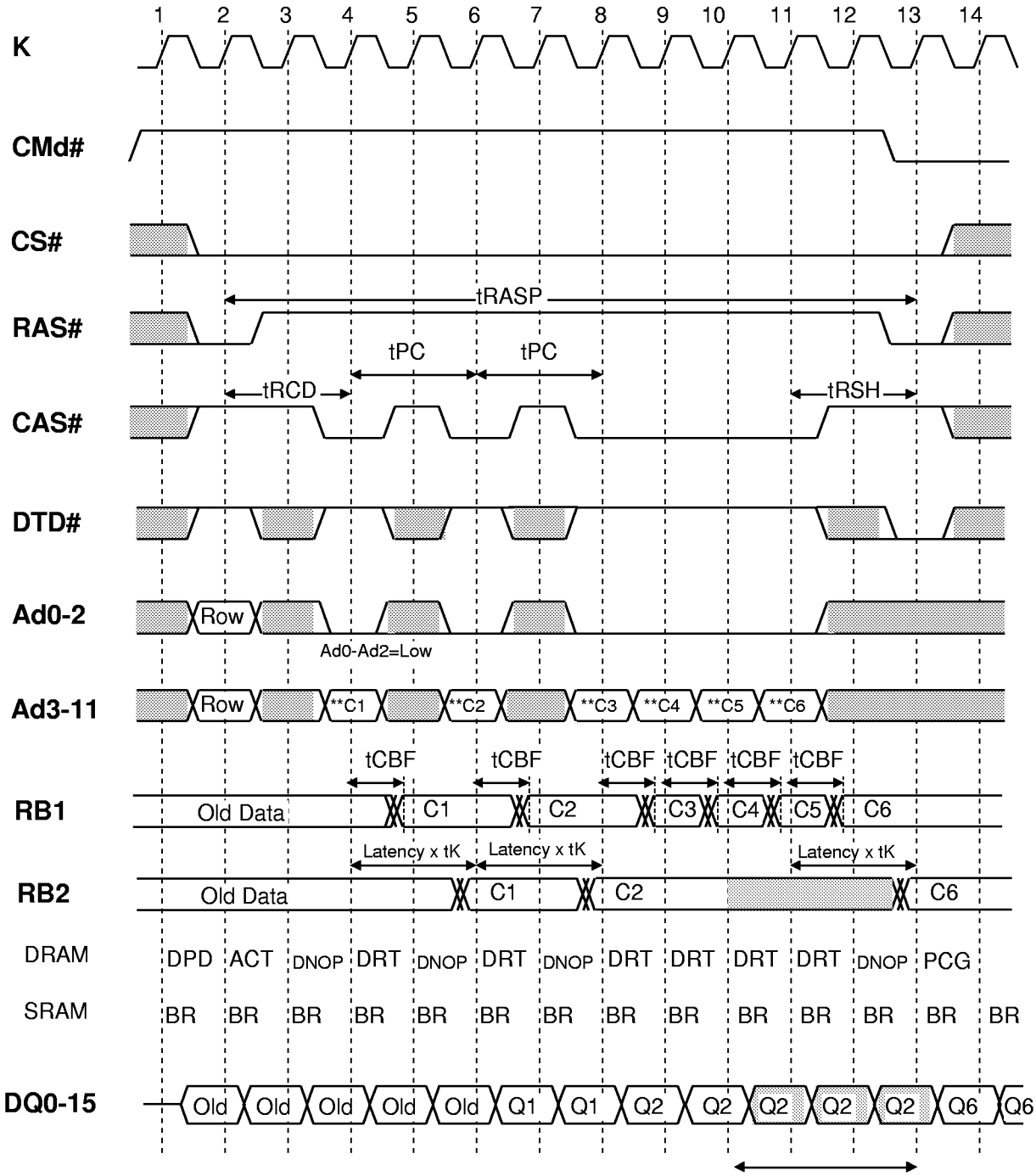
Page-Mode DRAM Read Transfer (Pipe-lined Page-Mode) Latency set=1



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

Page-Mode DRAM Read Transfer Latency set=2

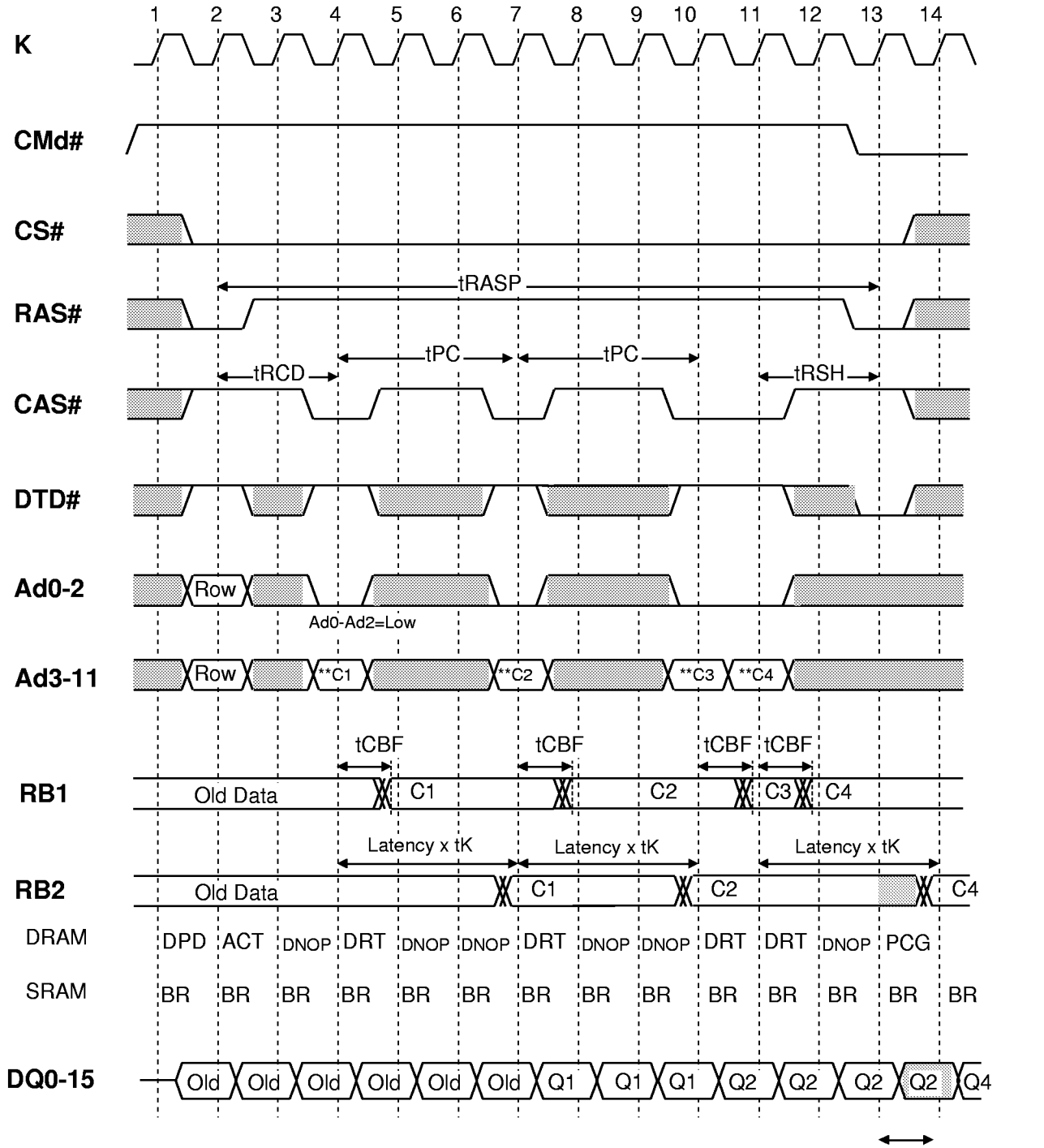


If next DRT happens within the latency, new data does not transferred to RB2. However this operation is not guaranteed.

SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

Page-Mode DRAM Read Transfer Latency set=3

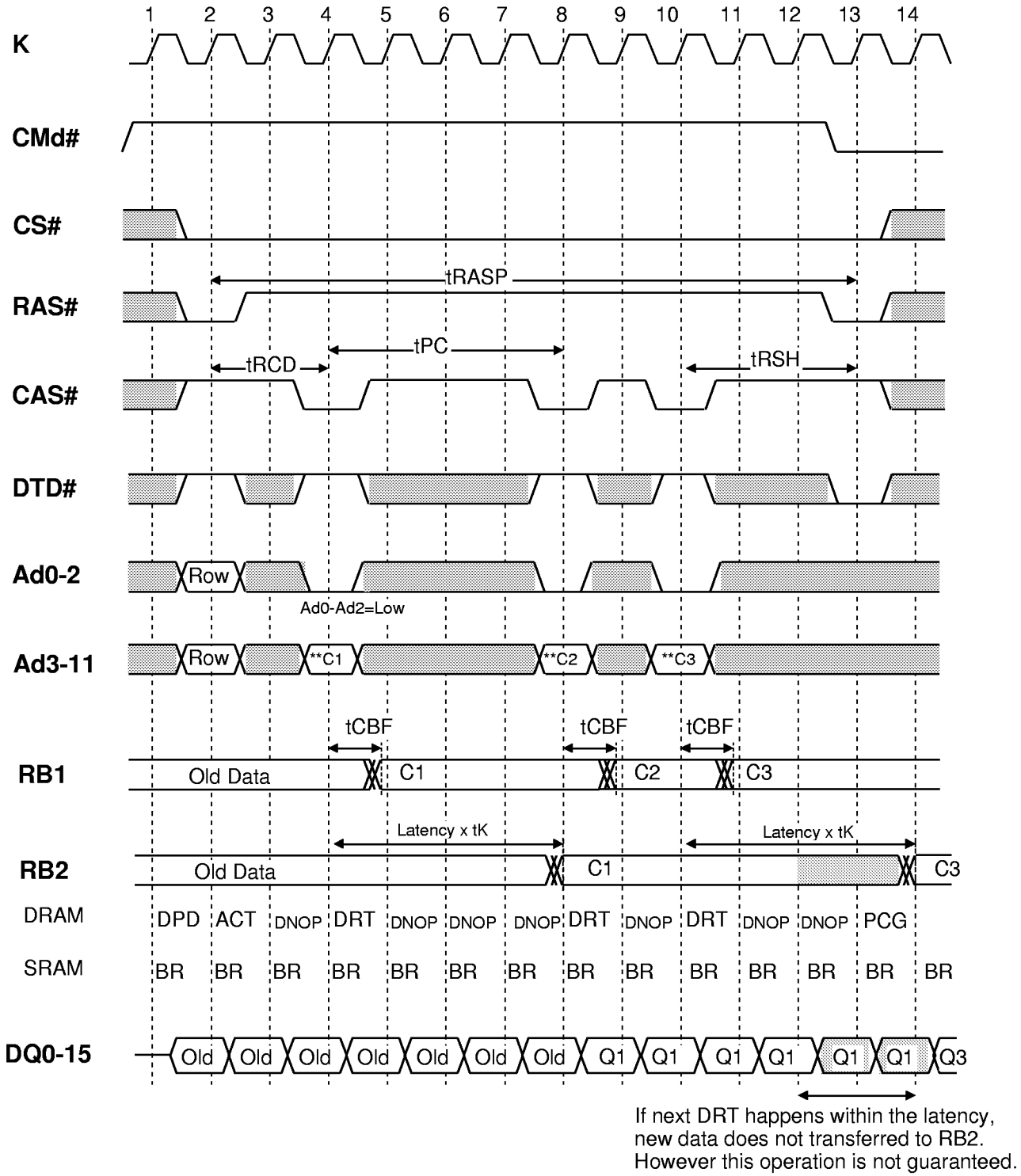


If next DRT happens within the latency, new data does not transferred to RB2. However this operation is not guaranteed.

SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

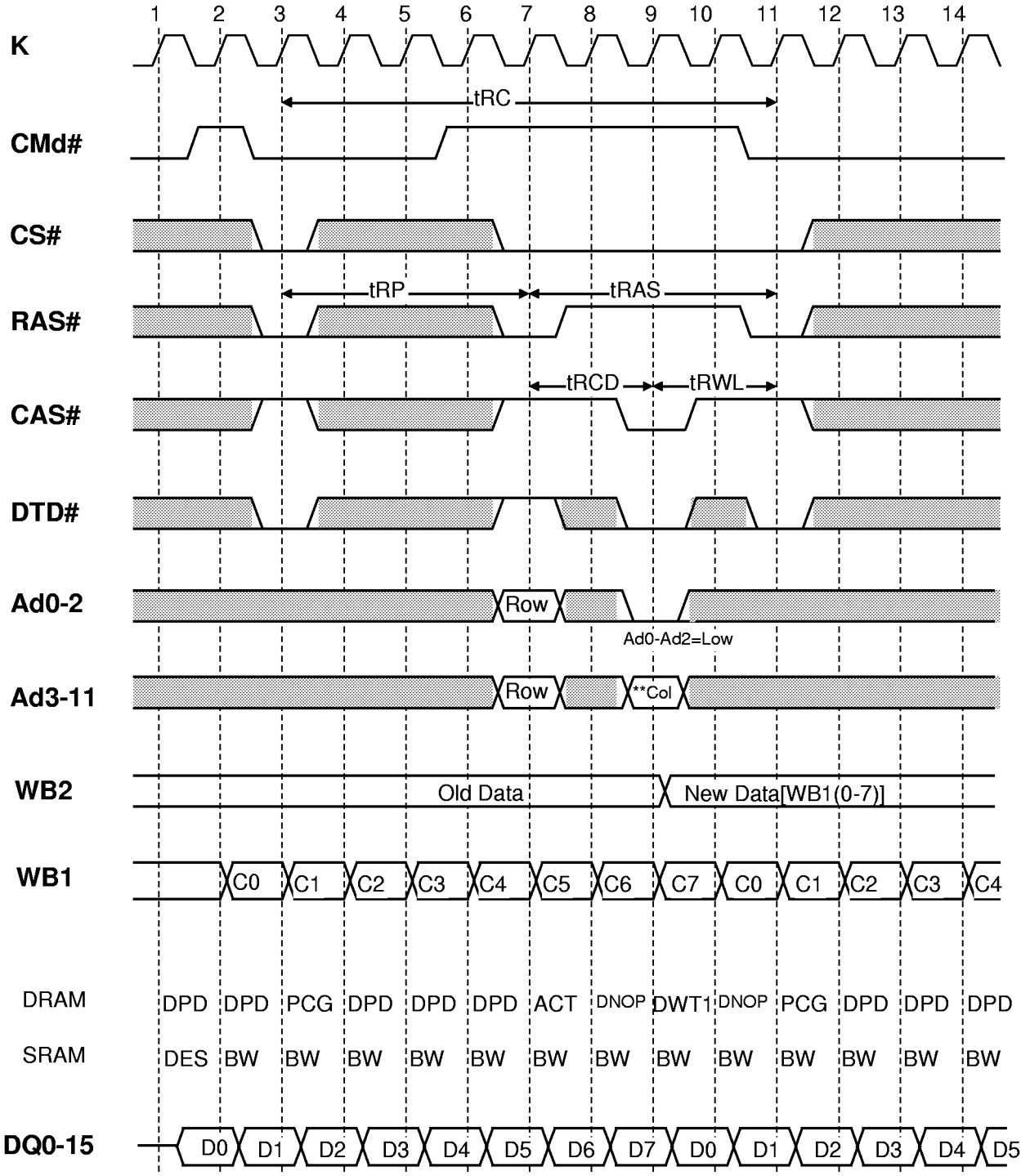
Page-Mode DRAM Read Transfer Latency set=4



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write (DIN->WB1)



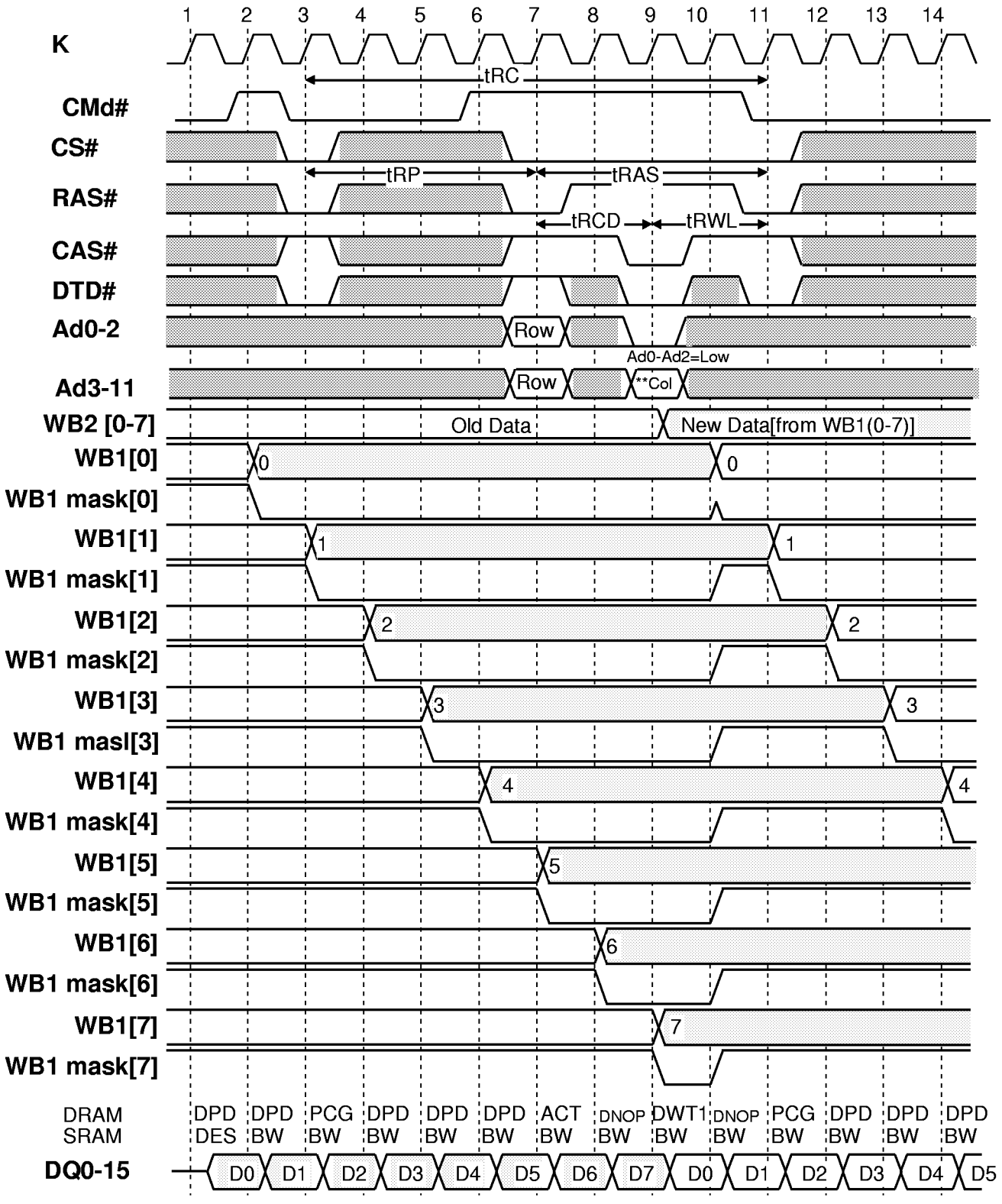
Please refer to next page in detail.

SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write (DIN->WB1)

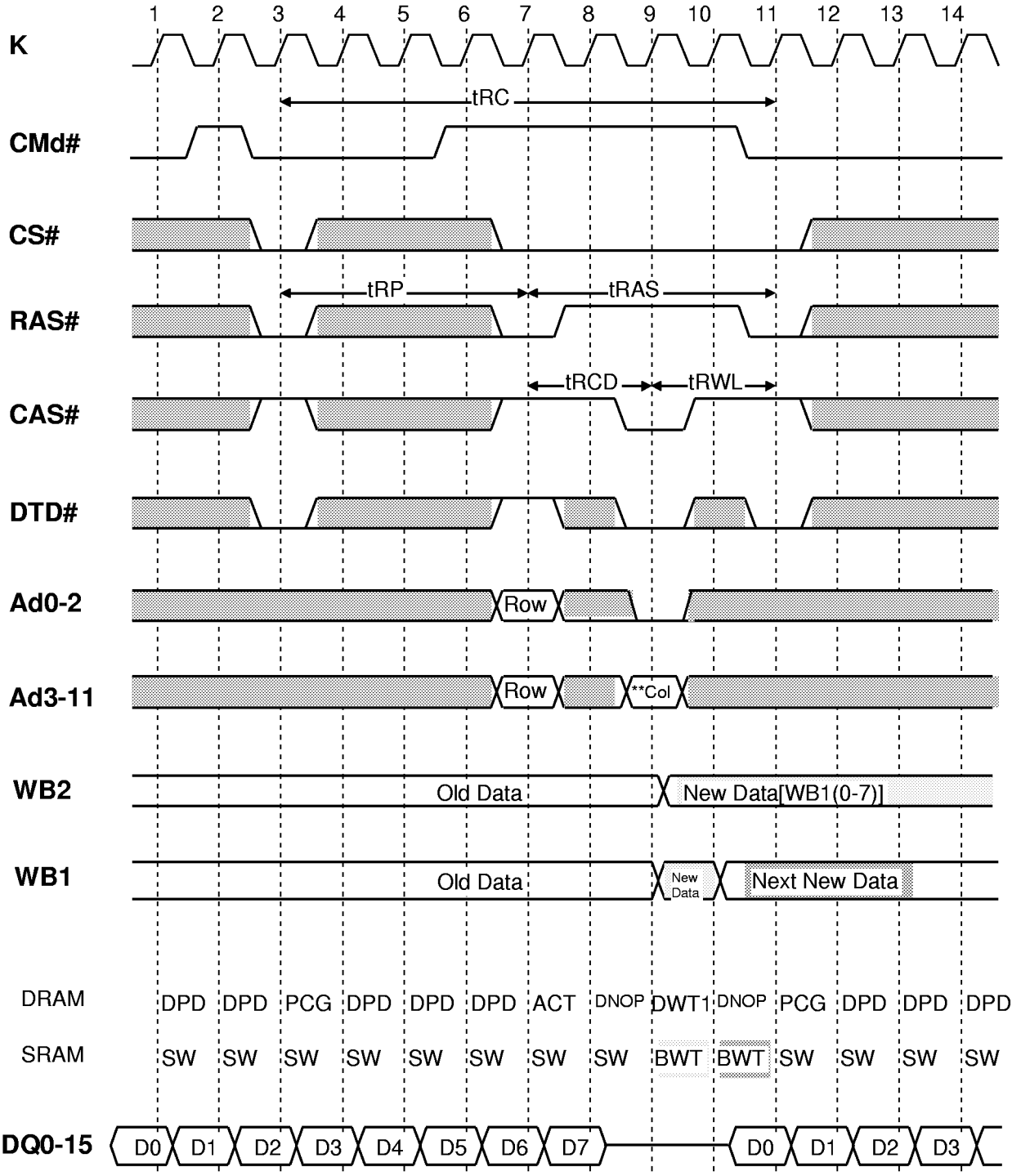
detail



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write Transfer (SRAM->WB1)



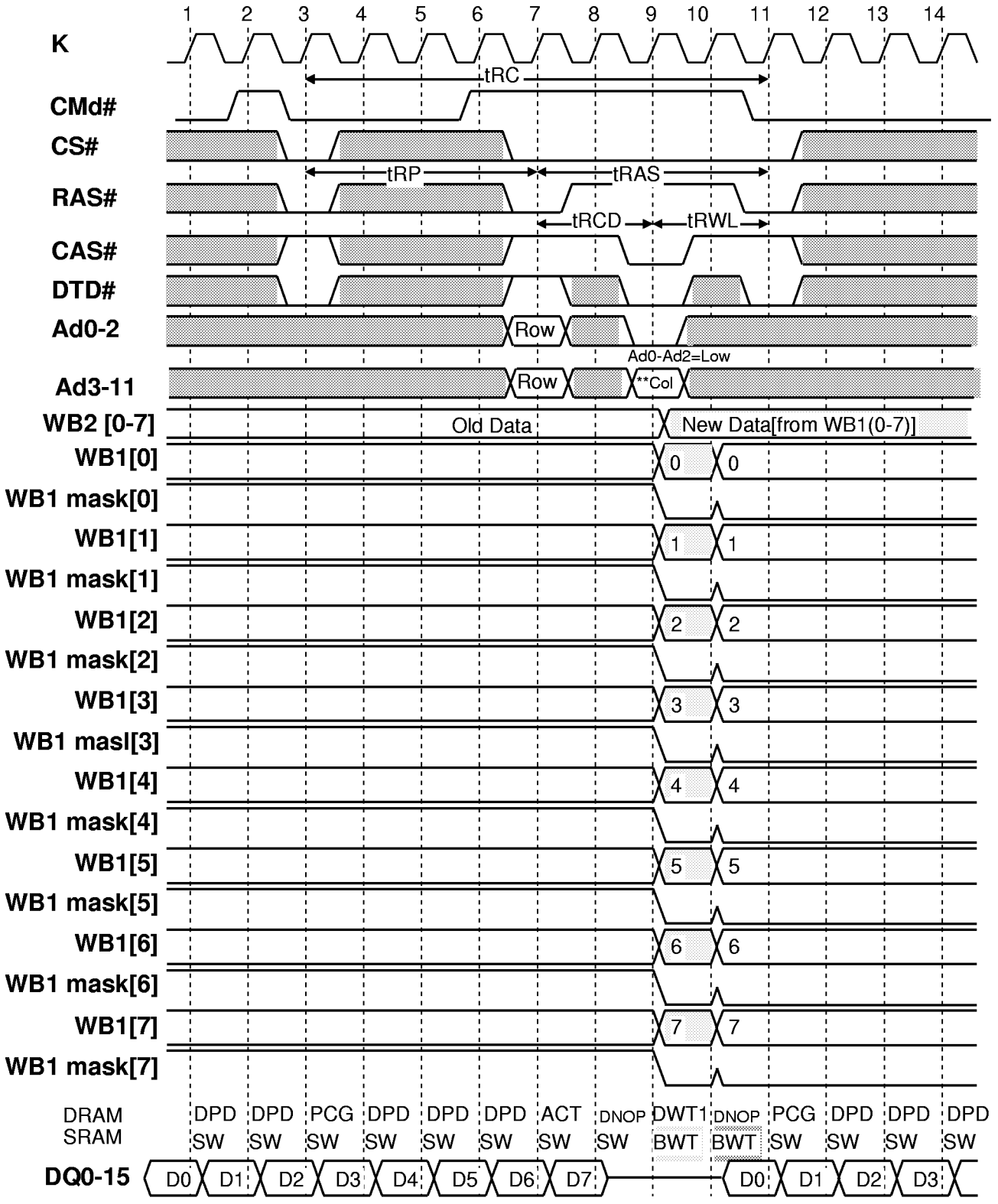
Please refer to next page in detail.

SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write Transfer (SRAM->WB1)

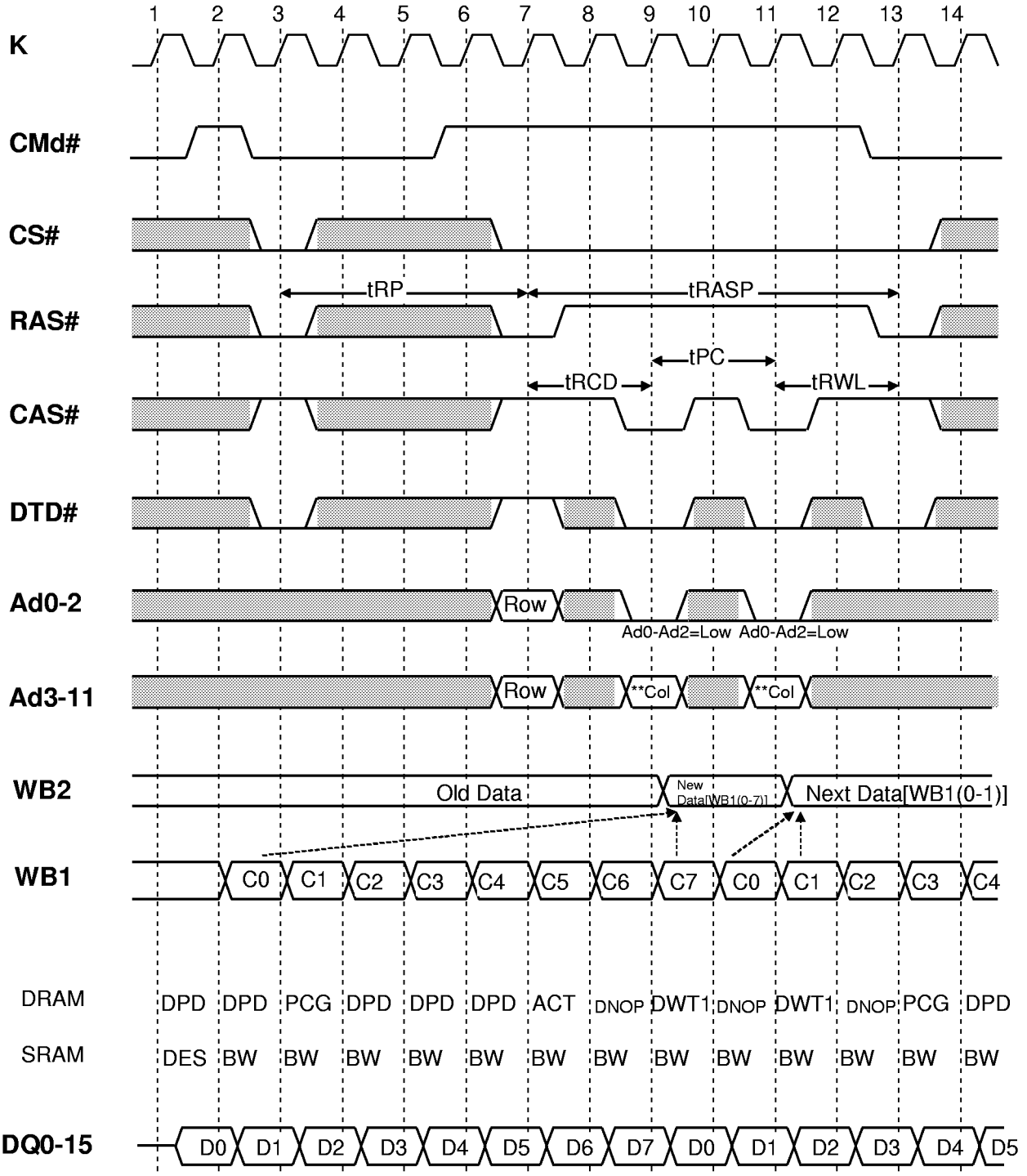
detail



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

Page-Mode DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write (DIN->WB1)



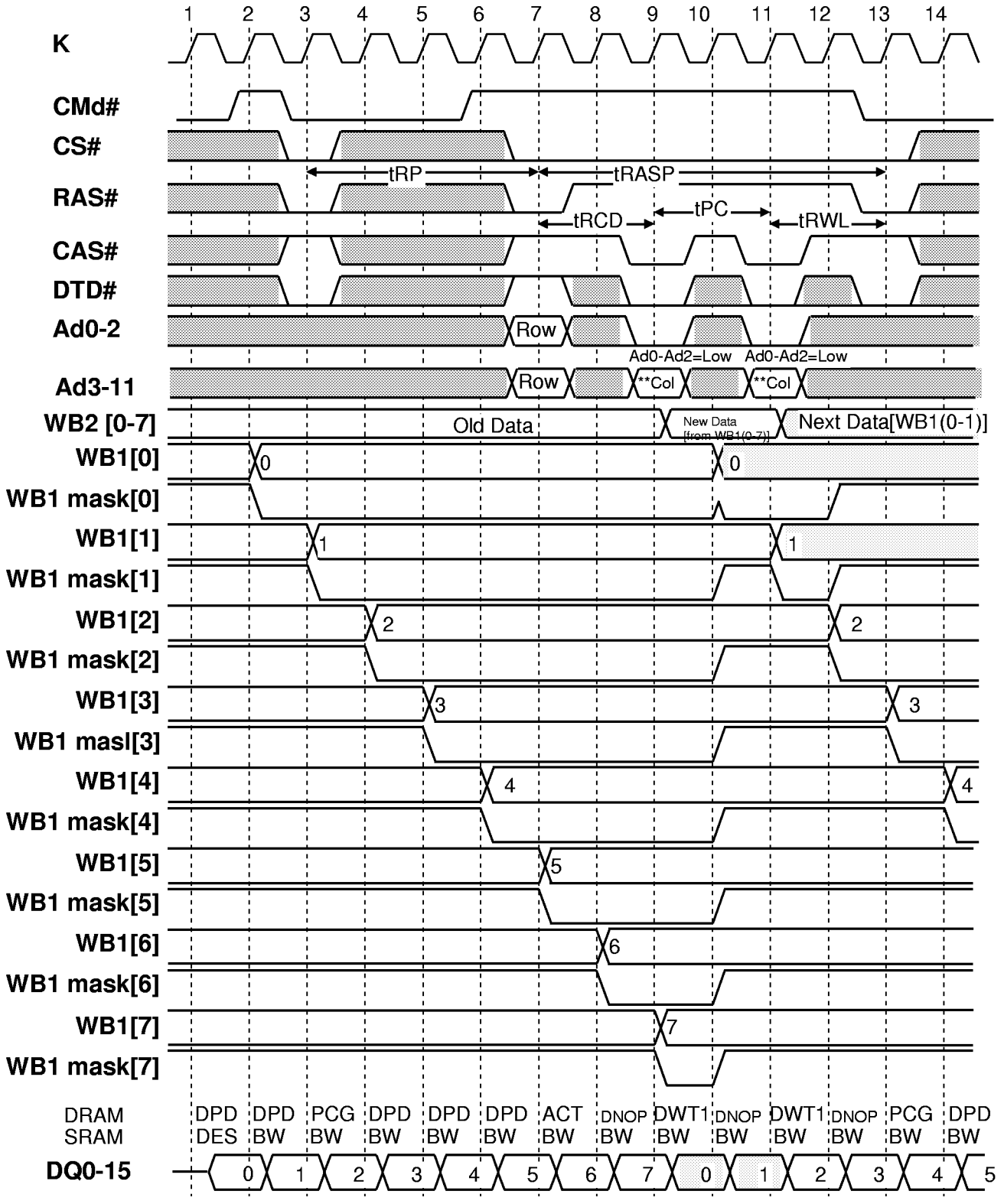
Please refer to next page in detail.

SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

Page-Mode DRAM Write Transfer 1 (WB1->WB2->DRAM)
Buffer Write (DIN->WB1)

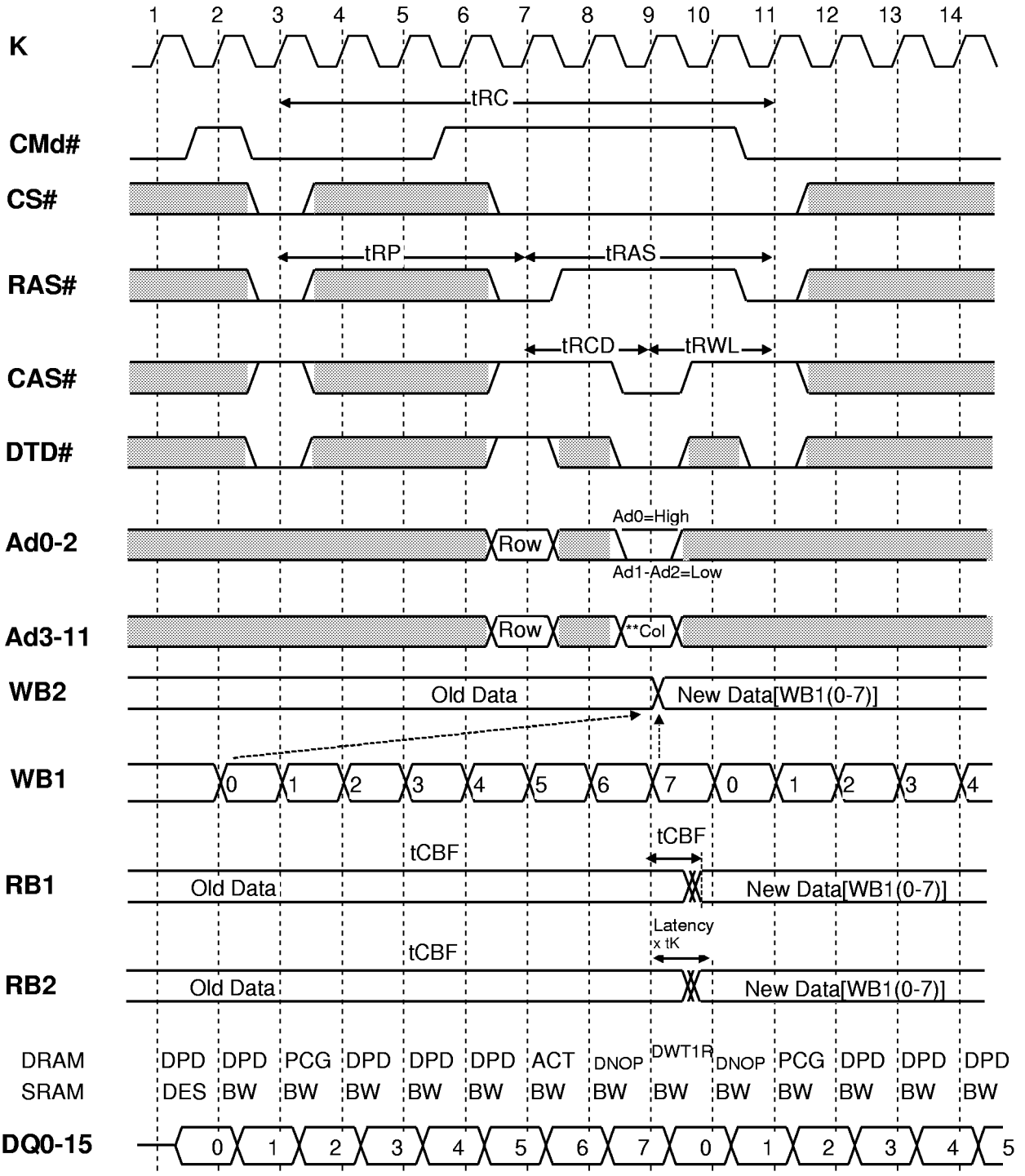
detail



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

DRAM Write Transfer 1&Read (WB1->WB2->DRAM->RB) Latency set=1
Buffer Write (DIN->WB1)

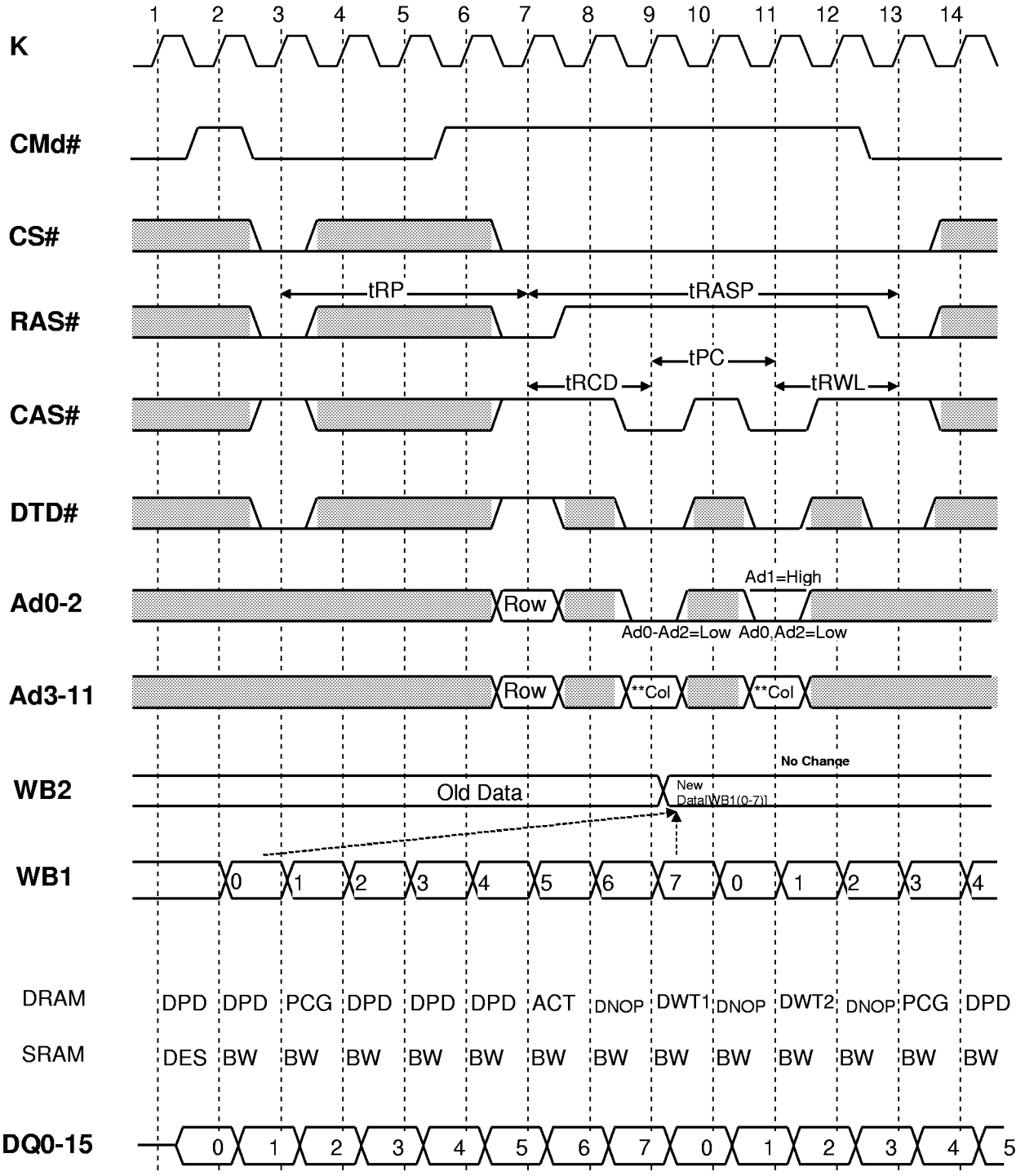


New Data on RB appears as to latency set count. See DRT timing chart.

SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

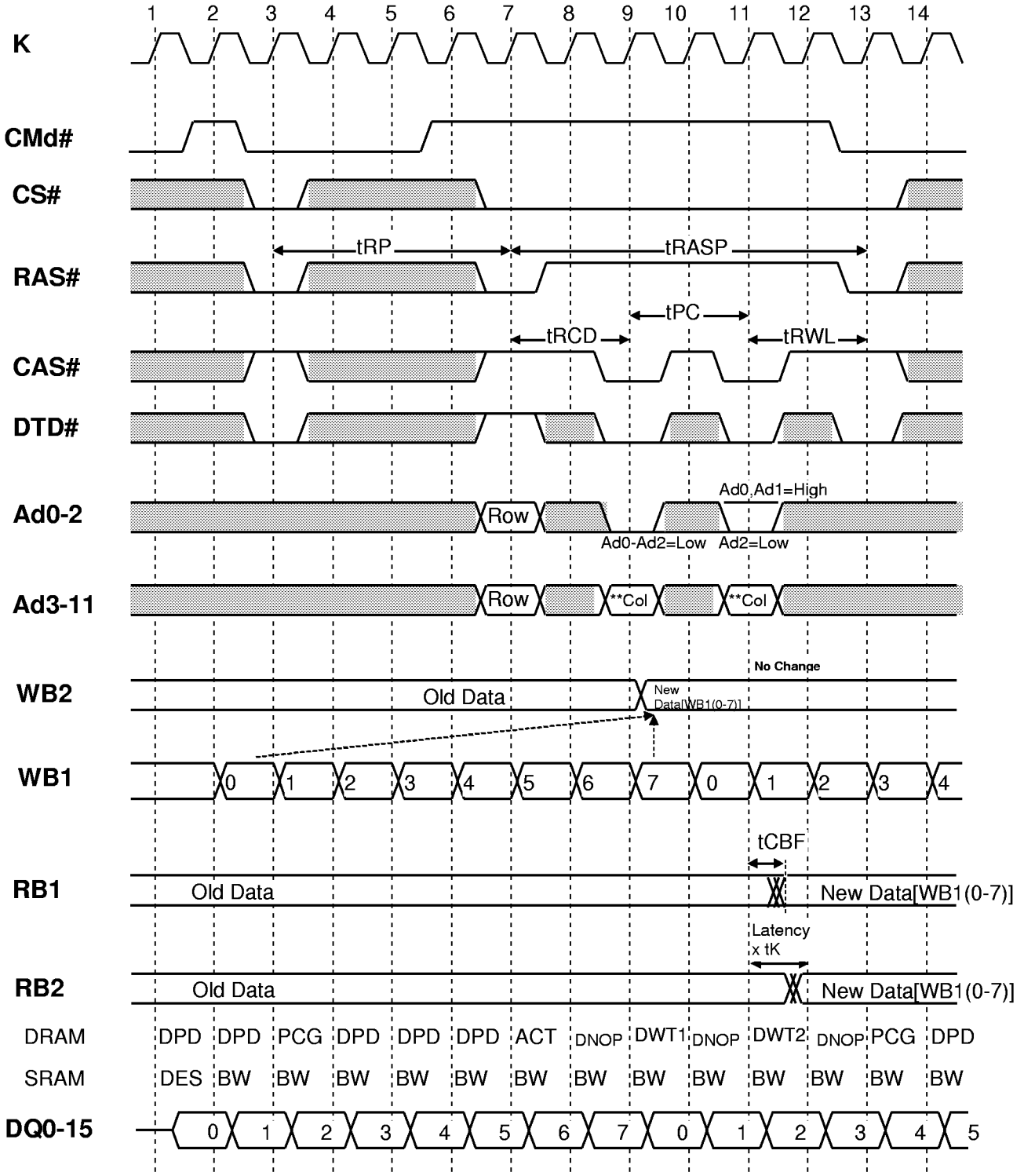
DRAM Write Transfer 2 (WB2->DRAM)



SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

DRAM Write Transfer2 & Read (WB2->DRAM->RB) Latency set=1

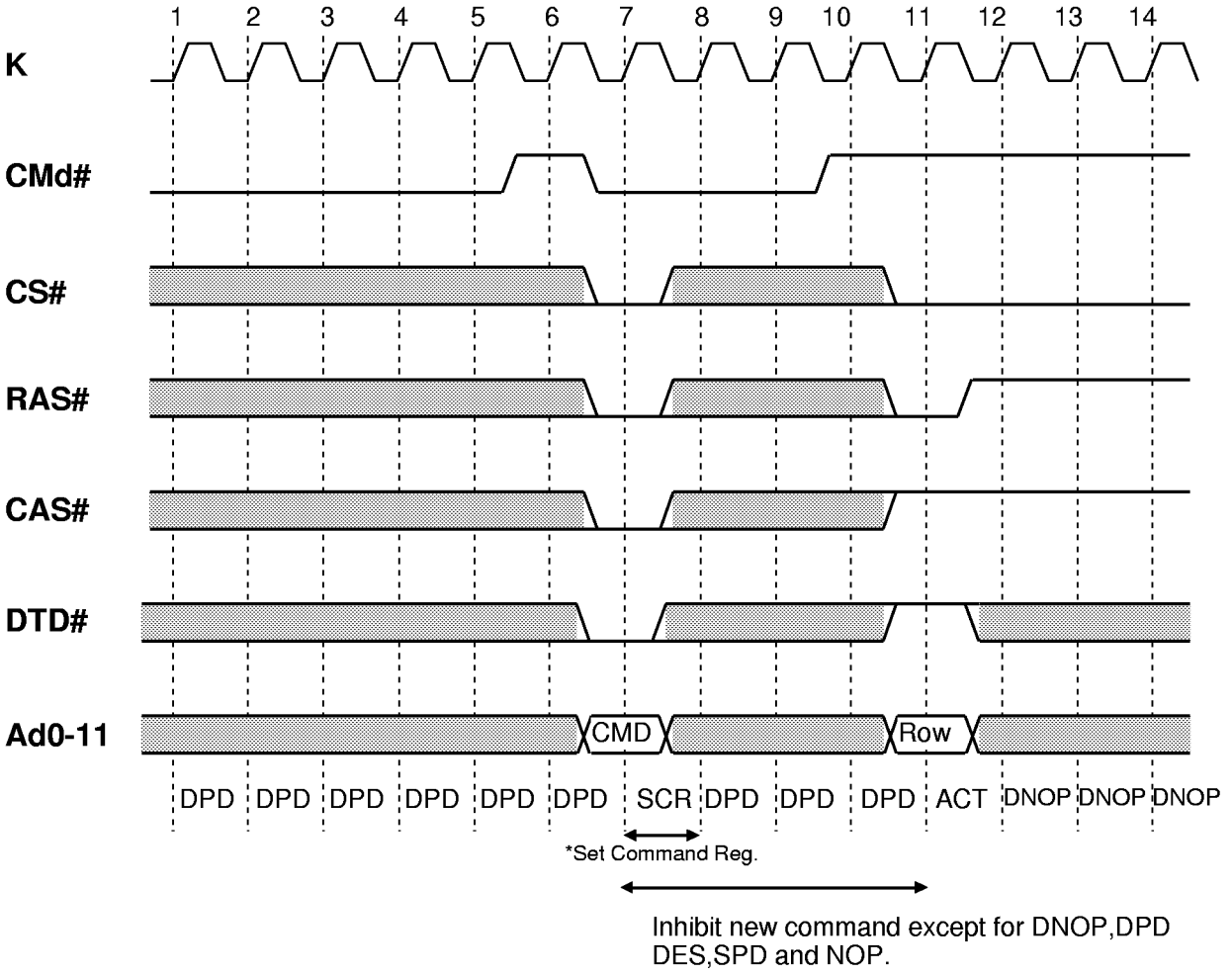


New Data on RB appears as to latency set count. See DRT timing chart.

SRAM operation can be freely performed.

** Ad3-Ad7 are column block addresses (Ad8-Ad11=Low).

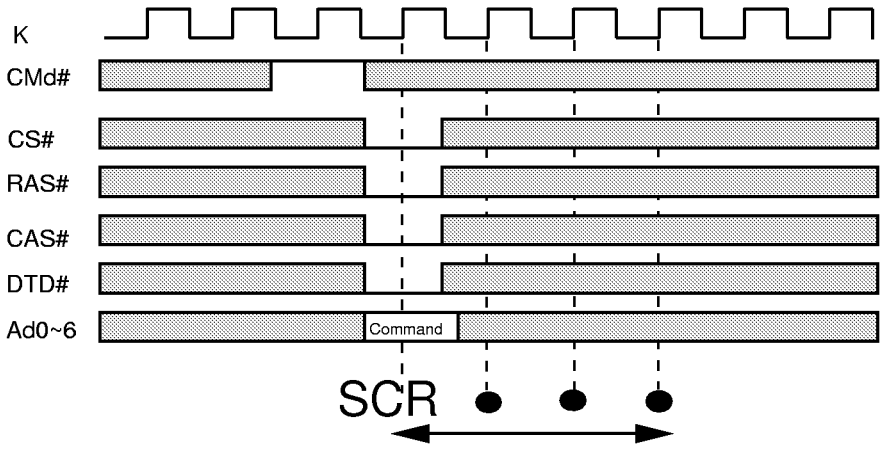
Set Command Register



* Ad0-11 must be set according to set command truth table while Ad8-Ad11=Low

Set Command Register
Detailed Truth Table for SCR

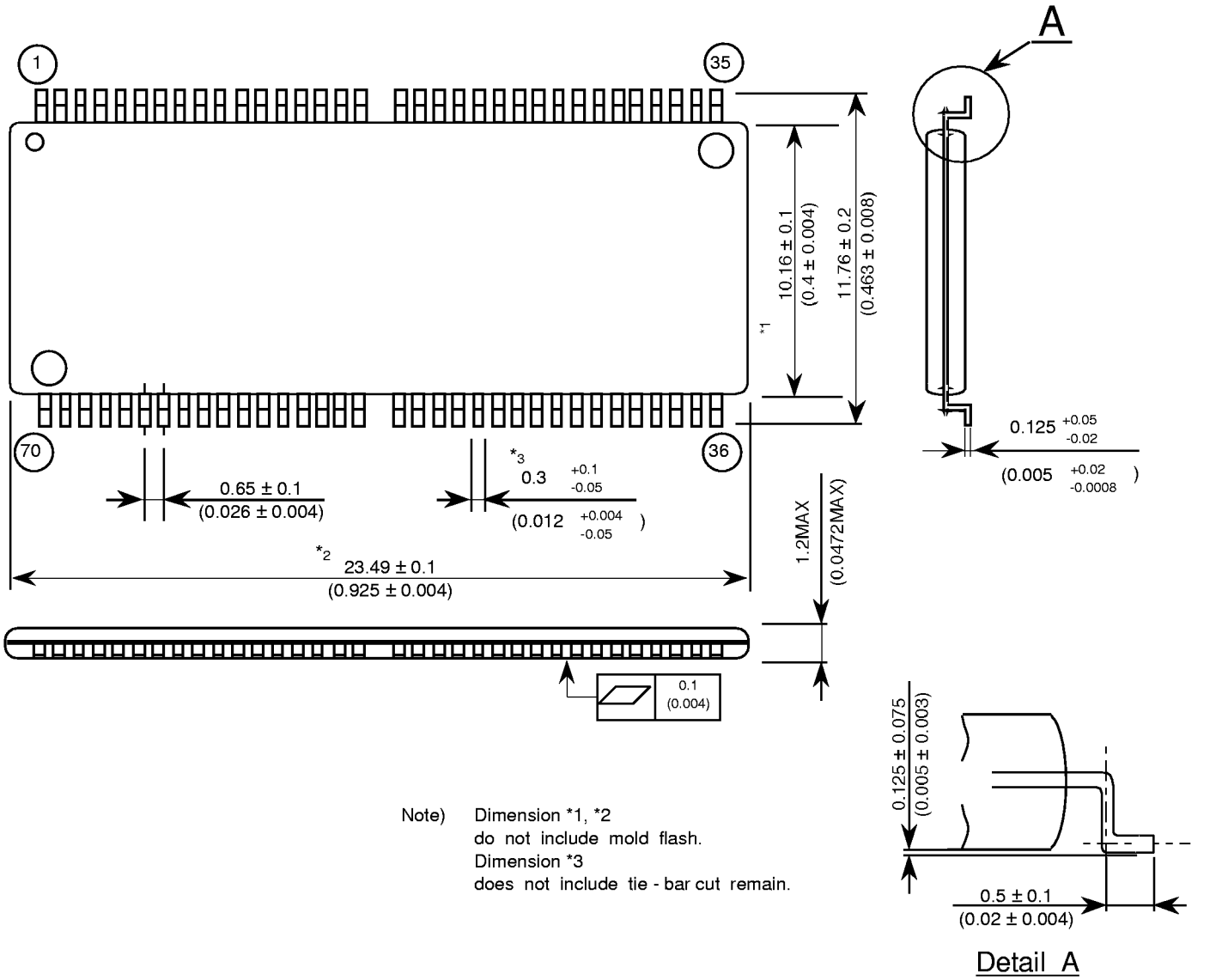
Address Input												Command
Ad11	Ad10	Ad9	Ad8	Ad7	Ad6	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0	
L	X	X	X	X	L	L	L	X	X	L	X	* Latency 1
L	X	X	X	X	L	L	H	X	X	L	X	2
L	X	X	X	X	L	H	L	X	X	L	X	3
L	X	X	X	X	L	H	H	X	X	L	X	4
L	X	X	X	X	X	X	X	L	L	L	X	Output Mode Transparent
L	X	X	X	X	X	X	X	L	H	L	X	Latched
L	X	X	X	X	X	X	X	H	L	L	X	Registered
L	X	X	X	X	X	X	X	X	X	L	L	No Operation of Mask
L	X	X	X	X	X	X	X	X	X	L	H	Set All WB1 Xfer Masks
L	X	X	L	L	X	X	X	X	X	L	X	reserved
L	X	X	L	H	X	X	X	X	X	L	X	reserved
L	X	X	H	L	X	X	X	X	X	L	X	reserved
L	X	X	H	H	X	X	X	X	X	L	X	reserved
L	X	L	X	X	X	X	X	X	X	L	X	reserved
L	X	H	X	X	X	X	X	X	X	L	X	reserved



Inhibit new read or write function during these 4 clocks.

* **Latency** is the number of clock cycles required to transfer new data from the DRAM to the Read Buffer . Therefore, it can be adjusted to the clock frequency of the system. (Latency) x (tK) should meet tCBF min. timing requirement.

70P3S Package Dimension



Note) Dimension *1, *2
do not include mold flash.
Dimension *3
does not include tie - bar cut remain.

UNIT : mm / (INCH)