Signetics

74170, LS170
Register Files

4 x 4 Register File (Open Collector)
Product Specification

Logic Products

FEATURES

- **Simultaneous and independent Read and Write operations**
- **Expandable to 1024 words by n-bits**
- **Open Collector outputs for wired-AND expansion**
- **See '670 for 3-State output version**

DESCRIPTION

The '170 is a 16-bit register file organized as 4 words of 4 bits each, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable ($\overline{WE}$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form. Data and Write Address inputs are inhibited when $\overline{WE}$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is LOW. Data outputs are inhibited and remain HIGH when the Read Enable input is HIGH. This permits simultaneous reading and writing, eliminates recovery times, and is limited in speed only by the read time and the write time.

Up to 256 devices can be stacked to increase the word size to 1024 locations by tying the Open Collector outputs together. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

TYPE	TYPICAL PROPAGATION DELAY (RE to Q)	TYPICAL SUPPLY CURRENT (TOTAL)
74170	10ns (t_{PLH}) 20ns (t_{PHL})	127mA
74LS170	20ns (t_{PLH}) 20ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74170N, N74LS170N

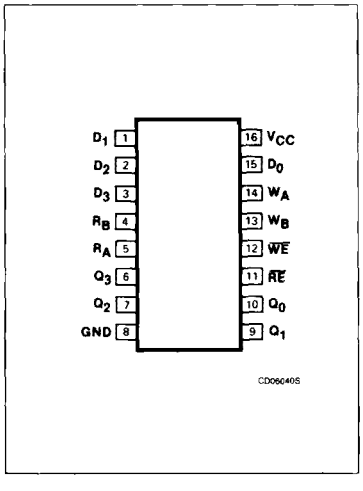
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

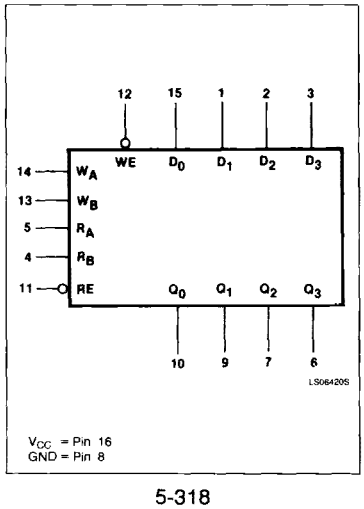
PINS	DESCRIPTION	74	74LS
D, W_A, W_B, R_A, R_B	Inputs	1ul	1LSul
$\overline{WE}$, $\overline{RE}$	Inputs	1ul	2LSul
All	Outputs	10ul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL} and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

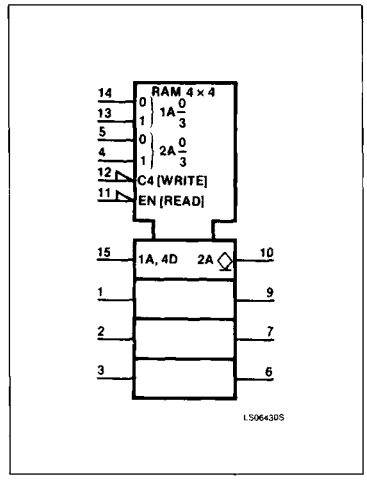
PIN CONFIGURATION



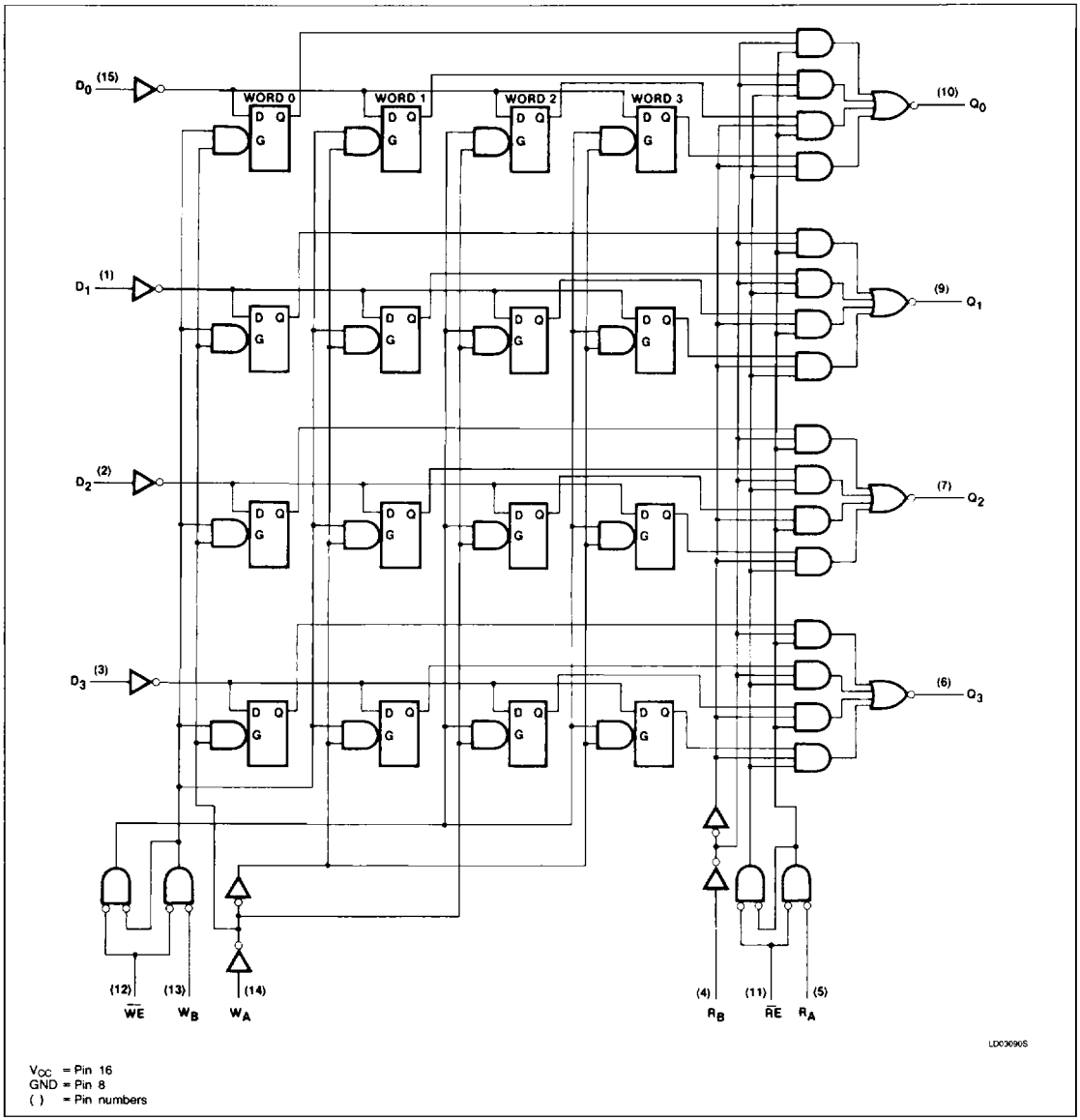
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES[a]
	$\overline{WE}$	D_n	
Write data	L	L	L
	L	H	H
Data latched	H	X	no change

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS
	$\overline{RE}$	Internal Latches[b]	Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care.

NOTES:

a. The Write Address (W_A and W_C) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.

b. The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	−0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18	mA
V_{OH}	HIGH-level output voltage			5.5			5.5	V
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74170			74LS170			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					30			100	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX		I_{OL} = MAX		0.2	0.4		0.35	0.5	V
				I_{OL} = 4mA (74LS)					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	D, W_A, W_B, R_A, R_B inputs						0.1	mA
				$\overline{WE}$, $\overline{RE}$ inputs						0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V	D, W_A, W_B, R_A, R_B inputs						20	μA
				$\overline{WE}$, $\overline{RE}$ inputs						40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		D, W_A, W_B, R_A, R_B inputs			−1.6			−0.4	mA
				$\overline{WE}$, $\overline{RE}$ inputs			−1.6			−0.8	mA
I_{CC}	Supply current[3] (total)	V_{CC} = MAX				127	150		25	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Measure I_{CC} with 4.5V applied to all Data and both Enable inputs, the Address inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Read Enable to output	Waveform 1		15 30		30 30	ns
t_{PLH} t_{PHL}	Propagation delay Read Address to output	Waveform 2		35 40		40 40	ns
t_{PLH} t_{PHL}	Propagation delay Write Enable to output	Waveform 1		40 45		45 40	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		30 45		45 35	ns

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AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

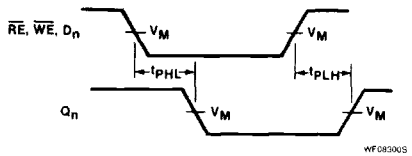
PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			Min	Max	Min	Max	
t_W	Write enable pulse width	Waveform 3	25		25		ns
t_s	Set-up time, data to positive-going $\overline{WE}$[c]	Waveform 3	10		10		ns
t_h	Hold time, data to positive-going $\overline{WE}$[c]	Waveform 3	15		15		ns
t_s	Set-up time, read address to negative-going $\overline{WE}$[c]	Waveform 3	15		15		ns
t_h	Hold time, read address to positive-going $\overline{WE}$[c]	Waveform 3	5.0		5.0		ns
t_W	Read enable pulse width	Waveform 4	25		25		ns
t_{latch}	Latch time for new data[d]	Waveform 5	25		25		ns

NOTES:

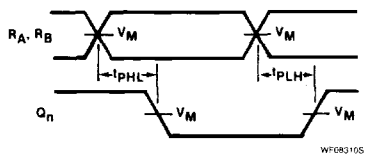
c. Write Address set-up time will protect the data written into the previous address. If protection of data in the previous address is not required, t_s (Write Address to $\overline{WE}$) can be ignored, as any address selection sustained for the final 30ns of the $\overline{WE}$ pulse and during t_h (Write Address to $\overline{WE}$) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

d. Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of $\overline{WE}$ to the rising edge of R_A or R_B. $\overline{RE}$ must be LOW.

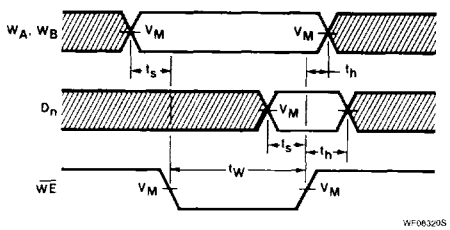
AC WAVEFORMS



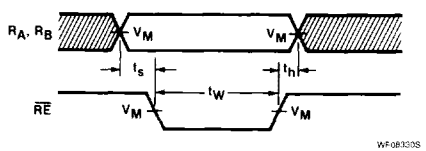
Waveform 1. Propagation Delay Read Enable, Write Enable And Data To Outputs



Waveform 2. Propagation Delay Read Address To Outputs

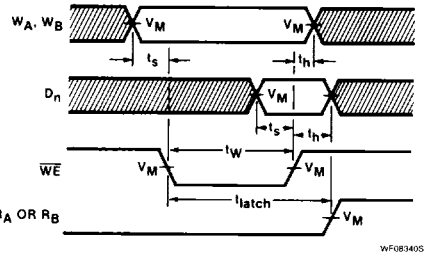


Waveform 3. Set-up And Hold Times Write Address And Data To Write Enable



Waveform 4. Set-up And Hold Times Read Address To Read Enable

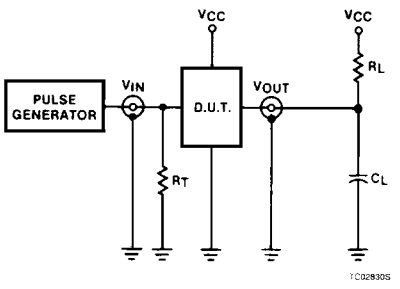
AC WAVEFORMS (Continued)



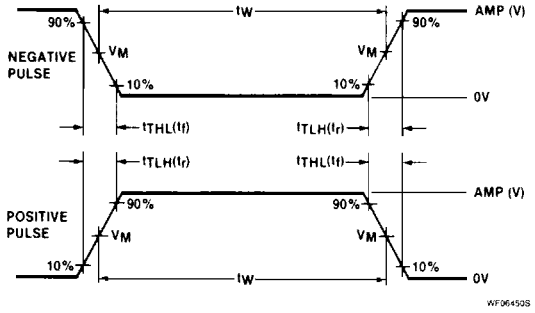
For all waveforms, V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5. Set-up And Hold Times Write Address And Data To Write Enable

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns