

2GB – 2x128Mx64 DDR2 SDRAM UNBUFFERED

FEATURES

- Unbuffered 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4300 and PC2-3200
- $V_{CC} = V_{CCQ} = 1.8V$
- $V_{CCSPD} = +1.7V$ to $+3.6V$
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, 5* and 6*
- Adjustable data-output drive strength
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Auto & self refresh (64ms 8,192 cycle refresh)
- Gold edge contacts
- Product is lead-free
- Dual Rank
- RoHS compliant
- Package option
 - 240 Pin DIMM
 - 30.00mm (1.181") TYP

DESCRIPTION

The WV3HG2128M64EEU is a 2x128Mx64 Double Data Rate DDR2 SDRAM high density module. This memory module consists of sixteen 128Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 240-pin DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

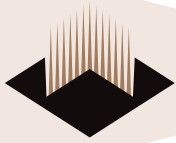
NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option
- Parity function

OPERATING FREQUENCIES

	PC2-6400*	PC2-5300*	PC2-4300	PC2-3200
Clock Speed	400MHz	333MHz	266MHz	200MHz
CL-trCD-trP	6-6-6	5-5-5	4-4-4	3-3-3

* Consult factory for availability



PIN CONFIGURATION

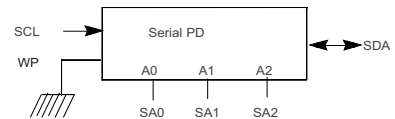
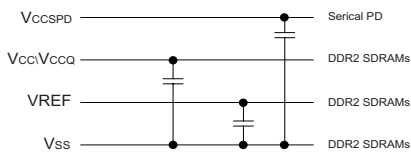
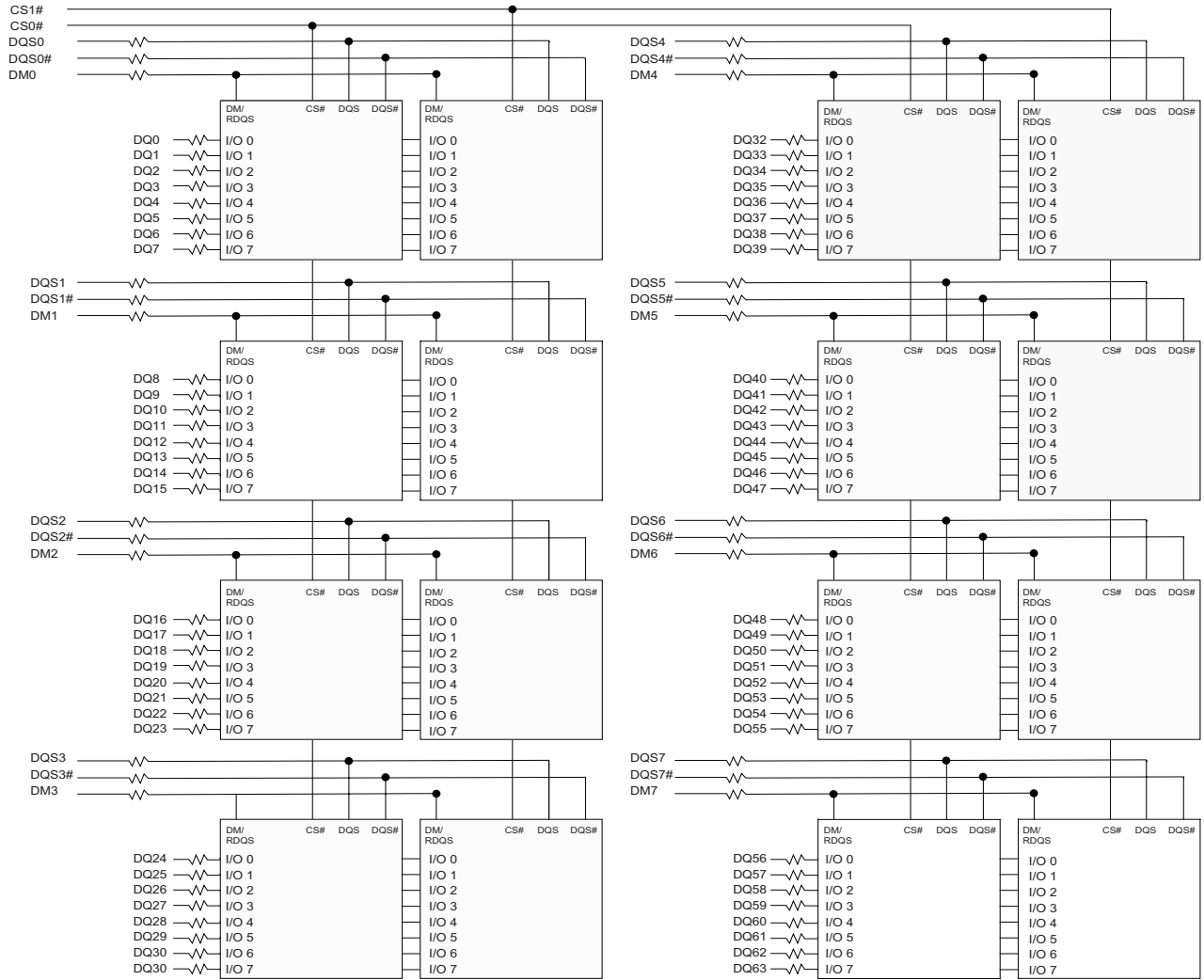
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	VREF	61	A4	121	Vss	181	Vcc
2	Vss	62	Vcc	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	Vcc	124	Vss	184	Vcc
5	Vss	65	Vss	125	DM0	185	CK0
6	DQS0#	66	Vss	126	NC	186	CK0#
7	DQS0	67	Vcc	127	Vss	187	Vcc
8	Vss	68	NC	128	DQ6	188	A0
9	DQ2	69	Vcc	129	DQ7	189	Vcc
10	DQ3	70	A10/AP	130	Vss	190	BA1
11	Vss	71	BA0	131	DQ12	191	Vcc
12	DQ8	72	Vcc	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	Vss	193	CS0#
14	Vss	74	CAS#	134	DM1	194	Vcc
15	DQS1#	75	Vcc	135	NC	195	ODT0
16	DQS1	76	CS1#	136	Vss	196	A13
17	Vss	77	ODT1	137	CK1	197	Vcc
18	NC	78	Vccq	138	CK1#	198	Vss
19	NC	79	Vss	139	Vss	199	DQ36
20	Vss	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	Vss
22	DQ11	82	Vss	142	Vss	202	DM4
23	Vss	83	DQS4#	143	DQ20	203	NC
24	DQ16	84	DQS4	144	DQ21	204	Vss
25	DQ17	85	Vss	145	Vss	205	DQ38
26	Vss	86	DQ34	146	DM2	206	DQ39
27	DQS2#	87	DQ35	147	NC	207	Vss
28	DQS2	88	Vss	148	Vss	208	DQ44
29	Vss	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	Vss
31	DQ19	91	Vss	151	Vss	211	DM5
32	Vss	92	DQS5#	152	DQ28	212	NC
33	DQ24	93	DQS5	153	DQ29	213	Vss
34	DQ25	94	Vss	154	Vss	214	DQ46
35	Vss	95	DQ42	155	DM3	215	DQ47
36	DQS3#	96	DQ43	156	NC	216	Vss
37	DQS3	97	Vss	157	Vss	217	DQ52
38	Vss	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	Vss
40	DQ27	100	Vss	160	Vss	220	CK2
41	Vss	101	SA2	161	NC	221	CK2#
42	NC	102	NC	162	NC	222	Vss
43	NC	103	Vss	163	Vss	223	DM6
44	Vss	104	DQS6#	164	NC	224	NC
45	NC	105	DQS6	165	NC	225	Vss
46	NC	106	Vss	166	Vss	226	DQ54
47	Vss	107	DQ50	167	NC	227	DQ55
48	NC	108	DQ51	168	NC	228	Vss
49	NC	109	Vss	169	Vss	229	DQ60
50	Vss	110	DQ56	170	Vcc	230	DQ61
51	Vcc	111	DQ57	171	CKE1	231	Vss
52	CKE0	112	Vss	172	Vcc	232	DM7
53	Vcc	113	DQS7#	173	NC	233	NC
54	BA2	114	DQS7	174	NC	234	Vss
55	NC	115	Vss	175	Vcc	235	DQ62
56	Vcc	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	Vss
58	A7	118	Vss	178	Vcc	238	VccSPD
59	Vcc	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
BA0,BA2	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data strobes
DQS0#-DQS7#	Data strobes complement
DM0-DM7	Data masks
ODT0, ODT1	On-die termination control
CK0,CK0#-CK2,CK2#	Clock Inputs
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
SA0-SA2	SPD address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
Vcc	Core Power (1.8V)
Vss	Ground
VREF	Power Supply for Reference
VccSPD	SPD Power
NC	Spare pins, No connect



FUNCTIONAL BLOCK DIAGRAM

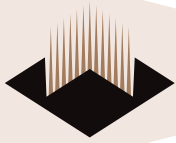


- CS0# ——— CS0#: DDR 2 SDRAMs
- CS1# ——— CS1#: DDR 2 SDRAMs
- BA0-BA2 ——— BA0-BA2: DDR 2 SDRAMs
- A0-A13 ——— A0-A13: DDR 2 SDRAMs
- RAS# ——— RAS#: DDR 2 SDRAMs
- CAS# ——— CAS#: DDR 2 SDRAMs
- WE# ——— WE#: DDR 2 SDRAMs
- CKE0 ——— CKE0: DDR 2 SDRAMs
- CKE1 ——— CKE1: DDR 2 SDRAMs
- ODT0 ——— ODT0: DDR 2 SDRAMs
- ODT1 ——— ODT1: DDR 2 SDRAMs

*Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0#	4 DDR2 SDRAMs
*CK1/CK1#	6 DDR2 SDRAMs
*CK2/CK2#	6 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

- Notes:
1. DQ, DM, DQS/DQS# resistors: 5.1 Ohms +/-5%
 2. BAx, Ax RAS#, CAS#, WE# resistors: 5.1 Ohms +/- 5%



DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V _{CC}	1.7	1.8	1.9	V	3
I/O Reference Voltage	V _{REF}	0.49 x V _{CC}	0.50 x V _{CC}	0.51 x V _{CC}	V	1
I/O Termination Voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	2
SPD Supply Voltage	V _{CCSPD}	1.7	-	3.6	V	

Notes:

- V_{REF} is expected to equal V_{CC2} of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- V_{CCQ} of all IC's are tied to V_{CC}.

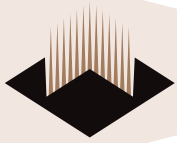
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-0.5	2.3	V	
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5	2.3	V	
T _{STG}	Storage Temperature	-55	100	°C	
I _L	Input leakage current; Any input 0V<V _{IN} <V _{CC} ; V _{REF} input 0V,V _{IN} ,0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#	-80	80	µA
		CS#, CKE	-40	40	µA
		CK, CK#	-30	30	µA
		DM	-10	10	µA
I _{OZ}	Output leakage current; 0V<V _{IN} <V _{CC} ; DQs and ODT are disable	-10	10	µA	
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level	-32	32	µA	

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz, V_{CC} = 1.8V

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A13, BA0-BA2, RAS#, CAS#, WE#)	C _{IN1}	20	36	pF
Input Capacitance (CKE0, CKE1), (ODT0, ODT1)	C _{IN2}	12	20	pF
Input Capacitance (CS0#, CS1#)	C _{IN3}	12	20	pF
Input Capacitance (CK0, CK0#-CK2, CK2#)	C _{IN4}	10	16	pF
Input Capacitance (DQS0-DQS7), (DM0-DM7)	C _{IN5} (665)	9	11	pF
	C _{IN5} (534, 403)	9	12	pF
Input Capacitance (DQ0-DQ63)	C _{OUT} (665)	9	11	pF
	C _{OUT} (534, 403)	9	12	pF



OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating Temperature (Commercial)	TOPER	0°C to 85°C	°C	1, 2

Notes:

- Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2.
- At 0 - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

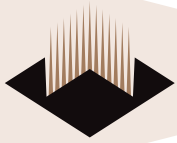
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V _{IH(DC)}	V _{REF} + 0.125	V _{CC} + 0.300	V
Input Low (Logic 0) Voltage	V _{IL(DC)}	-0.300	V _{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
AC Input Low (Logic 1) Voltage DDR2-400 & DDR2-533	V _{IL(AC)}	V _{REF} + 0.250		V
AC Input High (Logic 1) Voltage DDR2-667	V _{IH(AC)}	V _{REF} + 0.200		V
AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V _{IL(AC)}		V _{REF} - 0.250	V
AC Input Low (Logic 0) Voltage DDR2-667	V _{IL(AC)}		V _{REF} - 0.200	V



DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

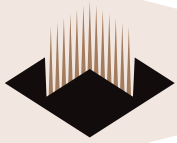
DDR2 SDRAM components only

Symbol	Proposed Conditions	806	665	553	403	Units	
I _{CC0} *	Operating one bank active-precharge current; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	816	776	736	mA	
I _{CC1} *	Operating one bank active-read-precharge current; I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}), t _{RCD} = t _{RCD} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W}	TBD	896	856	816	mA	
I _{CC2P} *	Precharge power-down current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	192	192	192	mA	
I _{CC2Q} **	Precharge quiet standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	640	560	560	mA	
I _{CC2N} **	Precharge standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	720	640	640	mA	
I _{CC3P} **	Active power-down current; All banks open; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	480	400	400	mA
		Slow PDN Exit MRS(12) = 1	TBD	192	192	192	mA
I _{CC3N} **	Active standby current; All banks open; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	800	720	720	mA	
I _{CC4W} *	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1,336	1,136	1,016	mA	
I _{CC4R} *	Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W}	TBD	1,336	1,136	1,016	mA	
I _{CC5B} **	Burst auto refresh current; t _{CK} = t _{CK} (I _{CC}); Refresh command at every t _{REF} (I _{CC}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	3,520	3,440	3,360	mA	
I _{CC6} **	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	160	160	160	mA
I _{CC7} *	Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = t _{RCD} (I _{CC})-1*t _{CK} (I _{CC}); t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RRD} = t _{RRD} (I _{CC}), t _{RCD} = 1*t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.	TBD	2,496	2,336	2,176	mA	

Note: I_{CC} specification is based on SAMSUNG components. Other DRAM Manufacturers specification may be different.

*: Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** : Value calculated reflects all module ranks in this operating condition.



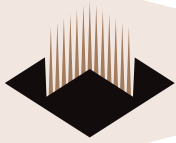
DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATION

V_{CC} = +1.8V ± 0.1V

AC CHARACTERISTICS			806		665		534		403			
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 6	t _{CK(6)}	TBD	TBD							ps
		CL = 5	t _{CK(5)}	TBD	TBD	3,000	8,000					ps
		CL = 4	t _{CK(4)}	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	t _{CK(3)}	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width		t _{CH}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	tck
	CK low-level width		t _{CL}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	tck
	Half clock period		t _{HP}	TBD	TBD	MIN(t _{CH} ,t _{CL})		MIN(t _{CH} ,t _{CL})		MIN(t _{CH} ,t _{CL})		ps
	Clock jitter		t _{JIT}	TBD	TBD	-125	125	-125	125	-125	125	ps
Data	DQ output access time from CK/CK#		t _{AC}	TBD	TBD	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t _{HZ}	TBD	TBD		t _{AC} (MAX)		t _{AC} (MAX)		t _{AC} (MAX)	ps
	Data-out low-impedance window from CK/CK#		t _{LZ}	TBD	TBD	t _{AC} (MIN)	t _{AC} (MAX)	t _{AC} (MIN)	t _{AC} (MAX)	t _{AC} (MIN)	t _{AC} (MAX)	ps
	DQ and DM input setup time relative to DQS		t _{DS}	TBD	TBD	100		100		150		
	DQ and DM input hold time relative to DQS		t _{DH}	TBD	TBD	225		225		275		
	DQ and DM input pulse width (for each input)		t _{DIPW}	TBD	TBD	0.35		0.35		0.35		tck
	Data hold skew factor		t _{QHS}	TBD	TBD		340		400		450	ps
	DQ - DQS hold, DQS to first DQ to go nonvalid, per access		t _{QH}	TBD	TBD	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ps
	Data valid output window (DVW)		t _{DVW}	TBD	TBD	t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		ns
Data Strobe	DQS input high pulse width		t _{DQSH}	TBD	TBD	0.35		0.35		0.35		tck
	DQS input low pulse width		t _{DQSL}	TBD	TBD	0.35		0.35		0.35		tck
	DQS output access time from CK/CK#		t _{DQSCK}	TBD	TBD	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising - setup time		t _{DSS}	TBD	TBD	0.2		0.2		0.2		tck
	DQS falling edge from CK rising - hold time		t _{DSH}	TBD	TBD	0.2		0.2		0.2		tck
	DQS - DQ skew, DQS to last DQ valid, per group, per access		t _{DQSQ}	TBD	TBD		240		300		350	ps
	DQS read preamble		t _{RPRE}	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	tck
	DQS read postamble		t _{RPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	tck
	DQS write preamble setup time		t _{WPRES}	TBD	TBD	0		0		0		ps
	DQS write preamble		t _{WPRE}	TBD	TBD	0.35		0.35		0.35		tck
	DQS write postamble		t _{WPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	tck
	Write command to first DQS latching transition		t _{DQSS}	TBD	TBD	WL- 0.25	WL+ 0.25	WL- 0.25	WL+ 0.25	WL- 0.25	WL+ 0.25	tck
	Address and control input pulse width for each input		t _{IPW}	TBD	TBD	0.6		0.6		0.6		tck
Address and control input setup time		t _{IS}	TBD	TBD	200		250		350		ps	
Address and control input hold time		t _{IH}	TBD	TBD	275		375		475		ps	
Address and control input hold time		t _{CCD}	TBD	TBD	2		2		2		tck	

* AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

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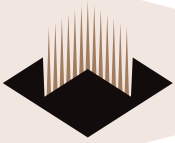


DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATION (cont'd)

V_{CC} = +1.8V ± 0.1V

AC CHARACTERISTICS			806		665		534		403		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t _{RC}	TBD	TBD	55		55		55		ns
	ACTIVE bank a to ACTIVE bank b command	t _{RRD}	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t _{RCD}	TBD	TBD	15		15		15		ns
	Four Bank Activate period	t _{FAW}	TBD	TBD	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t _{TRAS}	TBD	TBD	40	70,000	40	70,000	40	70,000	ns
	Internal READ to precharge command delay	t _{RTP}	TBD	TBD	7.5		7.5		7.5		ns
	Write recovery time	t _{WR}	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	t _{DAL}	TBD	TBD	t _{WR} +t _{RP}		t _{WR} +t _{RP}		t _{WR} +t _{RP}		ns
	Internal WRITE to READ command delay	t _{WTR}	TBD	TBD	7.5		7.5		10		ns
	PRECHARGE command period	t _{RP}	TBD	TBD	15		15		15		ns
	PRECHARGE ALL command period	t _{RPA}	TBD	TBD	t _{RP} +t _{CK}		t _{RP} +t _{CK}		t _{RP} +t _{CK}		ns
	LOAD MODE command cycle time	t _{MRD}	TBD	TBD	2		2		2		tck
	CKE low to CK,CK# uncertainty	t _{DELAY}	TBD	TBD	t _{IS} +t _{CK} t _{IH}		t _{IS} +t _{CK} t _{IH}		t _{IS} +t _{CK} t _{IH}		ns
Self Refresh	REFRESH to Active of Refresh to Refresh command interfal	t _{RFC}	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t _{REFI}	TBD	TBD		7.8		7.8		7.8	µs
	Exit self refresh to non-READ command	t _{XSNR}	TBD	TBD	t _{RFC(MIN)} +10		t _{RFC(MIN)} +10		t _{RFC(MIN)} +10		ns
	Exit self refresh to READ command	t _{XSRD}	TBD	TBD	200		200		200		tck
	Exit self refresh timing reference	t _{ISXR}	TBD	TBD	t _{IS}		t _{IS}		t _{IS}		ps
ODT	ODT turn-on delay	t _{AOND}	TBD	TBD	2	2	2	2	2	2	tck
	ODT turn-on	t _{AON}	TBD	TBD	t _{AC(MIN)}	t _{AC(MAX)} +1000	t _{AC(MIN)}	t _{AC(MAX)} +1000	t _{AC(MIN)}	t _{AC(MAX)} +1000	ps
	ODT turn-off delay	t _{AOFD}	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	tck
	ODT turn-off	t _{AOF}	TBD	TBD	t _{AC(MIN)}	t _{AC(MAX)} +600	t _{AC(MIN)}	t _{AC(MAX)} +600	t _{AC(MIN)}	t _{AC(MAX)} +600	ps
	ODT turn-on (power-down mode)	t _{AONPD}	TBD	TBD	t _{AC(MIN)} +2000	2 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2 x t _{CK} + t _{AC(MAX)} +1000	ps
	ODT turn-off (power-down mode)	t _{AOFPD}	TBD	TBD	t _{AC(MIN)} +2000	2.5 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2.5 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2.5 x t _{CK} + t _{AC(MAX)} +1000	ps
	ODT to power-down entry latency	t _{ANPD}	TBD	TBD	3		3		3		tck
	ODT power-down exit latency	t _{AXPD}	TBD	TBD	8		8		8		tck
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t _{XARD}	TBD	TBD	2		2		2		tck
	Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}	TBD	TBD	7-AL		6-AL		6-AL		tck
	A Exit precharge power-down to any non-READ command.	t _{XP}	TBD	TBD	2		2		2		tck
	CKE minimum high/low time	t _{CKE}	TBD	TBD	3		3		3		tck

* AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.



ORDERING INFORMATION FOR D6

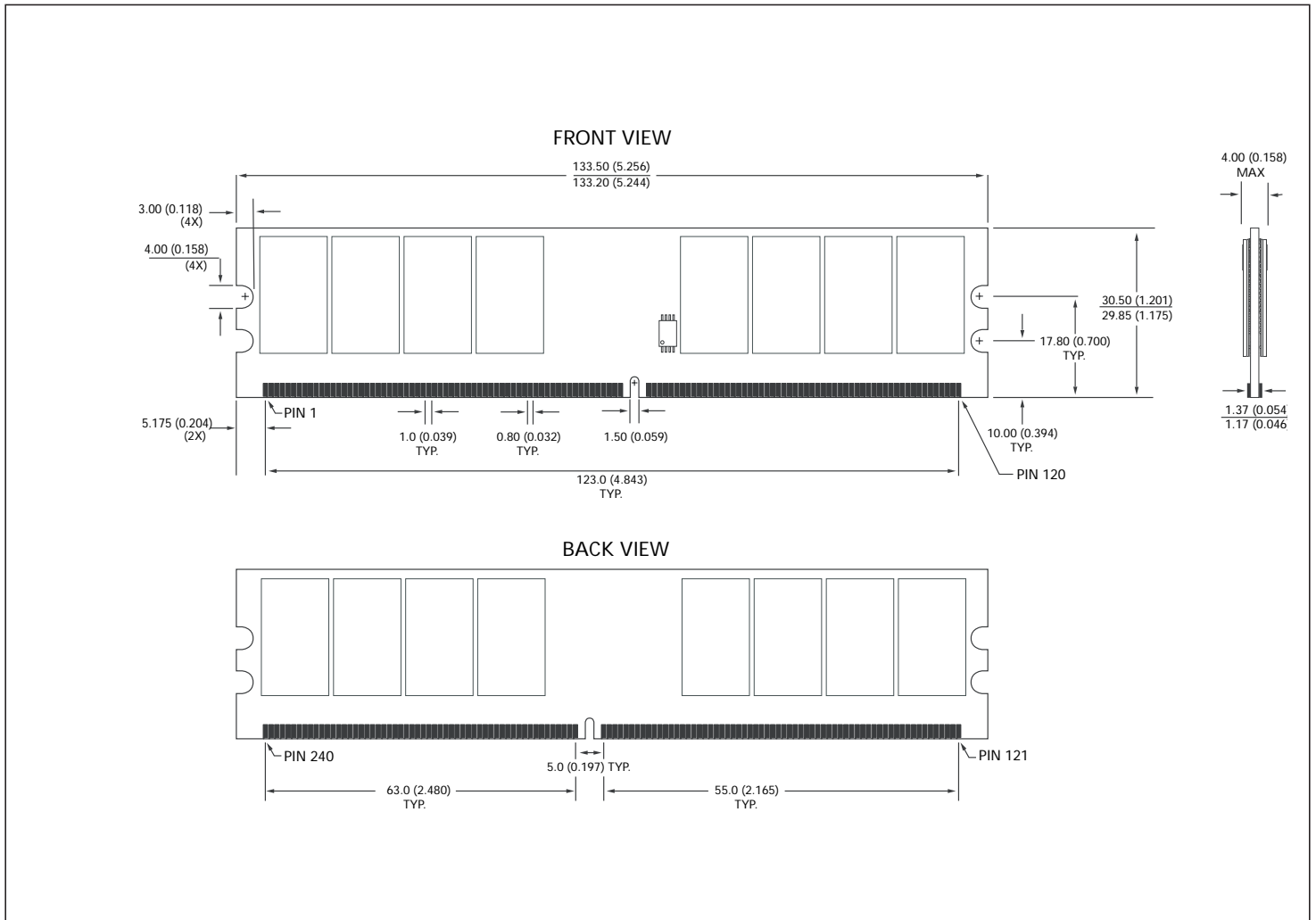
Part Number	Speed/Data Rate Frequency	CAS Latency	t _{RCD}	t _{RP}	Height**
WV3HG2128M64EEU806D6xxG*	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
WV3HG2128M64EEU665D6xxG*	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG2128M64EEU534D6xxG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG2128M64EEU403D6xxG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

* Contact factory for availability

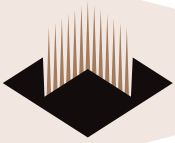
NOTES:

- RoHS compliant product. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

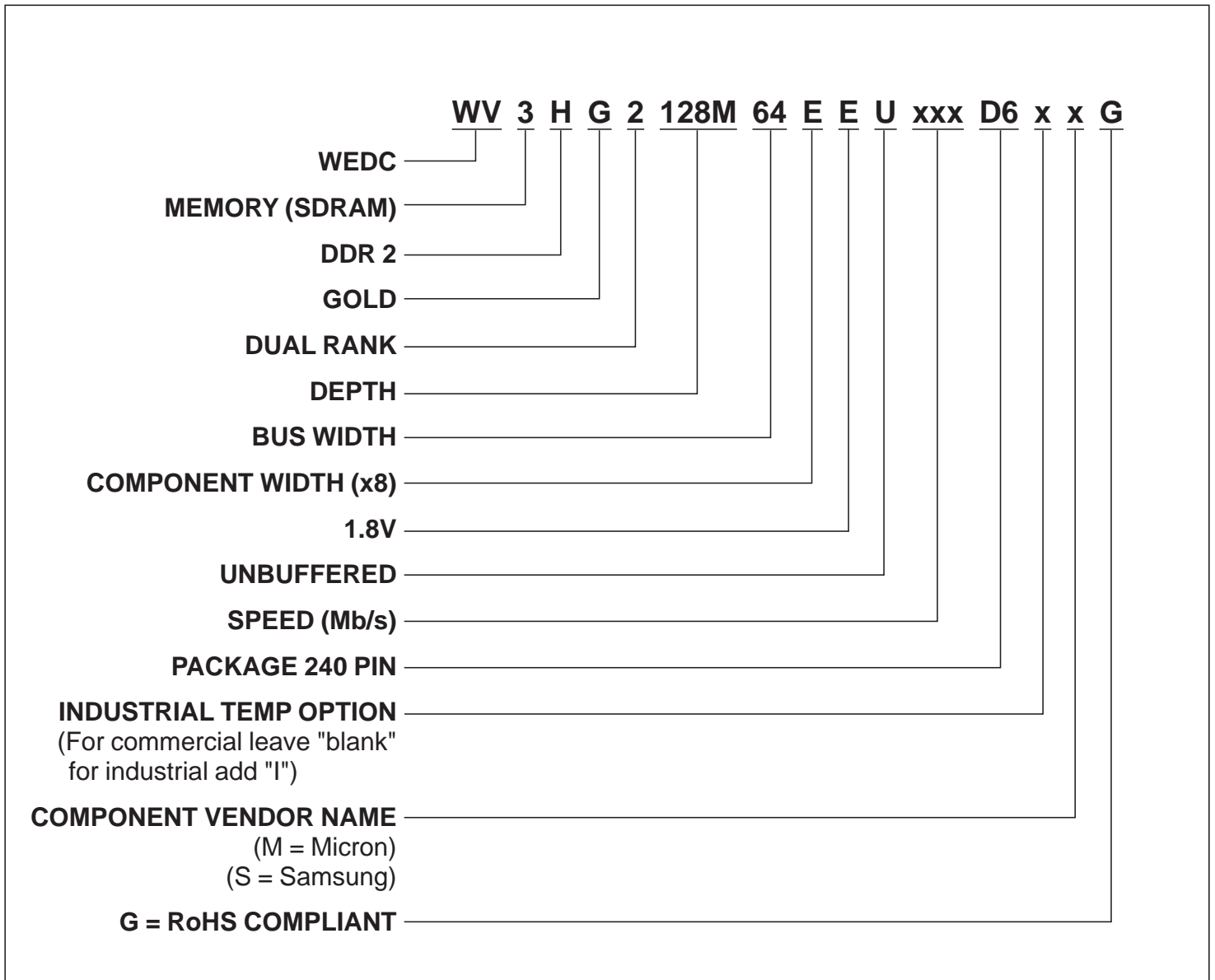
PACKAGE DIMENSIONS FOR D6

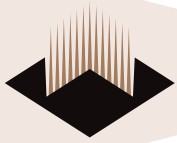


** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





Document Title

2GB – 2x128Mx64 DDR2 SDRAM UNBUFFERED

DRAM Die Options:

- SAMSUNG: B-Die
- MICRON: U28A: A-Die, move to U38Z: D-Die Q4'06 and U48B: E-Die Q2'07

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	June 2006	Concept
Rev 1	1.0 Engineering review	August 2006	Advanced
	1.1 Updated AC Specs		
	1.2 Moved from concept to advanced		
Rev 2	2.0 Updated AC title to indicate component AC specs only	October 2006	Advanced