

# OKI semiconductor

## MSM511002A

1,048,576-WORD x 1-BIT DYNAMIC RAM

### GENERAL DESCRIPTION

The MSM511002A is a new generation dynamic RAM organized as 1,048,576 words x 1 bit. The technology used to fabricate the MSM511002A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

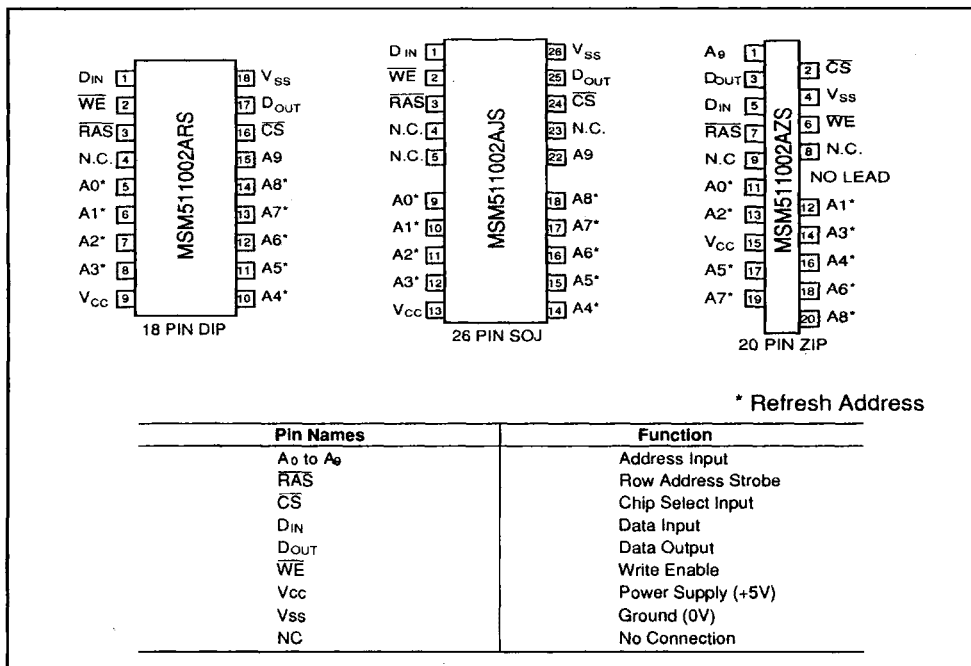
### FEATURES

- Silicon gate, triple polysilicon CMOS, 1-transistor memory cell
- Single +5V power supply,  $\pm 10\%$  tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using Early Write operation
- 1,048,576 words x 1 bit organization
- Static column mode, read/write capability
- $\overline{CS}$  before  $\overline{RAS}$  refresh, Hidden refresh,  $\overline{RAS}$ -only refresh capability
- Built-in  $V_{BB}$  generator circuit

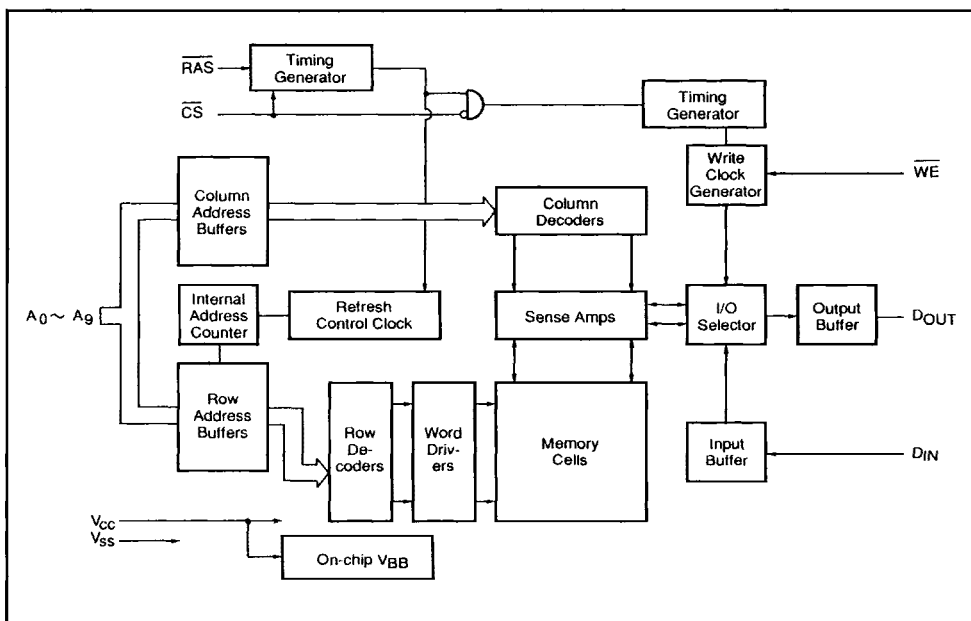
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| Family        | Access Time<br>(Max.) | Cycle Time<br>(Min.) | Power Dissipation |                |
|---------------|-----------------------|----------------------|-------------------|----------------|
|               |                       |                      | Operating (Max.)  | Standby (Max.) |
| MSM511002A-70 | 70ns                  | 140ns                | 468mW             | 5.5mW          |
| MSM511002A-80 | 80ns                  | 160ns                | 413mW             |                |
| MSM511002A-10 | 100ns                 | 190ns                | 358mW             |                |

## PIN CONFIGURATION (TOP VIEW)



## FUNCTIONAL BLOCK DIAGRAM



# **ELECTRICAL CHARACTERISTICS**

## **ABSOLUTE MAXIMUM RATINGS**

| Rating                                         | Symbol           | Conditions | Value        | Unit |
|------------------------------------------------|------------------|------------|--------------|------|
| Voltage on any pin relative to V <sub>SS</sub> | V <sub>T</sub>   | Ta = 25°C  | -1.0 to +7.0 | V    |
| Short circuit output current                   | I <sub>OS</sub>  | Ta = 25°C  | 50           | mA   |
| Power dissipation                              | P <sub>D</sub>   | Ta = 25°C  | 1            | W    |
| Operating temperature                          | T <sub>opr</sub> | —          | 0 to +70     | °C   |
| Storage temperature                            | T <sub>stg</sub> | —          | -55 to +150  | °C   |

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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## **RECOMMENDED OPERATING CONDITIONS**

(Ta = 0 ~ 70°C)

| Parameter          | Symbol          | Conditions | Value |      |      | Unit | Operating Temperature |
|--------------------|-----------------|------------|-------|------|------|------|-----------------------|
|                    |                 |            | Min.  | Typ. | Max. |      |                       |
| Supply voltage     | V <sub>CC</sub> | —          | 4.5   | 5.0  | 5.5  | V    | 0°C to +70°C          |
|                    | V <sub>SS</sub> | —          | 0     | 0    | 0    | V    |                       |
| Input high voltage | V <sub>IH</sub> | —          | 2.4   | —    | 6.5  | V    |                       |
| Input low voltage  | V <sub>IL</sub> | —          | -1.0  | —    | 0.8  | V    |                       |

**DC CHARACTERISTICS**
 $(V_{CC} = 5V \pm 10\%, T_a = 0 \text{ to } +70^\circ\text{C})$ 

| Parameter                                                   | Symbol           | Conditions                                                           | MSM<br>511002A-70 |                 | MSM<br>511002A-80 |                 | MSM<br>511002A-10 |                 | Unit | Notes |   |
|-------------------------------------------------------------|------------------|----------------------------------------------------------------------|-------------------|-----------------|-------------------|-----------------|-------------------|-----------------|------|-------|---|
|                                                             |                  |                                                                      | Min.              | Max.            | Min.              | Max.            | Min.              | Max.            |      |       |   |
| Output high voltage                                         | V <sub>OH</sub>  | I <sub>OH</sub> = -5.0mA                                             | 2.4               | V <sub>CC</sub> | 2.4               | V <sub>CC</sub> | 2.4               | V <sub>CC</sub> | V    | —     |   |
| Output low voltage                                          | V <sub>OL</sub>  | I <sub>OL</sub> = 4.2mA                                              | 0                 | 0.4             | 0                 | 0.4             | 0                 | 0.4             | V    | —     |   |
| Input leakage current                                       | I <sub>LI</sub>  | 0V ≤ V <sub>I</sub> ≤ 6.5V;<br>all other pins not<br>under test = 0V | -10               | 10              | -10               | 10              | -10               | 10              | μA   | —     |   |
| Output leakage current                                      | I <sub>LO</sub>  | DOUT disable<br>0V ≤ VO ≤ 5.5V                                       | -10               | 10              | -10               | 10              | -10               | 10              | μA   | —     |   |
| Average power supply<br>current* (Operating)                | I <sub>CC1</sub> | RAS, CS cycling,<br>t <sub>RC</sub> = min                            | —                 | 85              | —                 | 75              | —                 | 65              | mA   | —     |   |
| Power supply<br>current* (Standby)                          | I <sub>CC2</sub> | RAS=V <sub>IH</sub><br>CS=V <sub>IH</sub><br>DOUT=Hz                 | TTL               | —               | 2                 | —               | 2                 | —               | 2    | mA    | — |
|                                                             |                  | MOS                                                                  | —                 | 1               | —                 | 1               | —                 | 1               |      |       |   |
| Average power supply<br>current* (RAS-only refresh)         | I <sub>CC3</sub> | RAS cycling,<br>CS=V <sub>IH</sub><br>t <sub>RC</sub> =min           | —                 | 85              | —                 | 75              | —                 | 65              | mA   | —     |   |
| Average power supply<br>current* (CS before<br>RAS refresh) | I <sub>CC6</sub> | RAS cycling,<br>CS before RAS                                        | —                 | 85              | —                 | 75              | —                 | 65              | mA   | —     |   |
| Average power supply<br>current*<br>(Static column mode)    | I <sub>CC9</sub> | RAS=V <sub>IL</sub> ,<br>CS cycling<br>t <sub>SC</sub> =min          | —                 | 70              | —                 | 60              | —                 | 55              | mA   | —     |   |

\*  $I_{CC}$  depends on output loading and cycle rates. Specified values are obtained with the output open.

**CAPACITANCE**
 $(T_a = 25^\circ\text{C}, f = 1 \text{ MHz})$ 

| Parameter                                                                  | Symbol    | Conditions | Value |      | Unit |
|----------------------------------------------------------------------------|-----------|------------|-------|------|------|
|                                                                            |           |            | Min.  | Max. |      |
| Input capacitance ( $A_0$ to $A_9, D_{IN}$ )                               | $C_{IN1}$ | —          | —     | 6    | pF   |
| Input capacitance ( $\overline{RAS}$ , $\overline{CS}$ , $\overline{WE}$ ) | $C_{IN2}$ | —          | —     | 7    | pF   |
| Output capacitance ( $D_{OUT}$ )                                           | $C_{OUT}$ | —          | —     | 7    | pF   |

## AC CHARACTERISTICS

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to +70°C) Notes 1,2,3

| Parameter                                         | Symbol            | MSM 511002A-70 |         | MSM 511002A-80 |         | MSM 511002A-10 |         | Unit | Notes |
|---------------------------------------------------|-------------------|----------------|---------|----------------|---------|----------------|---------|------|-------|
|                                                   |                   | Min.           | Max.    | Min.           | Max.    | Min.           | Max.    |      |       |
| Refresh period                                    | t <sub>REF</sub>  | —              | 8       | —              | 8       | —              | 8       | ms   | —     |
| Random read or write cycle time                   | t <sub>RC</sub>   | 140            | —       | 160            | —       | 190            | —       | ns   | —     |
| Read/write cycle time                             | t <sub>RWC</sub>  | 165            | —       | 185            | —       | 220            | —       | ns   | —     |
| Static column mode cycle time                     | t <sub>SC</sub>   | 45             | —       | 50             | —       | 55             | —       | ns   | —     |
| Static column mode read/write cycle time          | t <sub>SRWC</sub> | 70             | —       | 80             | —       | 100            | —       | ns   | —     |
| Access time from RAS                              | t <sub>RAC</sub>  | —              | 70      | —              | 80      | —              | 100     | ns   | 4,5,6 |
| Access time from CS                               | t <sub>CAC</sub>  | —              | 20      | —              | 20      | —              | 25      | ns   | 4,5   |
| Access time from column address                   | t <sub>AA</sub>   | —              | 35      | —              | 40      | —              | 50      | ns   | 4,6,7 |
| Access time from last write                       | t <sub>ALW</sub>  | —              | 65      | —              | 75      | —              | 95      | ns   | 4,7   |
| Output low impedance time from CS                 | t <sub>CLZ</sub>  | 0              | —       | 0              | —       | 0              | —       | ns   | 4     |
| Data output hold time reference to column address | t <sub>AOH</sub>  | 5              | —       | 5              | —       | 5              | —       | ns   | —     |
| Data output enable time reference to WE           | t <sub>OW</sub>   | —              | 30      | —              | 30      | —              | 30      | ns   | —     |
| Output buffer turn-off delay time                 | t <sub>OFF</sub>  | 0              | 20      | 0              | 20      | 0              | 20      | ns   | —     |
| Transition time                                   | t <sub>T</sub>    | 3              | 50      | 3              | 50      | 3              | 50      | ns   | 3     |
| RAS precharge time                                | t <sub>RP</sub>   | 60             | —       | 70             | —       | 80             | —       | ns   | —     |
| RAS pulse width                                   | t <sub>RAS</sub>  | 70             | 10,000  | 80             | 10,000  | 100            | 10,000  | ns   | —     |
| RAS pulse width (Static column mode)              | t <sub>RASC</sub> | 70             | 100,000 | 80             | 100,000 | 100            | 100,000 | ns   | —     |
| RAS hold time                                     | t <sub>RSH</sub>  | 20             | —       | 20             | —       | 25             | —       | ns   | —     |
| CS precharge time                                 | t <sub>CP</sub>   | 10             | —       | 10             | —       | 10             | —       | ns   | —     |
| CS pulse width                                    | t <sub>CS</sub>   | 20             | 10,000  | 20             | 10,000  | 25             | 10,000  | ns   | —     |
| CS pulse width (Static column mode)               | t <sub>CSC</sub>  | 20             | 100,000 | 20             | 100,000 | 25             | 100,000 | ns   | —     |
| CS hold time                                      | t <sub>CSH</sub>  | 70             | —       | 80             | —       | 100            | —       | ns   | —     |
| RAS to CS delay time                              | t <sub>RCD</sub>  | 20             | 50      | 22             | 60      | 25             | 75      | ns   | 5     |
| RAS to column address delay time                  | t <sub>RAD</sub>  | 15             | 35      | 17             | 40      | 20             | 50      | ns   | 6     |
| CS to RAS precharge time                          | t <sub>CRP</sub>  | 10             | —       | 10             | —       | 10             | —       | ns   | —     |
| Row address set-up time                           | t <sub>ASR</sub>  | 0              | —       | 0              | —       | 0              | —       | ns   | —     |
| Row address hold time                             | t <sub>RAH</sub>  | 10             | —       | 12             | —       | 15             | —       | ns   | —     |
| Column address set-up time                        | t <sub>ASC</sub>  | 0              | —       | 0              | —       | 0              | —       | ns   | —     |
| Column address hold time                          | t <sub>CAH</sub>  | 15             | —       | 15             | —       | 20             | —       | ns   | —     |

AC CHARACTERISTICS (CONT.)

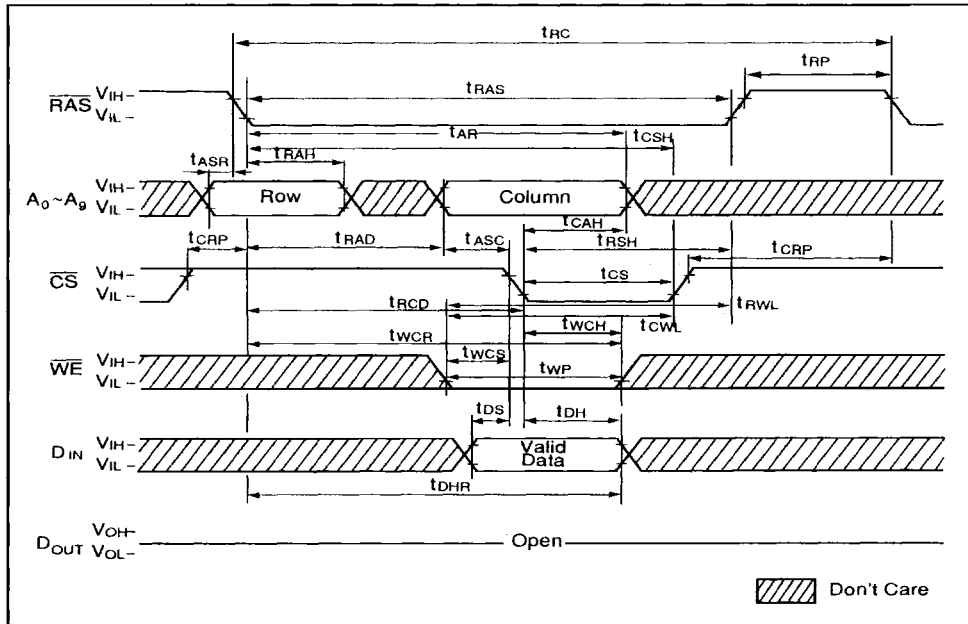
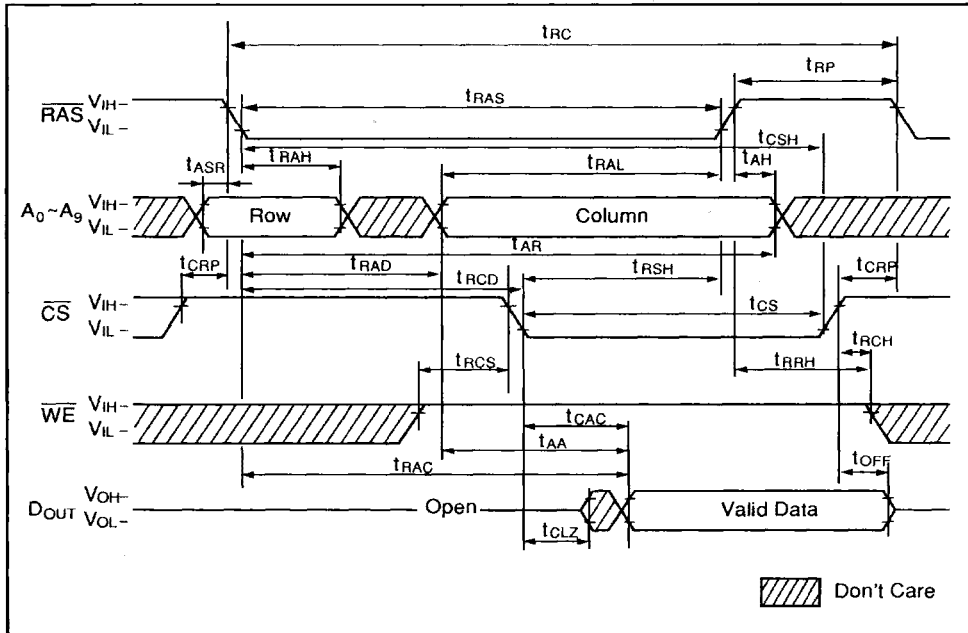
| Parameter                                                                         | Symbol            | MSM<br>511002A-<br>70 |      | MSM<br>511002A-<br>80 |      | MSM<br>511002A-<br>10 |      | Unit | Notes |
|-----------------------------------------------------------------------------------|-------------------|-----------------------|------|-----------------------|------|-----------------------|------|------|-------|
|                                                                                   |                   | Min.                  | Max. | Min.                  | Max. | Min.                  | Max. |      |       |
| Column address to $\overline{\text{RAS}}$<br>lead time                            | $t_{\text{RAL}}$  | 35                    | —    | 40                    | —    | 50                    | —    | ns   | —     |
| Column address hold time<br>reference to $\overline{\text{RAS}}$<br>(WRITE CYCLE) | $t_{\text{AWR}}$  | 55                    | —    | 60                    | —    | 75                    | —    | ns   | —     |
| Column address hold time<br>reference to $\overline{\text{RAS}}$                  | $t_{\text{AR}}$   | 85                    | —    | 95                    | —    | 115                   | —    | ns   | —     |
| Column address hold time<br>reference to $\overline{\text{RAS}}$ precharge        | $t_{\text{AH}}$   | 10                    | —    | 10                    | —    | 10                    | —    | ns   | —     |
| Column address hold time<br>reference to $\overline{\text{WE}}$                   | $t_{\text{AHLW}}$ | 65                    | —    | 75                    | —    | 95                    | —    | ns   | —     |
| Last write to column<br>address delay time                                        | $t_{\text{LWAD}}$ | 20                    | 30   | 20                    | 35   | 25                    | 45   | ns   | 7     |
| Read command set-up time                                                          | $t_{\text{RCS}}$  | 0                     | —    | 0                     | —    | 0                     | —    | ns   | —     |
| Read command hold time<br>reference to $\overline{\text{CS}}$                     | $t_{\text{RCH}}$  | 0                     | —    | 0                     | —    | 0                     | —    | ns   | 9     |
| Write command hold time<br>from $\overline{\text{RAS}}$                           | $t_{\text{WCR}}$  | 55                    | —    | 60                    | —    | 75                    | —    | ns   | —     |
| Write command set-up time                                                         | $t_{\text{WCS}}$  | 0                     | —    | 0                     | —    | 0                     | —    | ns   | 8     |
| Write command pulse width                                                         | $t_{\text{WP}}$   | 15                    | —    | 15                    | —    | 20                    | —    | ns   | —     |
| Write invalid time                                                                | $t_{\text{WI}}$   | 10                    | —    | 10                    | —    | 10                    | —    | ns   | —     |

## AC CHARACTERISTICS (CONT.)

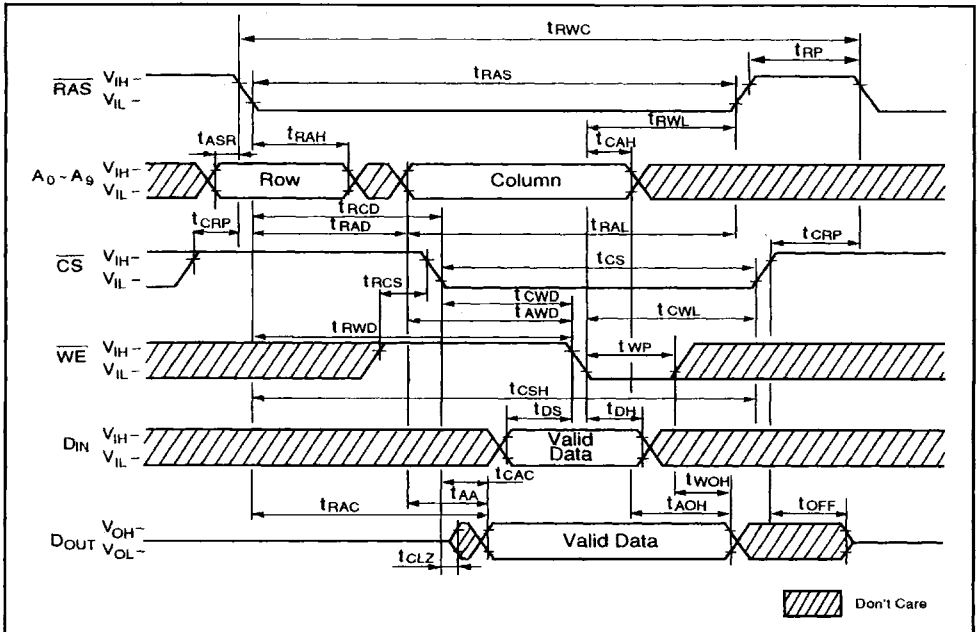
| Parameter                                   | Symbol     | MSM<br>511002A-<br>70 |      | MSM<br>511002A-<br>80 |      | MSM<br>511002A-<br>10 |      | Unit | Notes |
|---------------------------------------------|------------|-----------------------|------|-----------------------|------|-----------------------|------|------|-------|
|                                             |            | Min.                  | Max. | Min.                  | Max. | Min.                  | Max. |      |       |
| Write command hold time<br>(Dout disable)   | $t_{WCH}$  | 15                    | —    | 15                    | —    | 20                    | —    | ns   | —     |
| Data-in hold time from RAS                  | $t_{DHR}$  | 55                    | —    | 60                    | —    | 75                    | —    | ns   | —     |
| Data output hold time<br>reference to WE    | $t_{WOH}$  | 0                     | —    | 0                     | —    | 0                     | —    | ns   | —     |
| Write command to RAS<br>lead time           | $t_{RWL}$  | 20                    | —    | 20                    | —    | 25                    | —    | ns   | —     |
| Write command to CS<br>lead time            | $t_{CWL}$  | 20                    | —    | 20                    | —    | 25                    | —    | ns   | —     |
| Data-in set-up time                         | $t_{DS}$   | 0                     | —    | 0                     | —    | 0                     | —    | ns   | —     |
| Data-in hold time                           | $t_{DH}$   | 15                    | —    | 15                    | —    | 20                    | —    | ns   | —     |
| CS to WE delay time                         | $t_{CWD}$  | 20                    | —    | 20                    | —    | 25                    | —    | ns   | 8     |
| RAS to WE delay time                        | $t_{RWD}$  | 70                    | —    | 80                    | —    | 100                   | —    | ns   | 8     |
| Column address to WE<br>delay time          | $t_{AWD}$  | 35                    | —    | 40                    | —    | 50                    | —    | ns   | 8     |
| RAS to second WE delay time                 | $t_{RSWD}$ | 80                    | —    | 95                    | —    | 115                   | —    | ns   | —     |
| Read command hold time<br>reference to RAS  | $t_{RRH}$  | 0                     | —    | 10                    | —    | 10                    | —    | ns   | 9     |
| RAS to CS set-up time<br>(CS before RAS)    | $t_{CSR}$  | 10                    | —    | 10                    | —    | 10                    | —    | ns   | —     |
| RAS to CS hold time<br>(CS before RAS)      | $t_{CHR}$  | 30                    | —    | 30                    | —    | 30                    | —    | ns   | —     |
| CS active delay time from<br>RAS precharge  | $t_{RPC}$  | 10                    | —    | 10                    | —    | 10                    | —    | ns   | —     |
| CS precharge time<br>(Refresh counter test) | $t_{CPT}$  | 40                    | —    | 40                    | —    | 50                    | —    | ns   | —     |
| CS precharge time                           | $t_{CPN}$  | 10                    | —    | 10                    | —    | 15                    | —    | ns   | —     |

- Notes:
1. An initial pause of 100  $\mu$ s is required after power-up followed by a minimum of any 8 RAS cycles (example: RAS-only Refresh) before proper device operation is achieved.
  2. The AC measurements assume the transition time ( $t_T$ ) = 5 ns.
  3.  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. Measured using an equivalent load circuit of 2 TTL loads and 100pF.
  5. Operating within the  $t_{RCD}$  (max.) limit insures that  $t_{RAC}$  (max.) can be met. The spec.  $t_{RCD}$  (max.) is for reference only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max.) limit, the access time is controlled exclusively by  $t_{CAC}$ .
  6. Operating within the  $t_{RAD}$  (max.) limit insures that  $t_{RAC}$  (max.) can be met. The spec.  $t_{RAD}$  (max.) is for reference only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max.) limit, the access time is controlled exclusively by  $t_{AA}$ .
  7. Operating within the  $t_{LWAD}$  (max.) limit insures that  $t_{ALW}$  (max.) can be met. The spec.  $t_{LWAD}$  (max.) is for reference only. If  $t_{LWAD}$  is greater than the specified  $t_{LWAD}$  (max.) limit, the access time is controlled exclusively by  $t_{AA}$ .
  8. The specs  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet for reference only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$  the cycle is an Early Write cycle and data out remains in a high impedance state throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{RWD} \geq t_{RWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$  the cycle is a Read-Write cycle and the data out contains data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out is indeterminate at access time.
  9. Either the  $t_{RRH}$  or the  $t_{RCH}$  spec. must be satisfied for a proper read cycle.

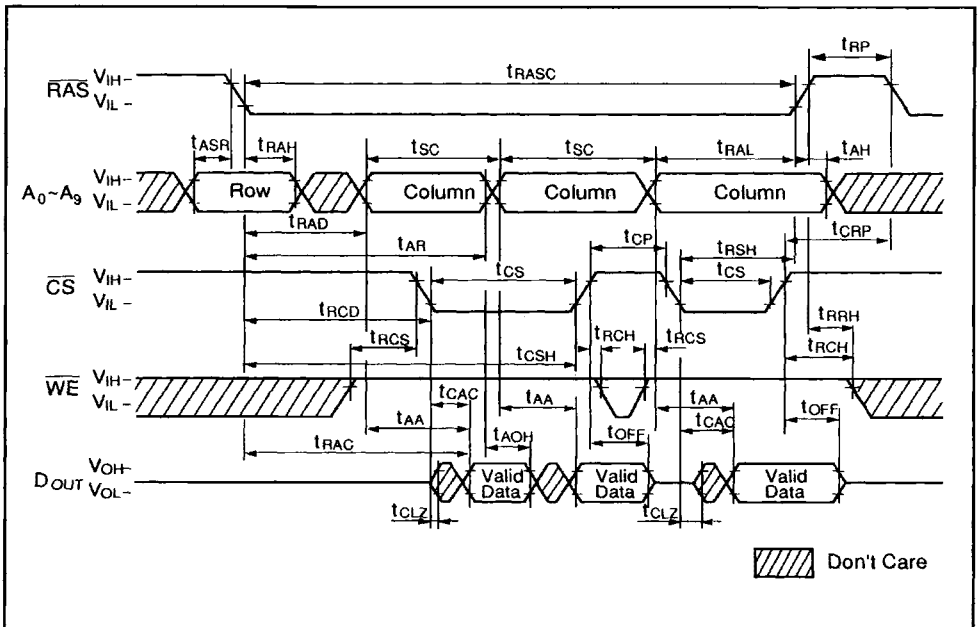




## READ/WRITE CYCLE

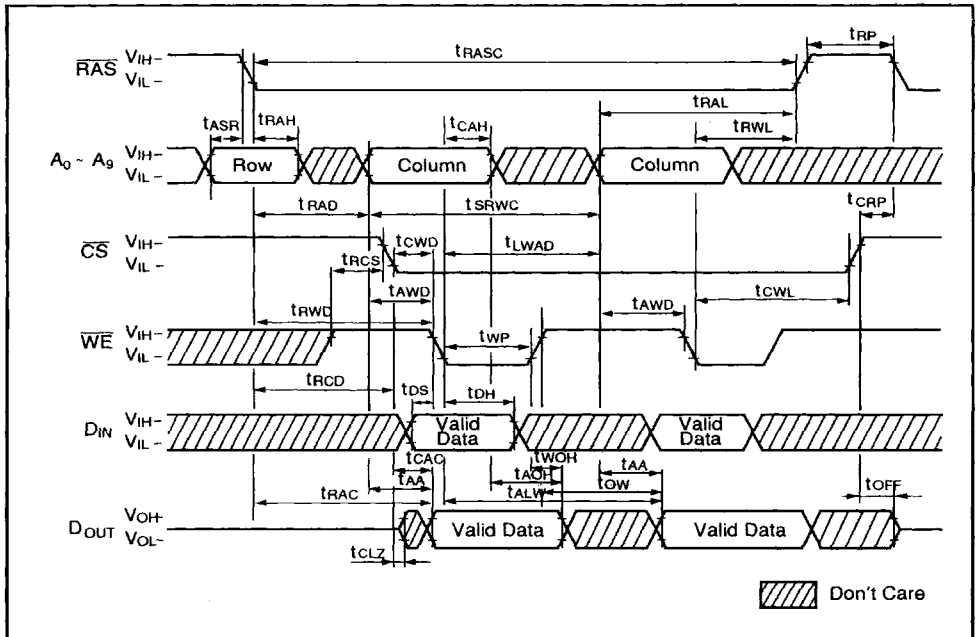


## STATIC COLUMN MODE READ CYCLE

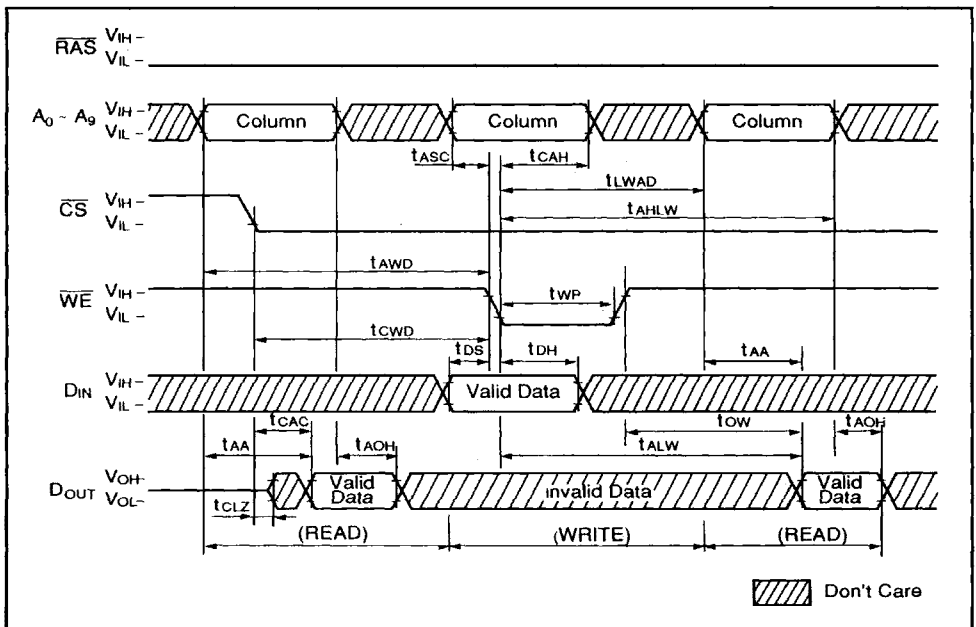




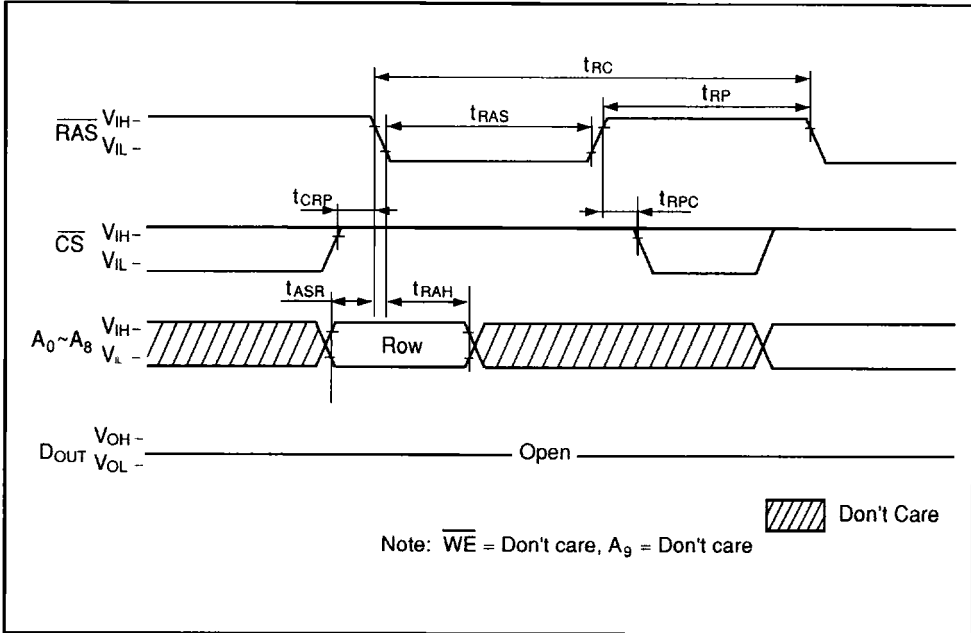
## STATIC COLUMN MODE READ/WRITE CYCLE



## STATIC COLUMN MODE READ/WRITE MIXED CYCLE

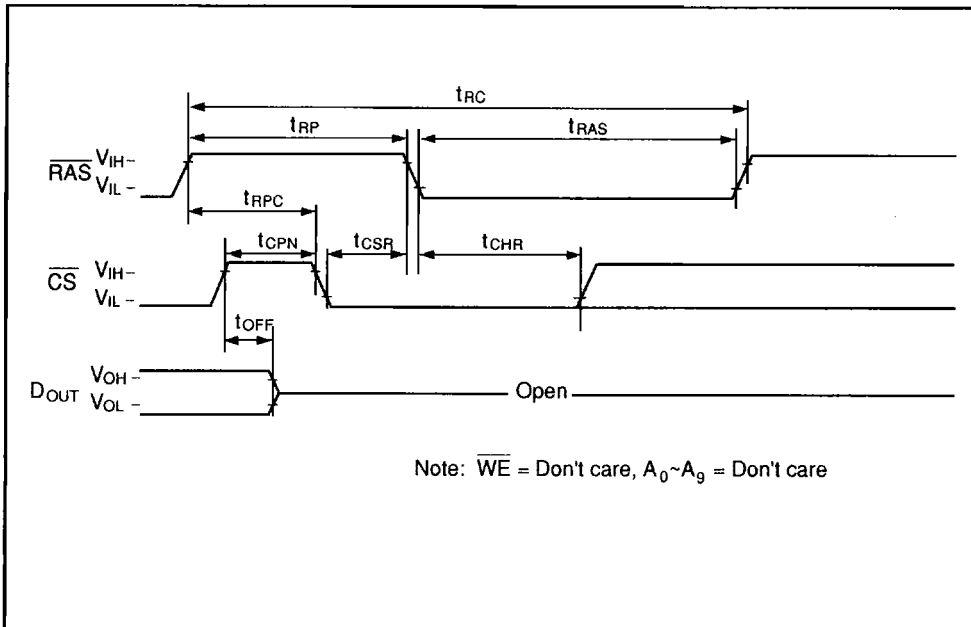


## RAS-ONLY REFRESH CYCLE

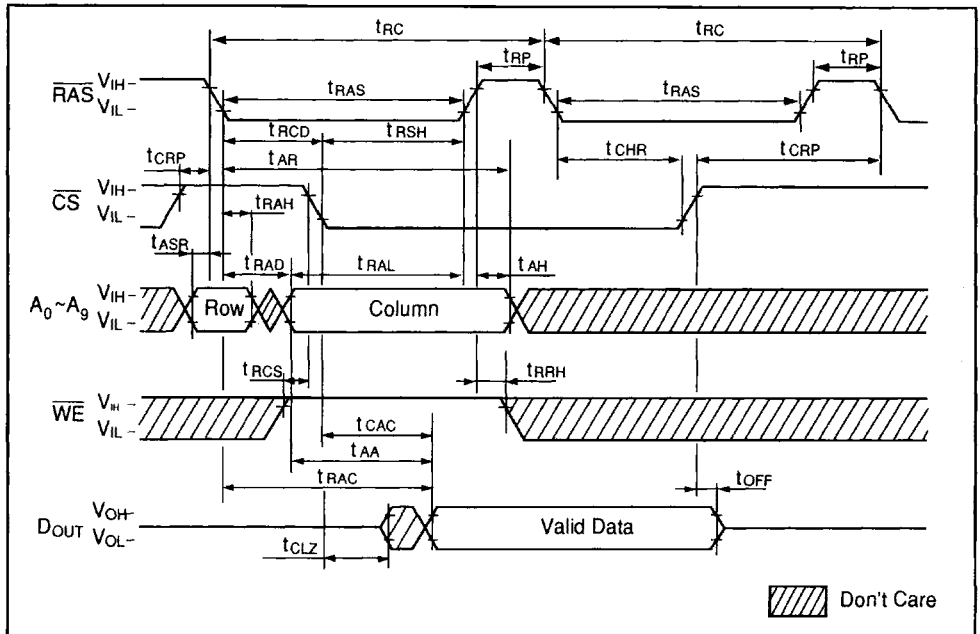


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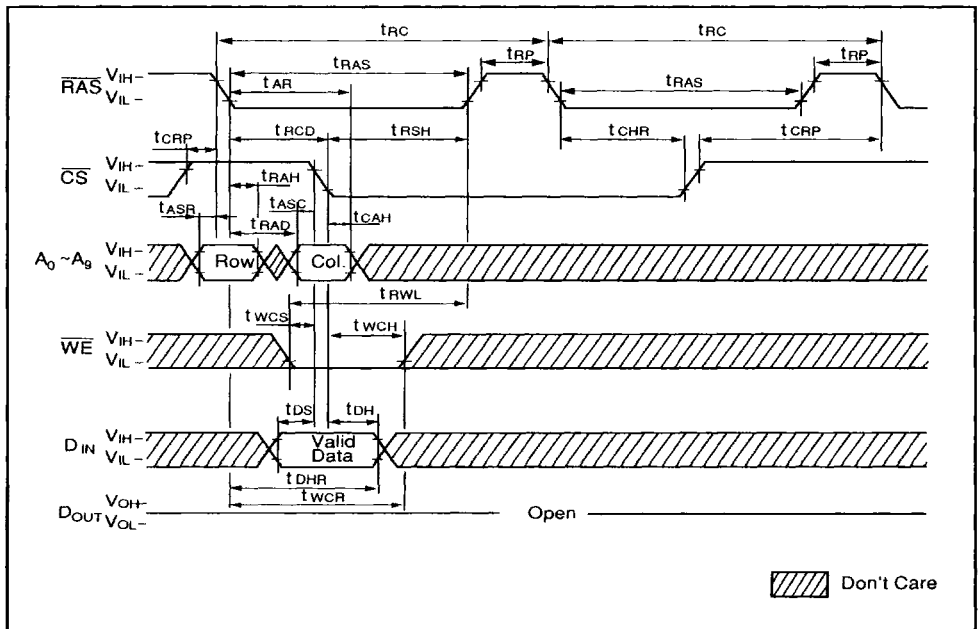
## CS BEFORE RAS AUTO-REFRESH CYCLE



## HIDDEN REFRESH READ CYCLE



## HIDDEN REFRESH WRITE CYCLE



# CS BEFORE RAS REFRESH COUNTER TEST

