VCXO

DIP TYPE

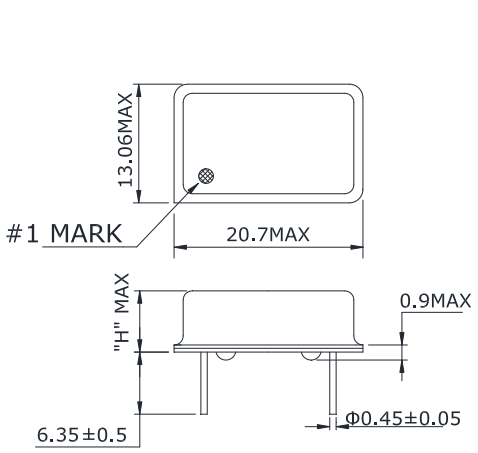
SVA(FULL)

- Voltage Controlled Crystal Oscillator
- 3.3V, 5.0V Supply Voltage
- CMOS Output
- Wide Frequency and Pull Range
- 14 Pin Dip Package

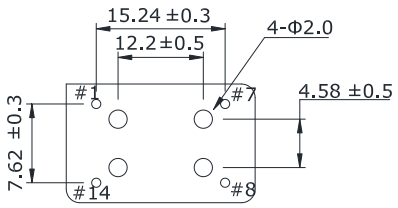
■ ELECTRICAL SPECIFICATIONS

ITEM	Value	Remarks
Output Logic Type	CMOS	CMOS VCXO
Frequency Range	1.000 to 80.000 MHz, 122.880 MHz	Fundamental
Supply Voltage(V_{DD})	3.3 V_{DC}, 5.0 V_{DC} ±5 %	
Operating Temperature Range	-20 to +70 ℃, -40 to +85 ℃	
Storage Temperature Range	-55 to +125 ℃	
Frequency Stability	±20 ppm, ±25 ppm, ±30 ppm, ±50 ppm, ±100 ppm Max.	Over operating temperature range
Input Current	10 mA Max. 20 mA(5V), 15 mA(3.3V, 2.5V) Max. 30 mA(5V), 25 mA(3.3V, 2.5V) Max. 40 mA(3.3V)	1.000 to 20.000 MHz 20.001 to 40.000 MHz 40.001 to 80.000 MHz 122.880 MHz
Output Voltage Logic High(V_{OH})	90 % of V_{DD} Min.	
Output Voltage Logic Low(V_{OL})	10 % of V_{DD} Max.	
Rise / Fall Time	10 ns Max.(1.000 to 20.000 MHz) 8 ns Max.(20.001 to 40.000 MHz) 5 ns Max.(40.001 to 80.000 MHz) 2.5 ns Max.(122.880 MHz)	Measured over 10 % to 90 % of waveform
Duty Cycle	45 to 55 %, 40 to 60 %	Measured at 50 % of waveform
Start-up Time	10 ms Max.	
Output Load Condition(CMOS)	15 pF Max.	
Frequency Deviation	±50 ppm, ±80 ppm, ±100 ppm Min.	Over Vc range
Control Voltage(Vc)	2.5 V ±2.0 V, 1.65 V ±1.35 V, 1.25 V ±1.05 V	Please specify
Linearity	10 % Max.	
Output Enable Function (V_{IH} and V_{IL})	70 % of V_{DD} Min. to Enable Output 30 % of V_{DD} Max. to Disable Output	High Impedance
RMS Phase Jitter	1 ps Max.	BW : 12 kHz to 20 MHz
Frequency Aging	±3 ppm Max.	25℃, First year

■ MECHANICAL DIMENSIONS (mm)



"H" SIZE
5.1 Max
7.5 Max



CONNECTION
#1 : V.C
#7 : GND
#8 : OUTPUT
#14 : VDD

■ PART NUMBERING GUIDE

SVA 3 15 A D B T F – 27.000M

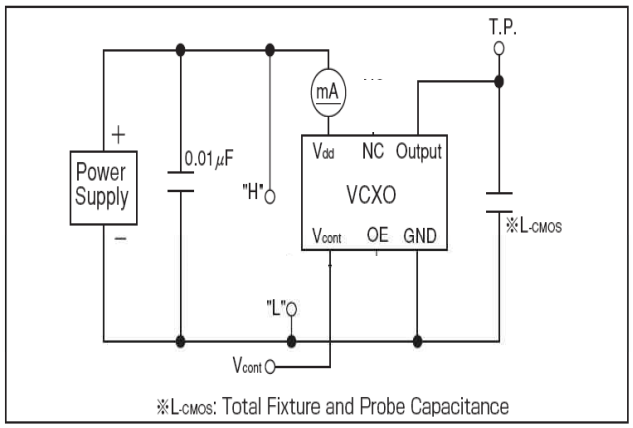
- **SUPPLY VOLTAGE(V_{DD})** 3 : 3.3 V, 2 : 2.5 V
- **FRQUENCY STABILITY** TABLE 1
- **OPERATING TEMPERAURE RANGE** TABLE 1
- **DUTY CYCLE** D : 45/55, E : 40/60
- **DEVIATION** A : ±30 ppm min. B : ±50 ppm min. C : ±80 ppm min. D : ±100 ppm min. E : ±130 ppm min. F : ±150 ppm min.
- **FREQUENCY** M : MHz
- **PACKAGE OPTION** H : HALF SIZE F : FULL SIZE
- **OUTPUT** T : TTL M : HCMOS C : COMPATIBLE

■ TABLE 1

FREQUENCY STABILITY VS. TEMPERATURE RANGE

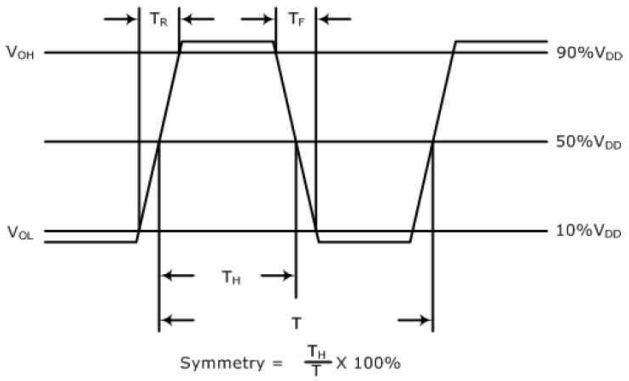
Temp \ Stability		±15	±20	±25	±30	±50	±100
		15	20	25	30	50	100
0~50 ℃	A	*	*	*	*	*	*
0~60 ℃	B		*	*	*	*	*
-10~60 ℃	C		*	*	*	*	*
0~70 ℃	D		*	*	*	*	*
-10~70 ℃	E		*	*	*	*	*
-20~70 ℃	F		*	*	*	*	*
-40~85 ℃	G			*	*	*	*

■ TEST CIRCUIT (CMOS)



※L-CMOS: Total Fixture and Probe Capacitance

■ WAVEFORM (CMOS)

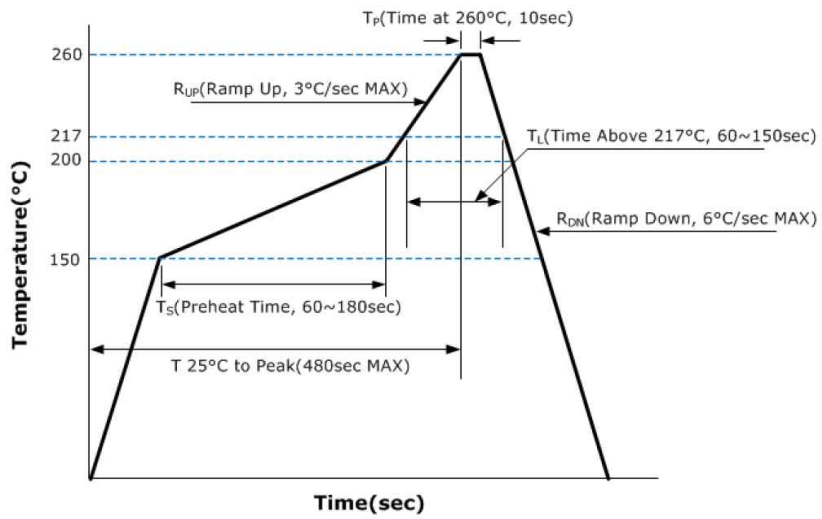


Symmetry = $\frac{T_H}{T}$ X 100%

■ ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-202, Method 213, Condition C
Vibration	MIL-STD-883, Method 2007, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Solderability	MIL-STD-883, Method 2003

■ REFLOW PROFILE



■ MARKING GUIDE

Frequency in MHz

Model Name

LINE 1 : SVA25DDM

LINE 2 : XX.XXX (3)

LINE 3 : YY MM

LINE 4 : ● SUNNY

Year

Month

Supply Voltage