

High Performance 128K×8 CMOS SRAM



128K×8 CMOS SRAM

AS7C1024
AS7C31024

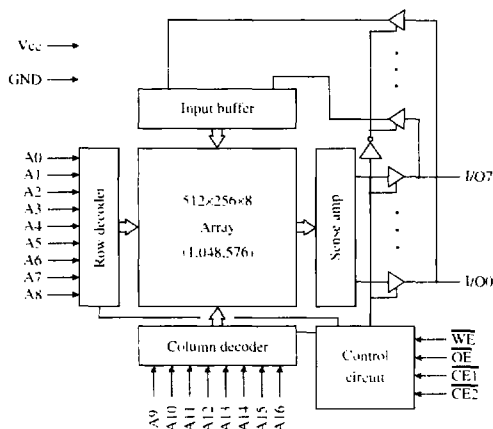
Features

- Organization: 131,072 words × 8 bits
- High speed
 - 10/12/15/20/25 ns address access time
 - 3/3/4/5/6 ns output enable access time
- Low power consumption
 - Active: 770 mW max (10 ns cycle)
 - Standby: 55 mW max, CMOS I/O
 - Very low DC component in active power
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$ inputs

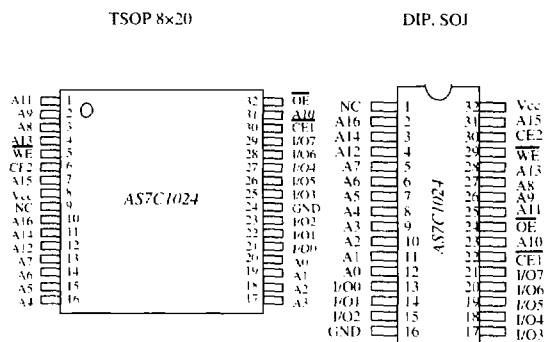
- TTL/LVTTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
 - 300 mil PDIP and SOJ
 - Socket compatible with 7C512
 - 400 mil PDIP and SOJ
 - 8×20 TSOP
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- 3.3V version available (AS7C31024)

SRAM

Logic block diagram



Pin arrangement



Selection guide

	7C1024-10	7C1024-12	7C1024-15	7C1024-20	7C1024-25	Unit
	-	7C31024-12	7C31024-15	7C31024-20	7C31024-25	
Maximum address access time					25	ns
Maximum output enable access time					6	ns
Maximum operating current					100	mA
					60	mA
Maximum CMOS standby current					10.0	mA

Shaded areas contain advance information



Functional description

The AS7C1024 and AS7C31024 are high performance CMOS 1,048,576-bit Static Random Access Memories (SRAM) organized as 131,072 words × 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 10/12/15/20/25 ns with output enable access times (t_{OE}) of 3/3/4/5/6 ns are ideal for high performance applications. Active-high and low chip enables ($\overline{CE1}$, $\overline{CE2}$) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE1}$ is HIGH or $\overline{CE2}$ is LOW the device enters standby mode. The standard AS7C1024 is guaranteed not to exceed 55 mW power consumption in standby mode. Both devices offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, $\overline{CE2}$). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or $\overline{CE2}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, $\overline{CE2}$), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL/LVTTL-compatible, and operation is from a single 5V supply (AS7C1024) or 3.3V supply (AS7C31024). The AS7C1024 and AS7C31024 are packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any pin relative to GND	V_I	-0.5	+7.0	V
Power dissipation	P_D	—	1.0	W
Storage temperature (plastic)	T_{stg}	-55	+150	°C
Temperature under bias	T_{bias}	-10	+85	°C
DC output current	I_{out}	—	20	mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB} , I_{SB1})
X	L	X	X	High Z	Standby (I_{SB} , I_{SB1})
L	H	H	H	High Z	Output disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage	AS7C1024	V_{CC}	4.5	5.0	5.5	V
	AS7C31024	V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
Input voltage	AS7C1024	V_{IH}	2.2	—	$V_{CC} + 0.5$	V
	AS7C31024	V_{IH}	2.0	—	$V_{CC} + 0.5$	V
		V_{IL}	-0.5	—	0.8	V

[†] V_{IH} min = -3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics ¹

Parameter	Symbol	Test conditions	-10		-12		-15		-20		-25		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$ I_{II} $	$V_{CC} = \text{Max},$ $V_{in} = \text{GND to } V_{CC}$											μA
Output leakage current	$ I_{LO} $	$\overline{\text{CE1}} = V_{IH} \text{ or } \text{CE2} = V_{IL},$ $V_{CC} = \text{Max},$ $V_{out} = \text{GND to } V_{CC}$											μA
Operating power supply current	I_{CC}	$\overline{\text{CE1}} = V_{IL}, \text{CE2} = V_{IH},$ $f = f_{\text{max}}, I_{out} = 0 \text{ mA}$											AS7C1024 mA
													AS7C31024 mA
Standby power supply current	I_{SB}	$\overline{\text{CE1}} = V_{IH} \text{ or } \text{CE2} = V_{IL},$ $f = f_{\text{max}}$											mA
		$\overline{\text{CE1}} \geq V_{CC} - 0.2 \text{ V or } \text{CE2} \leq 0.2 \text{ V},$ $V_{in} \leq 0.2 \text{ V or } V_{in} \geq V_{CC} - 0.2 \text{ V},$ $f = 0$											mA
Output voltage	V_{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$											V
	V_{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$											V

Shaded areas contain advance information

Capacitance ²(f = 1 MHz, T_a = Room temperature, V_{CC} = 5V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	A, $\overline{\text{CE1}}$, CE2, $\overline{\text{WE}}$, $\overline{\text{OE}}$	V _{in} = 0V	5	pF
I/O capacitance	C _{I/O}	I/O	V _{in} = V _{out} = 0V	7	pF

Read cycle ^{3,9,12}

Parameter	Symbol	-10		-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	15	—	20	—	25	—	25	—	25	—	ns	
Address access time	t _{AA}	—	15	—	20	—	25	—	25	—	25	ns	3
Chip enable ($\overline{\text{CE1}}$) access time	t _{ACE1}	—	15	—	20	—	25	—	25	—	25	ns	3, 12
Chip enable (CE2) access time	t _{ACE2}	—	15	—	20	—	25	—	25	—	25	ns	3, 12
Output enable ($\overline{\text{OE}}$) access time	t _{OE}	—	4	—	5	—	6	—	6	—	6	ns	
Output hold from address change	t _{OH}	3	—	3	—	3	—	3	—	3	—	ns	5
$\overline{\text{CE1}}$ LOW to output in Low Z	t _{CLZ1}	3	—	3	—	3	—	3	—	3	—	ns	4, 5, 12
CE2 HIGH to output in Low Z	t _{CLZ2}	3	—	3	—	3	—	3	—	3	—	ns	4, 5, 12
$\overline{\text{CE1}}$ HIGH to output in High Z	t _{CHZ1}	—	4	—	5	—	6	—	6	—	6	ns	4, 5, 12
CE2 LOW to output in High Z	t _{CHZ2}	—	4	—	5	—	6	—	6	—	6	ns	4, 5, 12
$\overline{\text{OE}}$ LOW to output in Low Z	t _{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	4, 5
$\overline{\text{OE}}$ HIGH to output in High Z	t _{OHZ}	—	4	—	5	—	6	—	6	—	6	ns	4, 5
Power up time	t _{PU}	0	—	0	—	0	—	0	—	0	—	ns	4, 5, 12
Power down time	t _{PD}	—	15	—	20	—	25	—	25	—	25	ns	4, 5, 12



Key to switching waveforms

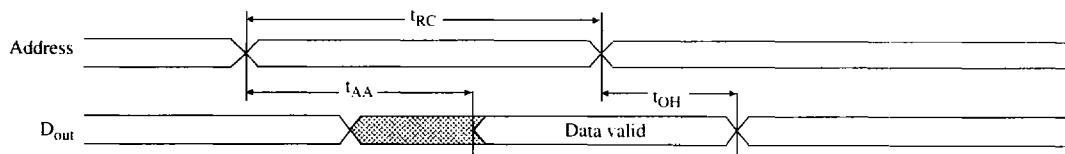
Rising input

Falling input

Undefined output/don't care

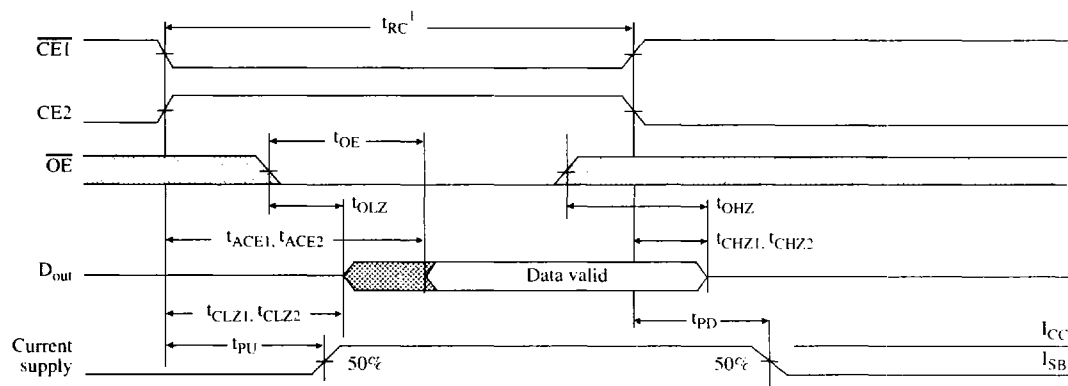
Read waveform 1 3,6,7,9,12

Address controlled



Read waveform 2 3,6,8,9,12

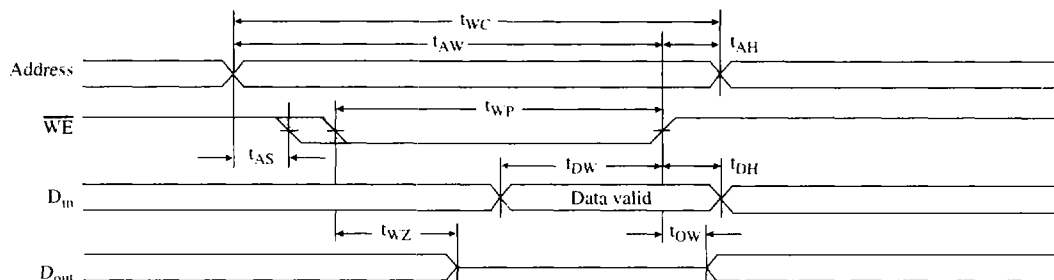
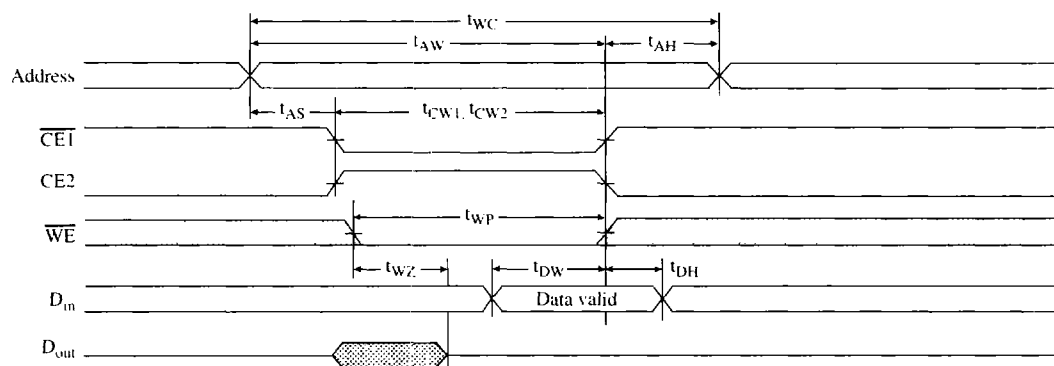
$\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ controlled



Write cycle 11, 12

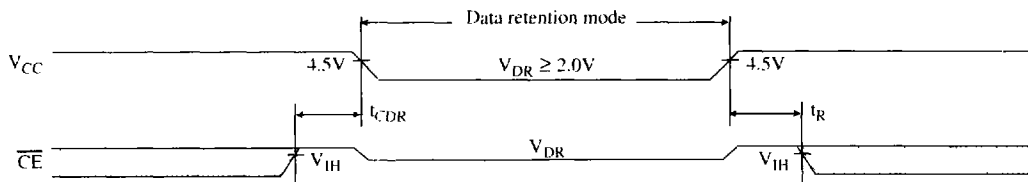
Parameter	Symbol	-10		-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	15	—	20	—	20	—	20	—	20	—	ns	
Chip enable ($\overline{\text{CE1}}$) to write end	t_{CW1}	12	—	12	—	15	—	15	—	15	—	ns	12
Chip enable ($\overline{\text{CE2}}$) to write end	t_{CW2}	12	—	12	—	15	—	15	—	15	—	ns	12
Address setup to write end	t_{AW}	12	—	12	—	15	—	15	—	15	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	12
Write pulse width	t_{WP}	9	—	12	—	15	—	15	—	15	—	ns	
Address hold from end of write	t_{AH}	0	—	0	—	0	—	0	—	0	—	ns	
Data valid to write end	t_{DW}	9	—	10	—	10	—	10	—	10	—	ns	
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	4, 5
Write enable to output in High Z	t_{WZ}	—	5	—	5	—	5	—	5	—	5	ns	4, 5
Output active from write end	t_{OW}	3	—	3	—	3	—	3	—	3	—	ns	4, 5

Shaded areas contain advance information.


Write waveform 1 ^{10,11,12}
 $\overline{\text{WE}}$ controlled

Write waveform 2 ^{10,11,12}
 $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ controlled

Data retention characteristics ¹³

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	$V_{CC} = 2.0V$	2.0	—	V
Data retention current	I_{CCDR}	$\overline{\text{CE1}} \geq V_{CC} - 0.2V$ or $\text{CE2} \leq 0.2V$	—	500	μA
Chip deselect to data retention time	t_{CDDR}		0	—	ns
Operation recovery time	t_R	$V_{in} \geq V_{CC} - 0.2V$ or $V_{in} \leq 0.2V$	t_{RC}	—	ns
Input leakage current	$ I_{LI} $		—	1	μA

Data retention waveform





AC test conditions

- 5V output load: see Figure B, except as noted see Figure C.
- 3.3V output load: see Figure D, except as noted see Figure E.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

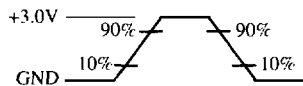


Figure A: Input waveform

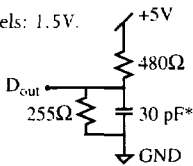


Figure B: Output load

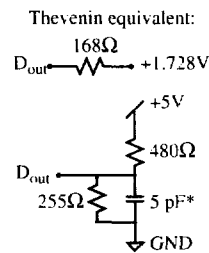


Figure C: Output load for t_{CLZ} , t_{CHZ} , t_{OLZ} , t_{OHZ} , t_{OW}

*including scope and jig capacitance

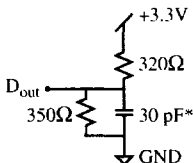


Figure D: Output load

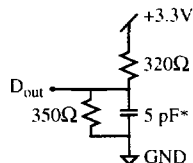


Figure C: Output load for t_{CLZ} , t_{CHZ} , t_{OLZ} , t_{OHZ} , t_{OW}

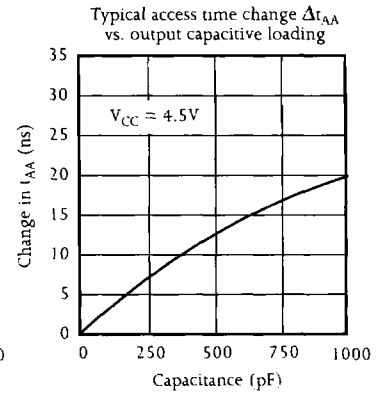
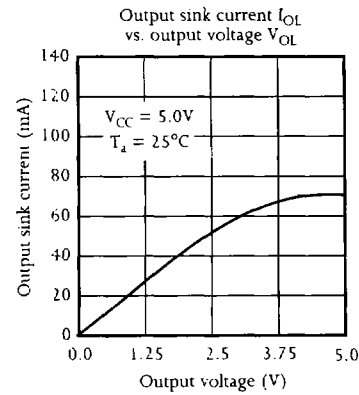
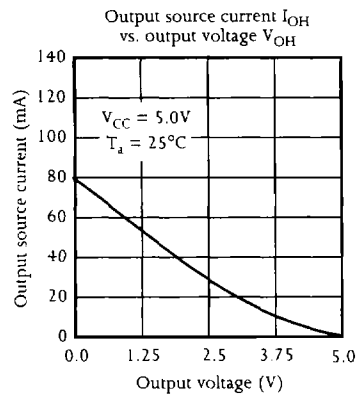
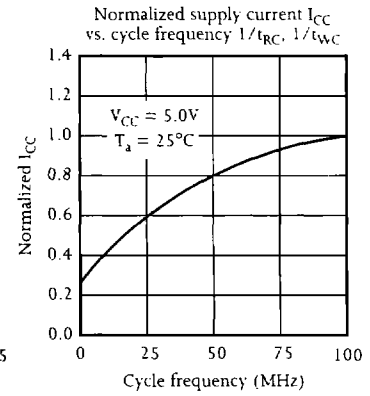
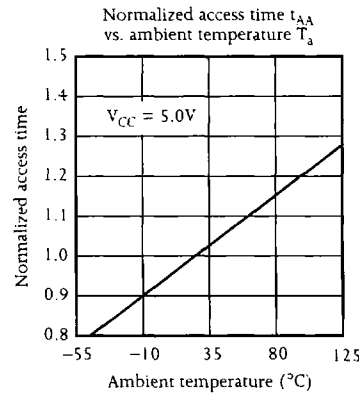
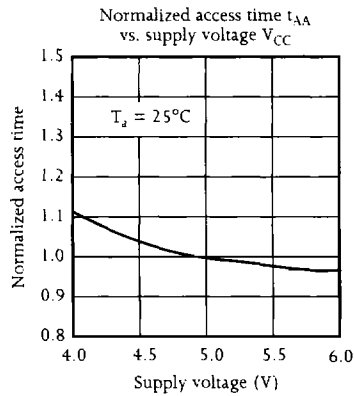
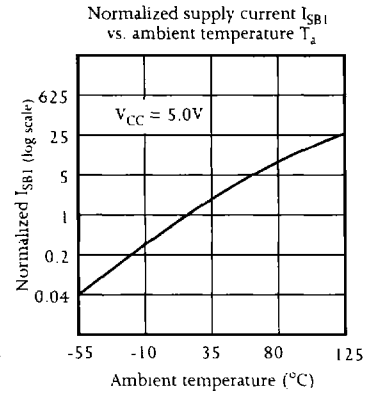
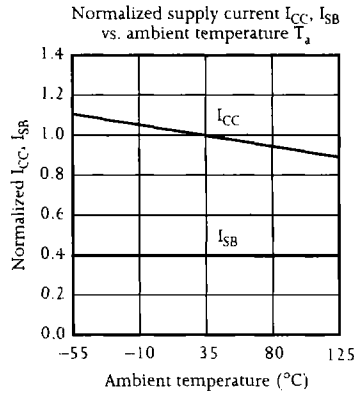
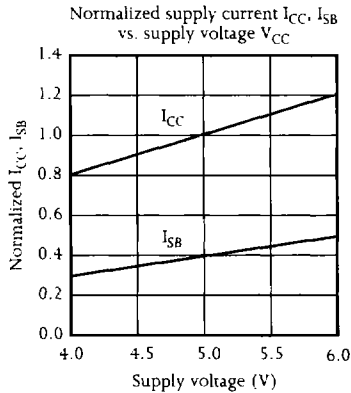
*including scope and jig capacitance

Notes

- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{EB} specification
- 2 This parameter is sampled and not 100% tested
- 3 For test conditions, see AC Test Conditions, Figures A, B, C.
- 4 t_{CLZ} and t_{CHZ} are specified with $C_L = 5\text{ pF}$ as in Figure C. Transition is measured $\pm 50\text{ mV}$ from steady-state voltage.
- 5 This parameter is guaranteed but not tested.
- 6 $\overline{WE}$ is HIGH for read cycle.
- 7 $\overline{CE1}$ and $\overline{OE}$ are LOW and $CE2$ is HIGH for read cycle
- 8 Address valid prior to or coincident with $\overline{CE}$ transition LOW
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 $\overline{CE1}$ or $\overline{WE}$ must be HIGH or $CE2$ LOW during address transitions
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address
- 12 $\overline{CE1}$ and $CE2$ have identical timing
- 13 This data applicable to the AS7C1024. The AS7C31024 functions similarly



Typical DC and AC characteristics



AS7C1024
AS7C31024



AS7C1024 ordering codes

Package \ Access time	10 ns	12 ns	15 ns	20 ns	25 ns
Plastic DIP, 300 mil			AS7C1024-15TPC	AS7C1024-20TPC	AS7C1024-25TPC
			AS7C31024-15TPC	AS7C31024-20TPC	AS7C31024-25TPC
Plastic DIP, 400 mil			AS7C1024-15PC	AS7C1024-20PC	AS7C1024-25PC
			AS7C31024-15PC	AS7C31024-20PC	AS7C31024-25PC
Plastic SOJ, 300 mil			AS7C1024-15TJC	AS7C1024-20TJC	AS7C1024-25TJC
			AS7C31024-15TJC	AS7C31024-20TJC	AS7C31024-25TJC
Plastic SOJ, 400 mil			AS7C1024-15JC	AS7C1024-20JC	AS7C1024-25JC
			AS7C31024-15JC	AS7C31024-20JC	AS7C31024-25JC
TSOP 8×20			AS7C1024-15TC	AS7C1024-20TC	AS7C1024-25TC
			AS7C31024-15TC	AS7C31024-20TC	AS7C31024-25TC

Shaded areas contain advance information

AS7C1024 part numbering system

AS7C	X	1024	-XX	X	C
SRAM prefix	Blank = 5V CMOS 3 = 3.3V CMOS	Device number	Access time	Package: TP = PDIP 300 mil P = TJ = SOJ 300 mil J = T = TSOP 8×20	Commercial temperature range, 0°C to 70 °C