T-46-23-10

Order this data sheet by MCM6208-35/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM6208-35, -45
MCM6209-35, -45

64K × 4 Bit Static RAMs

The MCM6208 and MCM6209 are 262,144 bit static random access memories organized as 65,536 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

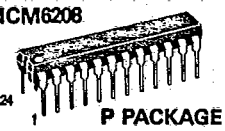
The MCM6209 has both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing greater system flexibility. Either input, when high, will force the outputs to high impedance.

- Single 5 V ±10% Power Supply
- Fast Access Time (Maximum):

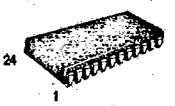
(xx = 08 or 09)	Address	Chip Enable	MCM6209 Output Enable
MCM62xx-35	35 ns	35 ns	15 ns
MCM62xx-45	45 ns	45 ns	17 ns

- Equal Address and Chip Enable Access Time
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems (MCM6209)
- Fully TTL Compatible—Three-State Data Output

MCM6208

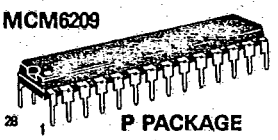


P PACKAGE
300 MIL PLASTIC
CASE 724A



J PACKAGE
300 MIL SOJ
CASE 810A

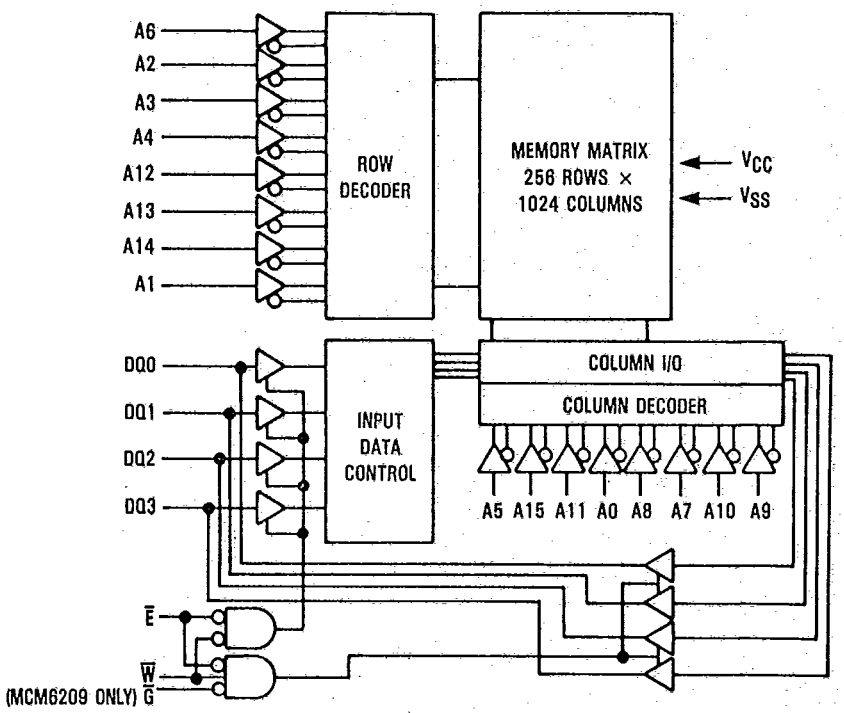
MCM6209



P PACKAGE
300 MIL PLASTIC
CASE 710B

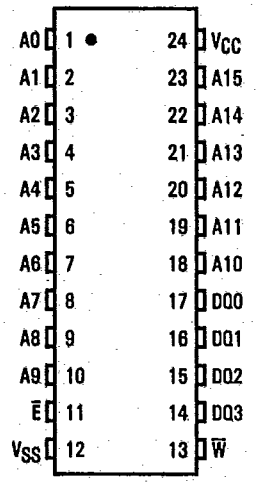
J PACKAGE
300 MIL SOJ
CASE 810B

BLOCK DIAGRAM

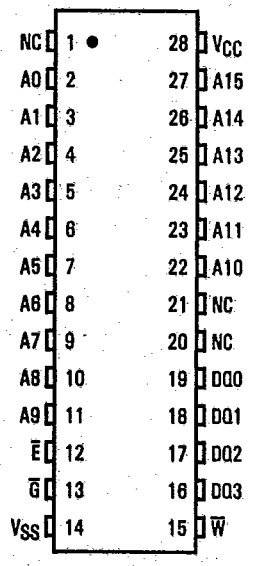


PIN ASSIGNMENT

MCM6208



MCM6209



PIN NAMES	
A0-A15 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3. . Data Input/Output	NC . . . . . No Connection
$\overline{W}$. . . . . Write Enable	V_{CC}. . . . +5 V Power Supply
$\overline{G}$ (MCM6209) . . Output Enable	V_{SS}. . . . . Ground

MOTOROLA

DS9941

MCM6208 TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6209 TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −2.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	—	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	—	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	t_{AVAV}=35 ns	I_{CCA}	—	—	130	mA
	t_{AVAV}=45 ns		—	—	130	
AC Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	—	35	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	—	10	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH}= −4.0 mA)		V_{OH}	2.4	—	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
I/O Capacitance	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

T-46-23-10

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

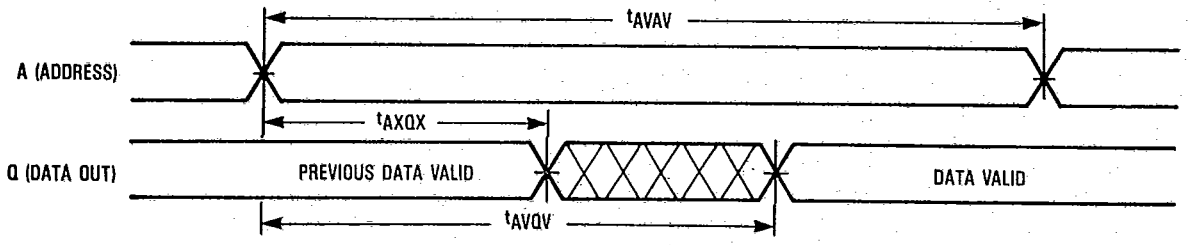
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

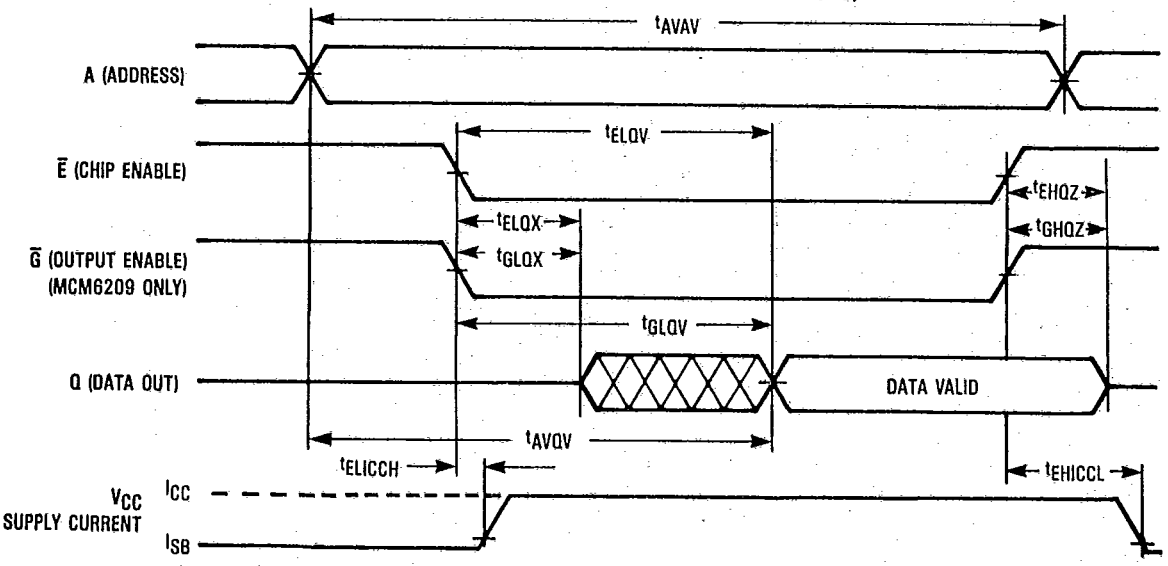
Parameter		Symbol		MCM6208-35 MCM6209-35		MCM6208-45 MCM6209-45		Units	Notes
		Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time		t_{AVAV}	t_{RC}	35	—	45	—	ns	2
Address Access Time		t_{AVQV}	t_{AA}	—	35	—	45	ns	
Enable Access Time		t_{ELQV}	t_{ACS}	—	35	—	45	ns	3
Output Hold from Address Change		t_{AXQX}	t_{OH}	4	—	4	—	ns	
Output Enable Access Time	MCM6209	t_{GLQV}	t_{OE}	—	15	—	17	ns	
Output Enable Low to Output Active	MCM6209	t_{GLQX}	t_{LZ}	0	—	0	—	ns	4,5,6
Output Enable High to Output High-Z	MCM6209	t_{GHQZ}	t_{HZ}	0	10	0	10	ns	4,5,6
Enable Low to Output Active		t_{ELQX}	t_{LZ}	4	—	4	—	ns	4,5,6
Enable High to Output High-Z		t_{EHQZ}	t_{HZ}	0	10	0	10	ns	4,5,6
Power Up Time		t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time		t_{EHICCL}	t_{PD}	—	35	—	45	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E} = V_{IL}$) and $\overline{G} = V_{IL}$ (MCM6209 only).

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note 3 Above)

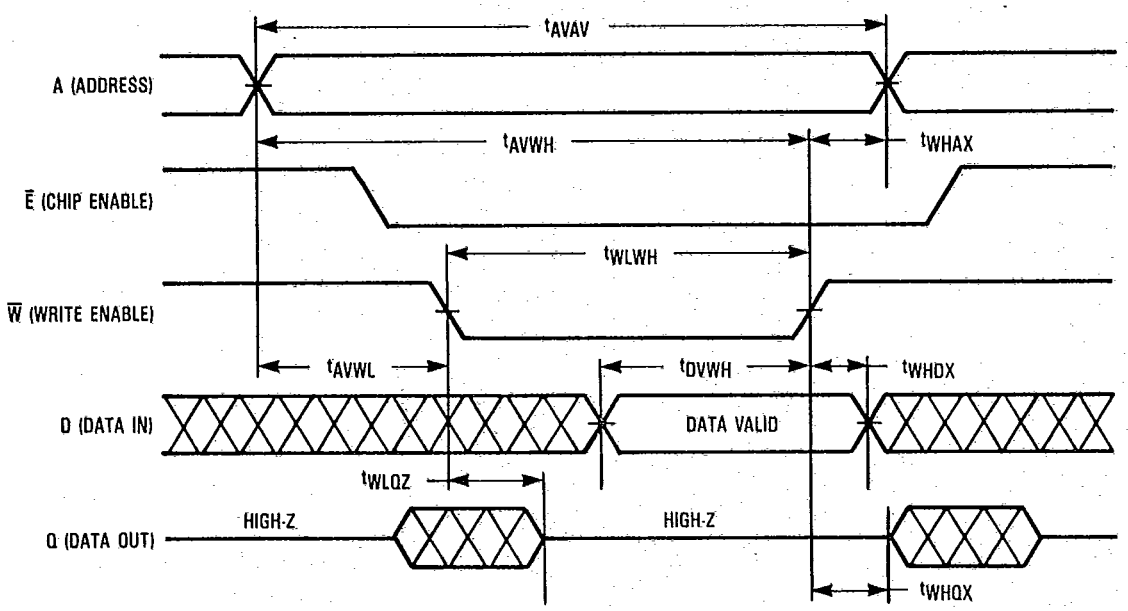


T-46-23-10

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM6208-35 MCM6209-35		MCM6208-45 MCM6209-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35	—	45	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	20	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	10	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. MCM6209, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



AC TEST LOADS

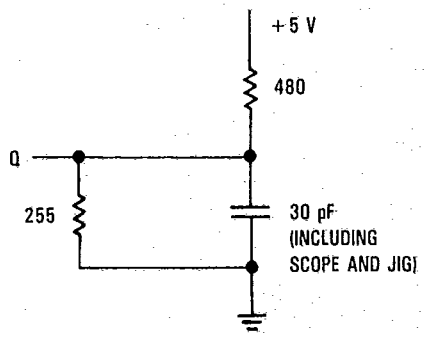


Figure 1A

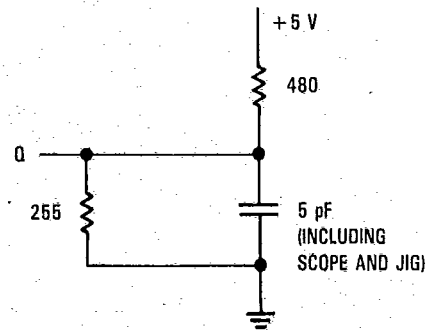


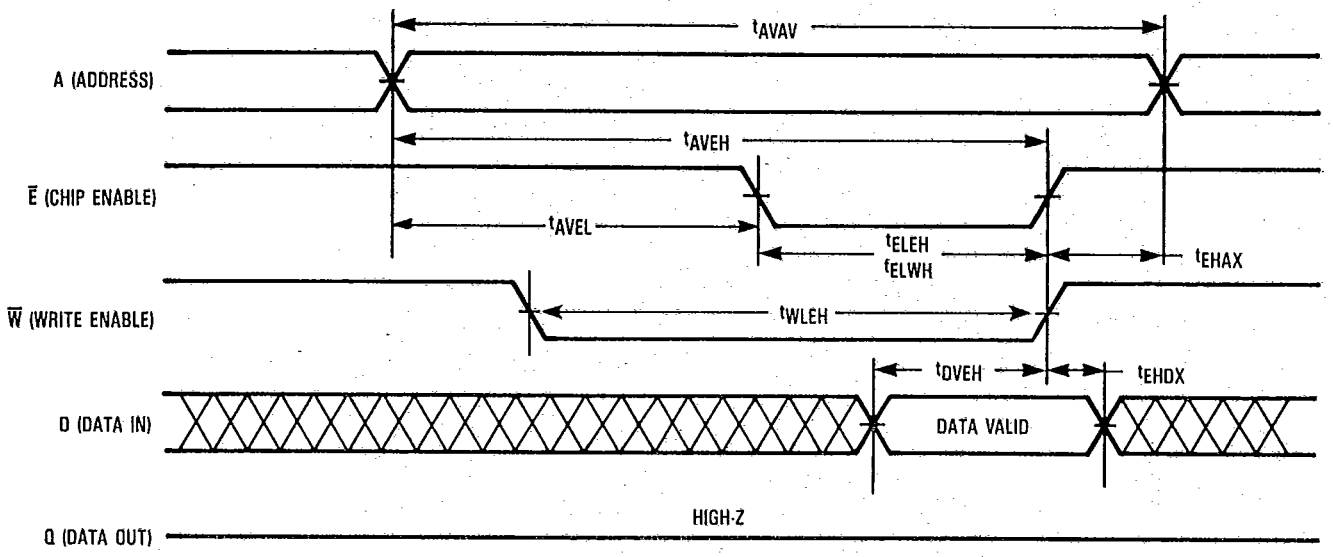
Figure 1B

T-46-23-10

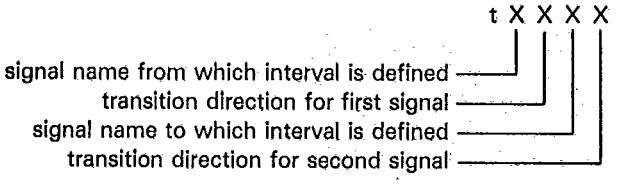
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 5)

Parameter	Symbol		MCM6208-35 MCM6209-35		MCM6208-45 MCM6209-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35	—	45	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	20	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	—	15	—	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	15	—	15	—	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	20	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.
5. MCM6209, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

T-46-23-10

ORDERING INFORMATION
(Order by Full Part Number)

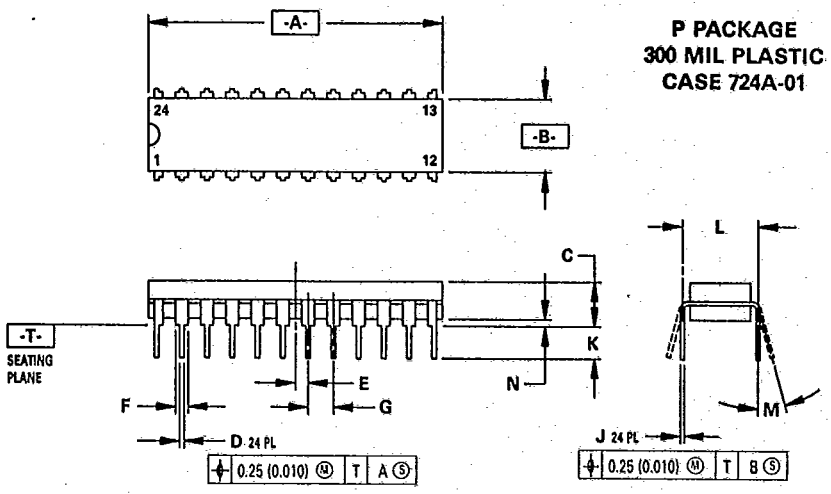
MCM 62XX X XX XX

- Motorola Memory Prefix
- Part Number
- Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- Speed (35 = 35 ns, 45 = 45 ns)
- Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6208P35, MCM6208P45, MCM6208J35, MCM6208J45, MCM6208J35R2, MCM6208J45R2, MCM6209P35, MCM6209P45, MCM6209J35, MCM6209J45, MCM6209J35R2, MCM6209J45R2

MCM6208-35, -45
PACKAGE DIMENSIONS

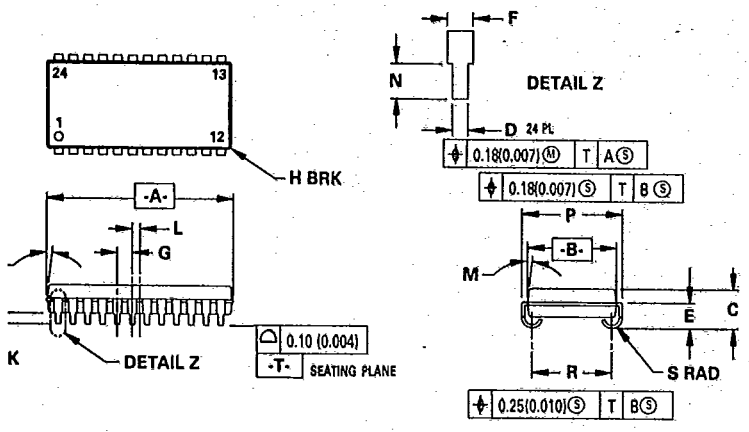
P PACKAGE
300 MIL PLASTIC
CASE 724A-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.47	29.71	1.160	1.170
B	7.12	7.62	0.280	0.300
C	3.81	4.57	0.150	0.180
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	3.18	3.42	0.125	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

J PACKAGE
300 MIL SOJ
CASE 810A-01



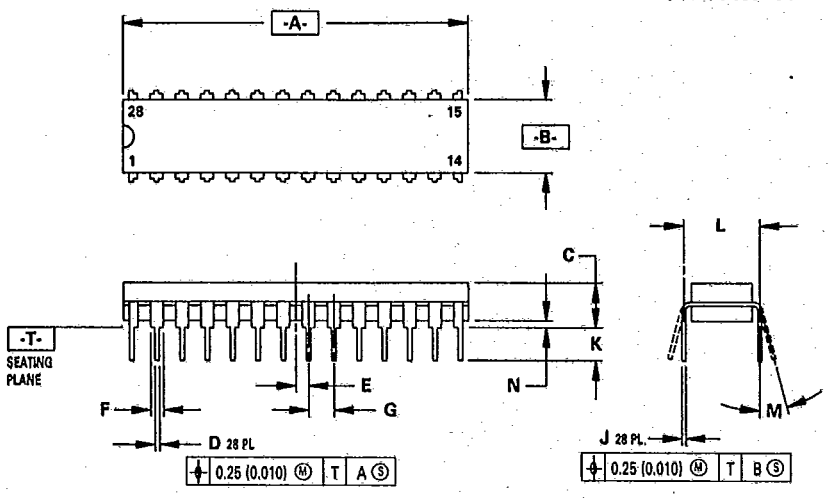
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.75	16.00	0.620	0.630
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.89	1.14	0.035	0.045
P	8.51	8.76	0.335	0.345
R	6.61	7.11	0.260	0.280
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM "R" TO BE DETERMINED AT DATUM -T-.

T-46-23-10

MCM6209-35, -45
PACKAGE DIMENSIONS

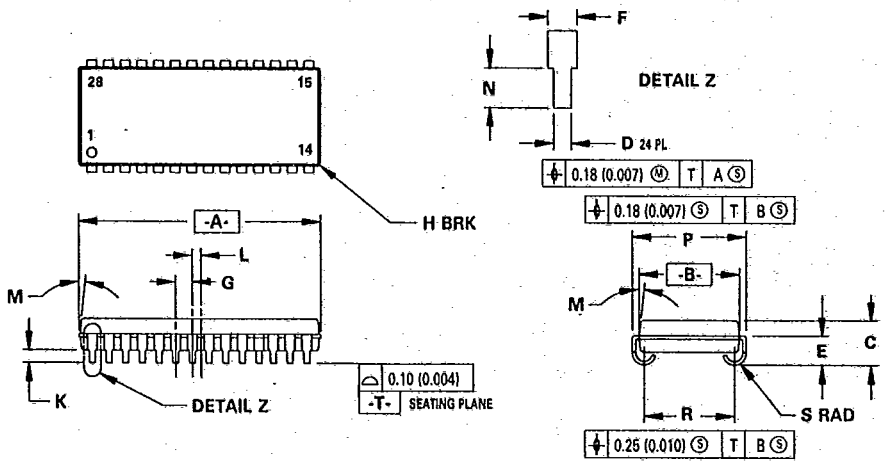
P PACKAGE
300 MIL PLASTIC
CASE 710B-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	34.55	34.79	1.360	1.370
B	7.12	7.62	0.280	0.300
C	3.81	4.57	0.150	0.180
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	3.18	3.42	0.125	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

J PACKAGE
300 MIL SOJ
CASE 810B-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.29	18.54	0.720	0.730
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	10°	0°	10°
N	0.89	1.14	0.035	0.045
P	8.51	8.76	0.335	0.345
R	6.61	7.11	0.260	0.280
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.