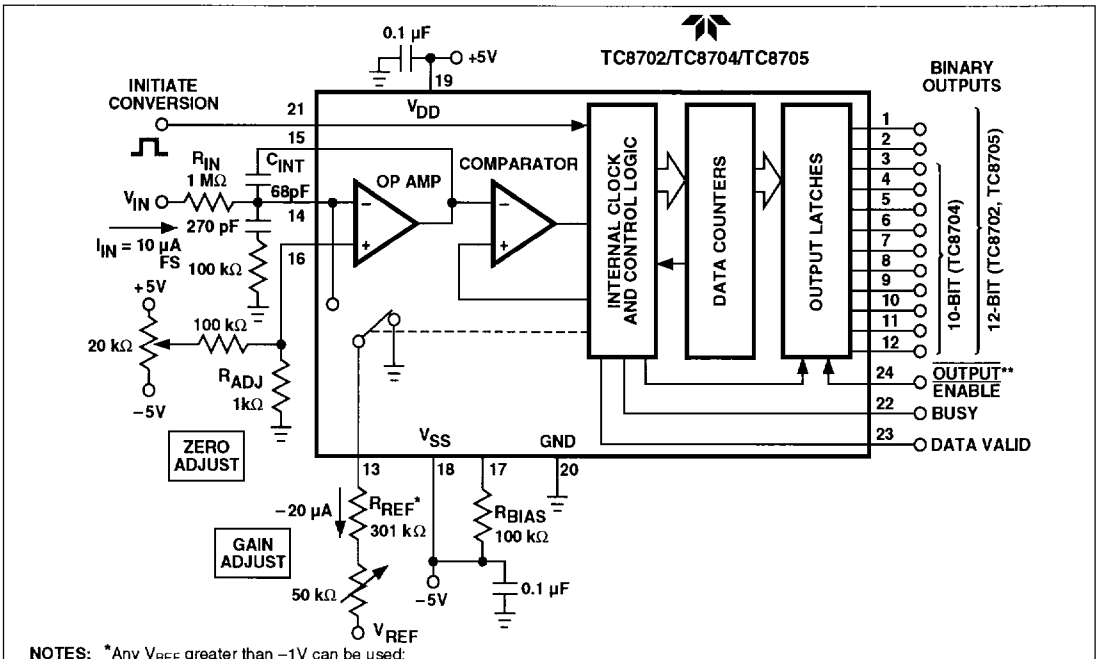
BINARY OUTPUT ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- High Accuracy — Up to 12-Bit Resolution With <±1/2 LSB Error
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation ..... 20 mW Typ
- Contains All Required Active Elements — Needs Only Passive Support Components, Reference Voltage, and Dual-Power Supply
- High Stability Over Full Temperature Range
  - — Gain Temperature Coefficient ... <25 ppm/°C Typ
  - — Zero Drift ..... <30 µV/°C Typ
  - — Differential Nonlinearity Drift ..... <25 ppm/°C Typ
- Latched Parallel Binary Outputs
- Three-State, Bus Compatible Outputs (TC8704 and TC8705)
- LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs
- Strobed or Free-Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

TEST CIRCUIT



NOTES: *Any V_{REF} greater than −1V can be used:

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example, with V_{REF} = −5V, R_{REF} = 250 kΩ

**No connection for TC8702.

4344 ILL F01

TC8702
TC8704
TC8705

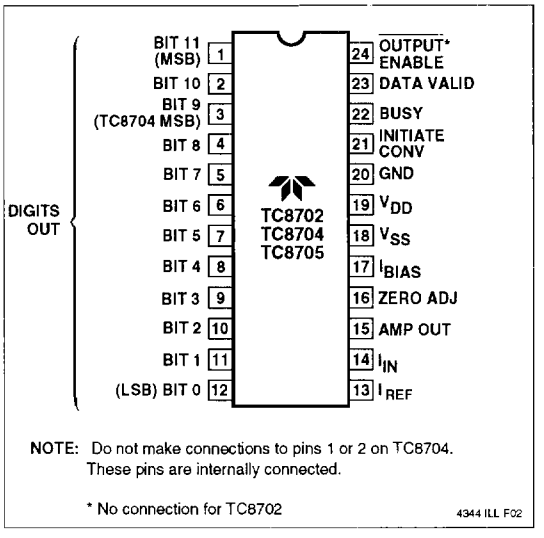
GENERAL DESCRIPTION

The TC8702/TC8704/TC8705 are 10- and 12-bit monolithic CMOS analog-to-digital converters (ADCs). Fully self-contained in a single 24-pin dual-in-line package, each converter requires only passive support components, reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero are counted. At the end of conversion, the total count is latched into the digital outputs as a 10- or 12-bit binary word.

The TC8704/8705 features a three-state output bus controlled by an output enable input. The output enable control switches to a high impedance or off-state when held high. The off-state allows bus-organized output connections. On the TC8702, outputs are always active.

PIN CONFIGURATION



NOTE: Do not make connections to pins 1 or 2 on TC8704. These pins are internally connected.

* No connection for TC8702

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ORDERING INFORMATION

Part No.	Previous Part No.	Resolution	Conversion Time (ms)	Package	Temperature Range
TC8702EHG	TSC8702CN	12-Bit	20	24-Pin CerDIP	–40°C to +85°C
TC8702MJG	TSC8702CN	12-Bit	20	24-Pin CerDIP	–55°C to +125°C
TC8704CPG	TSC8704CJ	10-Bit	5	24-Pin Plastic DIP	0°C to +70°C
TC8704EJG	TSC8704CL	10-Bit	5	24-Pin CerDIP	–40°C to +85°C
TC8704MJG	TSC8704BL	10-Bit	5	24-Pin CerDIP	–55°C to +125°C
TC8705CPG	TSC8705CJ	12-Bit	20	24-Pin Plastic DIP	0°C to +70°C
TC8705EHG	TSC8705CL	12-Bit	20	24-Pin CerDIP	–40°C to +85°C
TC8705MHG	TSC8705BL	12-Bit	20	24-Pin CerDIP	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

$V_{DD} - V_{SS}$ ..... +18V
I_{IN} ..... ±10 mA
I_{REF} ..... ±10 mA
Digital Input Voltage ..... −0.3V to V_{DD} +0.3V
Operating V_{DD} and V_{SS} Range ..... +3.5V to +7V
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
CPG ..... 0°C to +70°C
EJG ..... −40°C to +85°C
MJG, MHG ..... −55°C to +125°C

Package Dissipation ..... 500 mW
Lead Temperature (Soldering, 10 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V, V_{SS} = −5V, V_{GND} = 0, V_{REF} = −6.4V, R_{BIAS} = 100 kΩ, test circuit shown, unless otherwise specified. T_A = +25°C unless full temperature range is specified (−55°C to +125°C for MJG and MHG packages, −40°C to +85°C for EJG package, 0°C to +70°C for CPG package).

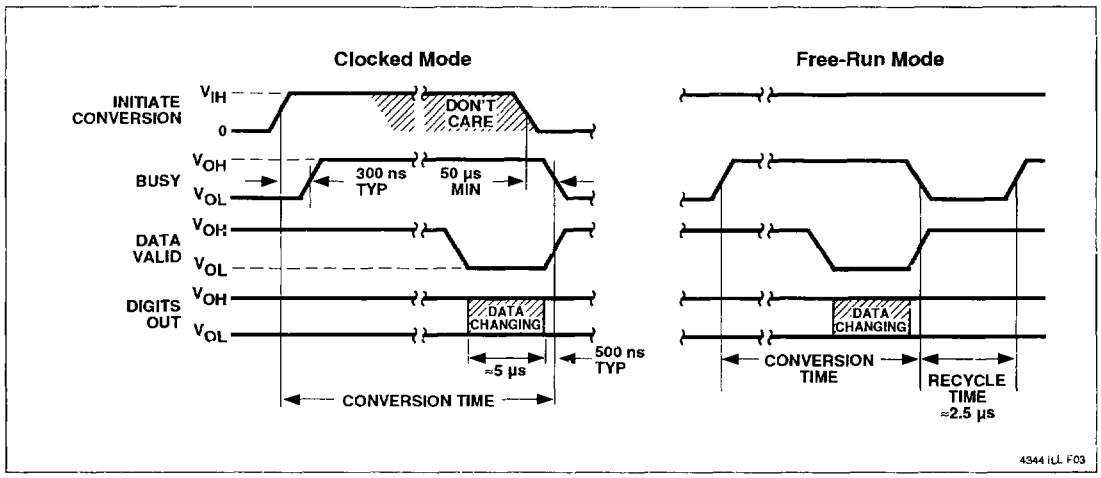
Parameter	Test Conditions	Definition	Min	Typ	CP/EJ Max	MJ/MH Max	Unit
Accuracy							
Resolution Accuracy							
TC8704		Binary Word Length of	10	—	—	—	Bits
TC8702/TC8705		Digital Output	12	—	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	±1/4	±1/2	±1/2	LSB
		(TC8705CPG Only)	—	1	±1.5	—	LSB
Differential Nonlinearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	±1/2	LSB
Differential Nonlinearity Temperature Drift	Full Temperature Range	Variation in Differential Nonlinearity Due to Temperature Change	—	±2.5	±5	±5	ppm/°C
Gain Variance		Variation From Exact A (Compensate by Trimming R_{IN} or R_{REF})	—	±2	±5	±5	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation in A Due to Temperature Change	—	±25	±75	±80	ppm/°C
Zero Offset	I_{IN} = 0, C_{INT} = 68 pF, R_{ADJ} = 1 kΩ (See Test Circuit)	Correction at Zero Adjust to Give Zero Output When Input is Zero	—	±10	±50	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation in Zero Offset Due to Temperature Change	—	±3	±5	±8	ppm/°C
Analog Input (See Note)							
I_{IN} Full Scale		Full-Scale Analog Input Current to Achieve Specified Accuracy	—	10	—	—	µA
I_{REF}		Reference Current Input to Achieve Specified Accuracy	—	−20	—	—	µA
Digital Input							
$V_{IN}(1)$	Full Temperature Range	Logic "1" Input Threshold for Initiate Conversion Input	3.5	—	—	—	V
$V_{IN}(0)$	Full Temperature Range	Logic "0" Input Threshold for Initiate Conversion Input	—	—	1.5	1.5	V

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Test Conditions	Definition	Min	Typ	CP/EJ Max	MJ/MH Max	Unit
Propagation Delay							
Output Enable (TC8704, TC8705)	C_L = 100 pF, R_L = 1 kΩ	t_{PLH}, t_{PHL}	—	500	—	1000	ns
Digital Output							
$I_{O(OFF)}$ (TC8704, TC8705)	OE = 3.5V 0.4V < V_C < 2.4V	Off-State Output Current	—	0.1	±10	±10	µA
V_{OUT}(1)	Full Temperature Range, I_{OUT} = −10 µA I_{OUT} = −500 µA	Logic "1" Output Voltage for Digits Out, Busy, and Data Valid Outputs	4.5 2.4	— —	— —	— —	V V
V_{OUT}(0)	Full Temperature Range, V_{DD} = 4.75V I_{OUT} = 500 µA	Logic "0" Output Voltage for Digits Out, Busy, and Data Valid Outputs	—	—	0.4	0.4	V
Dynamic							
Conversion Time TC8704 TC8702, TC8705	Full Temperature Range	Time Required to Perform One Complete A/D Conversion	 — —	 5 20	 6 24	 6 24	 ms ms
Conversion Rate in Free-Run Mode TC8704 TC8702, TC8705	$V_{INT\ CONV}$ = +5V		 167 42	 200 50	 — —	 — —	 sec
Minimum Pulse Width for Initiate Conversion	Full Temperature Range		500	—	—	—	ns
Supply Current							
I_{DD} Quiescent J/H Packages P Package	Full Temperature Range, $V_{INT\ CONV}$ = 0V	Current Required From Positive Supply During Operation	 — —	 1.4 1.4	 2.5 5	 3.5 —	 mA mA
I_{SS} Quiescent J/H Packages P Package	Full Temperature Range, $V_{INT\ CONV}$ = 0V	Current Required From Negative Supply During Operation	 — —	 −1.6 −1.6	 −2.5 −5	 −3.5 —	 mA mA
Supply Sensitivity	V_{DD} ±1V, V_{SS} ±1V	Change in Full-Scale Gain vs Supply Voltage Change	--	±0.5	±1	±1	%/V
	$\|V_{DD}\| = \|V_{SS}\|$ = 5V ±1V	Change in full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	±0.1	%/V

NOTE: I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See "Test Circuit."

TIMING DIAGRAMS



CIRCUIT DESCRIPTION

During conversion, the sum of a continuous current (I_{IN}) and pulses of a reference current (I_{REF}) is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} is balanced against the pulses of I_{REF}. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in binary) is latched into the outputs at the end of the conversion.

The converter contains two counters and a clock, in addition to an operational amplifier, comparator, latching output buffers, and housekeeping logic. One counter is a clock counter which starts counting clock pulses after a reset pulse; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times I_{REF} is switched into the summing input of the amplifier during the period defined by the clock counter.

When the initiate conversion input is strobed with a positive signal, the busy line latches high and a 10 µs (times given are approximate) start-up cycle begins. The integrating capacitor is discharged and both counters are reset during this start-up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 µs shutdown cycle. During the shutdown cycle, data valid goes low for 5 µs. This binary sequence is shown in the timing diagrams. Busy is true high and, when the circuit is busy, initiate conversion has no effect and may be high or low. Data valid is also true high. The data from a conversion remains valid for as long as power is applied to the circuit or until data valid falls at the end of a subsequent conversion, at which time the output data is updated to reflect the latest conversion.

PIN FUNCTIONS

Initiate Conversion Input

Accepts CMOS and most +5V logic inputs. Applying a logic "1" to the initiate conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the initiate conversion pin is disabled until conversion is complete. Two modes of operation are permitted: clocked or free-running. For clocked operation, the initiate conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation, the initiate conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low-power TTL (can sink and source 500 µA). A logic "1" output on the busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates conversion is complete and the result has been latched at the digit out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the

device is operating in the free-running mode, the busy output will remain low for approximately 2.5 µs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low-power TTL (can sink and source 50 µA). A logic "1" output at the data valid pin indicates the digits out pins are latched with the result of the last conversion cycle. The data valid output goes to logic "0" approximately 5 µs before the completion of a conversion cycle. During this 5 µs interval new data is being transferred to the digits out pins, and the digits out are not valid.

Digits Out

The binary digit outputs (Bit 0 . . . Bit 11) which are the result of the A/D conversion. These outputs are CMOS logic and low-power TTL compatible.

APPLICATIONS INFORMATION

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital counts} = \frac{V_{IN} \bullet A \bullet R_{REF}}{R_{IN} \bullet V_{REF}},$$

A = 2064 for TC8704; 8208 for TC8702/TC8705

where digital counts is the value of the binary output word presented at digits out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Outputs MSB LSB
$V_{IN} \leq$ Full Scale	1 . . . 111 . . . 1
= Full Scale –1 LSB	1 . . . 111 . . . 1
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high-accuracy conversion system depends on the voltage regulation of V_{REF} and thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. Supply connections V_{DD} and V_{SS} should have bypass capacitors of 0.1 µF value, or larger, at the device pins.

R_{IN}, R_{REF}

Values of these components are chosen to give a full-scale input current of approximately 10 µA and a reference current of approximately –20 µA:

$$R_{IN} \cong \frac{V_{IN}\ \text{Full Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}.$$

Examples:

$$R_{IN} \cong \frac{10V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} full scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high-accuracy applications because of their thermal stability and low-noise generation.

R_{BIAS}

Specifications for the TC87XX are based on R_{BIAS} = 100 kΩ ±10%, unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS}, the A/D will convert much faster and the supply current will be higher. For example, when R_{BIAS} is 20kΩ, the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA. Likewise, if R_{BIAS} is increased, the conversion time will be longer and the supply current will be much lower. For example, when R_{BIAS} = 1 MΩ, the conversion time will be six times longer, and supply current is now reduced to 0.5 mA. For details of this relationship, refer to AN–9 typical performance curves.

R_{DAMP}

The exact value is not critical, but should have a nominal value of 100Ω ±10%. Locate close to pin 14.

C_{DAMP}

The exact value is not critical, but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

The exact value is not critical, but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14 and 15.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5V are recommended, with 0.05% line and load regulation, and 0.1 μF decoupling capacitors.

Adjustment Procedure

The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e., below zero and above full scale), it is recommended transition points be used in setting the zero and full-scale values. The recommended procedure is:

(1) Set initiate conversion control high to provide free-run operation and verify converter is operating.

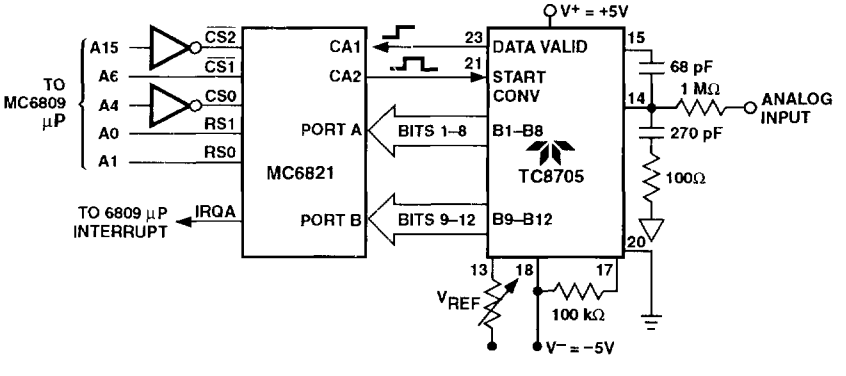
(2) Set V_{IN} to +1/2 LSB and trim the zero-adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.

(3) For full-scale adjustment, set V_{IN} to the full-scale value less 1-1/2 LSB and trim the gain-adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

TYPICAL APPLICATION/DESIGN CIRCUITS

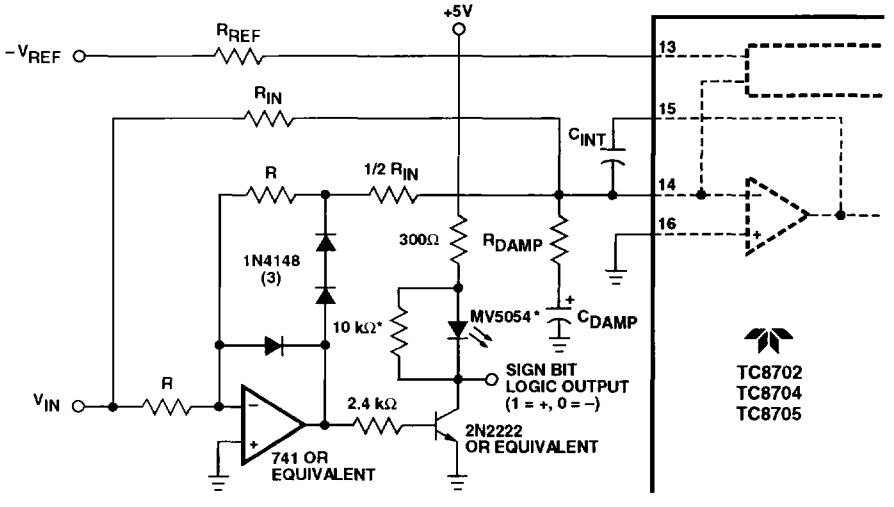
TC8705 Interface to MC6821 PIA



TYPICAL APPLICATION/DESIGN CIRCUITS (Cont.)

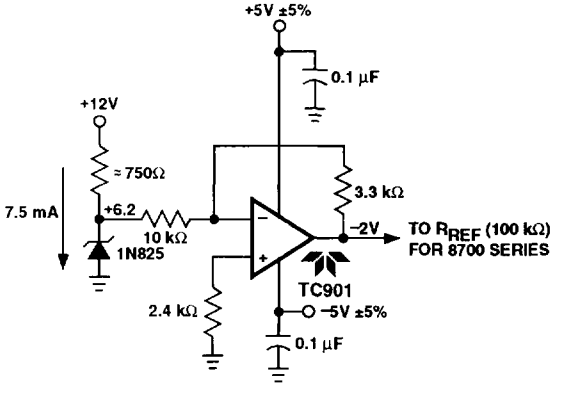
Bipolar Operation (+ and – Inputs)

ABSOLUTE VALUE CIRCUIT WITH SIGN



*Optional visual indication of negative input.
NOTE: Values for R should be between 10 kΩ and 100 kΩ.

Reference Voltage Supply



NOTE: $V_{REF} \approx 2V$ using voltages derived from 8080A µP.

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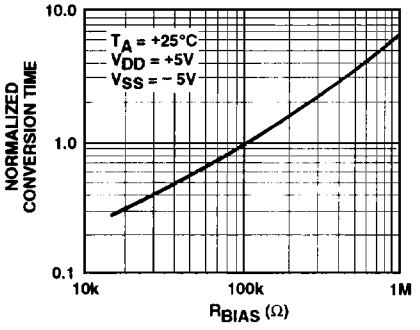
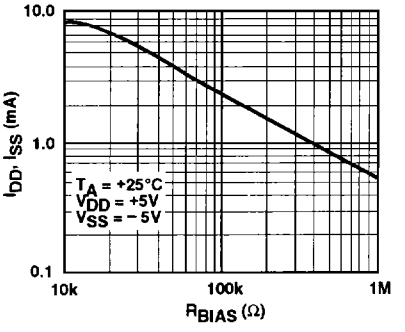
TYPICAL PERFORMANCE CURVES

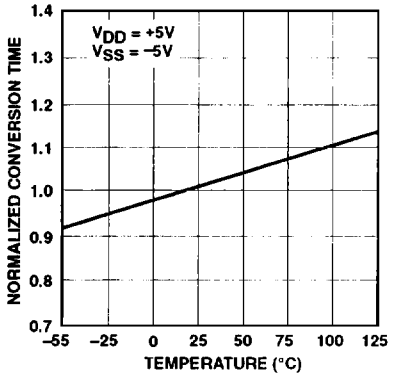
Conversion Time vs R_{BIAS}



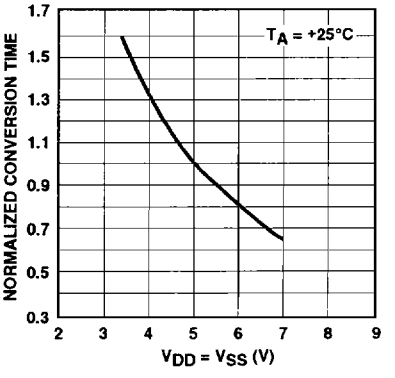
Supply Current vs R_{BIAS}



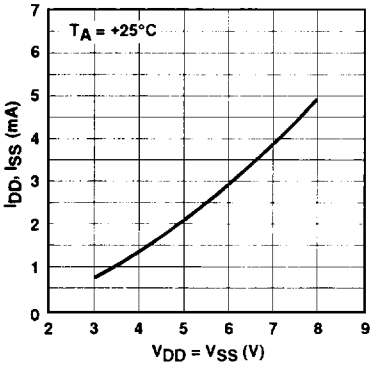
Conversion Time vs Temperature



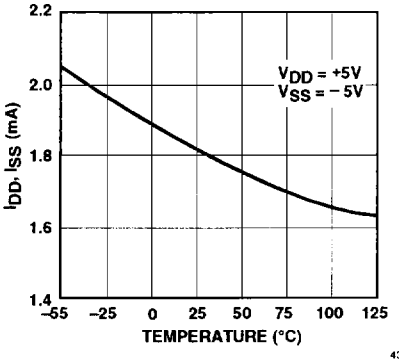
Conversion Time vs Supply Voltage



Supply Current vs Supply Voltage



Supply Current vs Temperature



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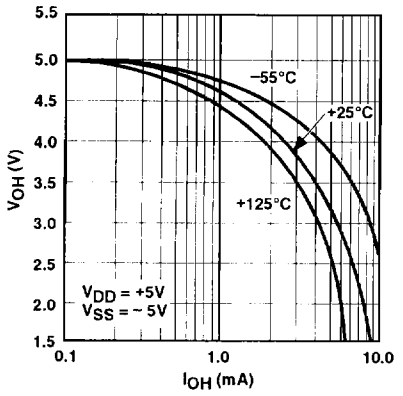
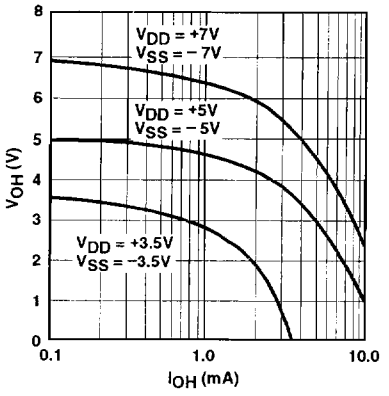
TYPICAL PERFORMANCE CURVES (Cont.)

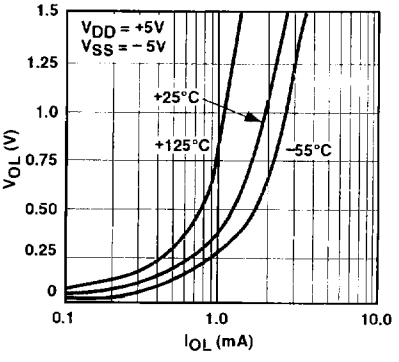
Output Source Current vs Temperature



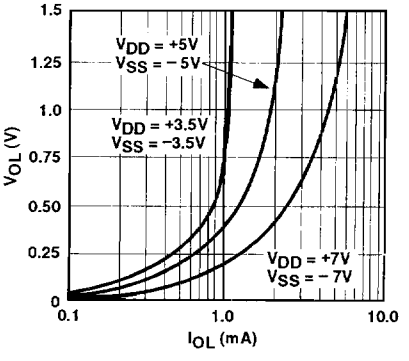
Output Source Current vs Supply Voltage



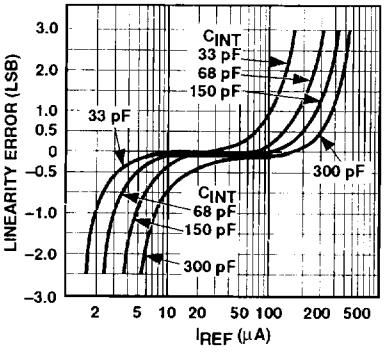
Output Sink Current vs Temperature



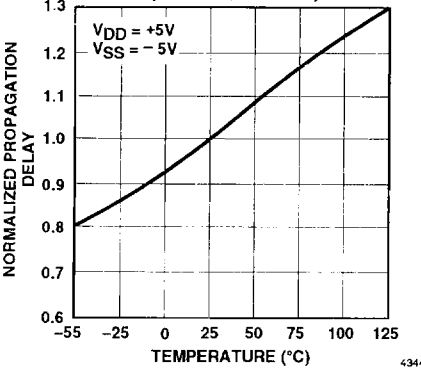
Output Sink Current vs Supply Voltage



Linearity vs Reference Current Input



Three-State Propagation Delay (TC8704, TC8705)



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