HARRIS SEMICONDUCTOR

HS-15530RH

Radiation Hardened CMOS Manchester Encoder-Decoder

December 1992

Features

- Functional Total Dose 1 x 10^5 RAD(Si)
- Latch-Up Free to 5 x 10^{11} RAD(Si)/s
- Support of MIL-STD-1553
- Low Operating Power 50mW at 5V
- 1.0 Megabit/s Data Rate
- Sync Identification and Lock-In
- Clock Recovery
- Manchester II Encode, Decode
- Separate Encode and Decode
- Military Temperature Range -55°C to +125°C

Description

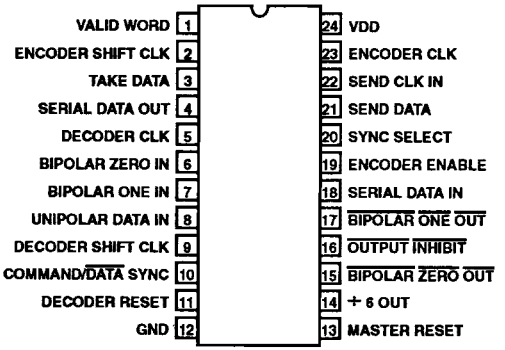
The Harris HS-15530 is a high performance, radiation resistant, CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over temperature while residing in a radiation environment. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5V supply.

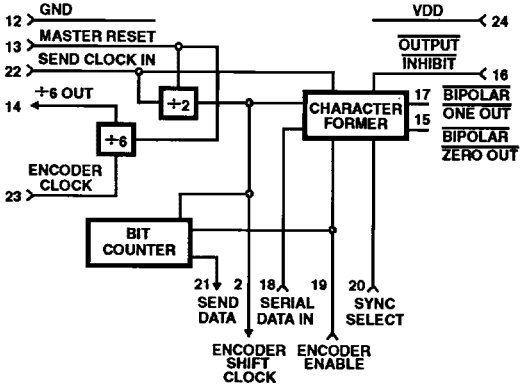
Pinout

24 PIN DIP
CASE OUTLINE D-3, CONFIGURATION 1
TOP VIEW

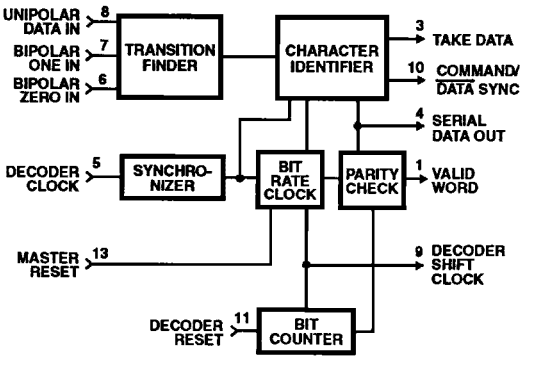


Block Diagrams

ENCODER



DECODER



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3203

Pin Description

NAME	PIN NO.	TYPE	SECTION	DESCRIPTION
VALID WORD	1	O	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
ENCODER SHIFT CLOCK	2	O	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of Encoder Shift Clock
TAKE DATA	3	O	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits
SERIAL DATA OUT	4	O	Decoder	Delivers received data in correct NRZ format
DECODER CLOCK	5	I	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to balance of the decoder, input a frequency equal to 12X the data rate
BIPOLAR ZERO IN	6	I	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
BIPOLAR ONE IN	7	I	Decoder	A high input should be applied when the bus is in its positive state. The pin must be held low when the Unipolar input is used.
UNIPOLAR DATA IN	8	I	Decoder	With pin 6 high and pin low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
DECODER SHIFT CLOCK	9	O	Decoder	Output which delvers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
COMMAND SYNC	10	O	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
DECODER RESET	11	I	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
GROUND	12	I	Both	Ground Supply pin.
MASTER RESET	13	I	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and reset the ÷6 circuit.
÷6 OUT	14	O	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK
BIPOLAR ZERO OUT	15	O	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
OUTPUT INHIBIT	16	I	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
BIPOLAR ONE OUT	17	O	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
SERIAL DATA IN	18	I	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK
ENCODER ENABLE	19	I	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete).
SYNC SELECT	20	I	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
SEND DATA	21	O	Encoder	An active high output which enables the external source of serial data.
SEND CLOCK IN	22	I	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷6 output
ENCODER CLOCK	23	I	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
VDD	24	I	Both	VDD is the +5V power supply pin. A 0.1µF decoupling capacitor from VDD (pin 24) to GROUND (pin 12) is recommended.

NOTE: I = Input and O = Output

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
I/O Voltage (applied for all grades) ..... VSS-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 10mA/MHz in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
CERDIP Package	48.9°C/W	9.9°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.715W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.75V to +5.25V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.2VDD
Input High Voltage ..... 0.7VDD to VDD
Clock Input Low Voltage (VILC) ..... 0V to 0.5V
Clock Input High Voltage (VIHC) ..... VDD-0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output High Voltage	VOH	VDD = 4.75V, IO = -3mA, VIN = 0V or 4.75V	1, 2, 3	-55°C, +25°C, +125°C	2.4	-	V
Output Low Voltage	VOL	VDD = 4.75V, IO = +1.8mA, VIN = 0V or 4.75V	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Input Leakage Current	IIL or IIH	VDD = 5.25V, VIN = 0V or 5.25V	1, 2, 3	-55°C, +25°C, +125°C	-1.0	1.0	µA
Standby Power Supply Current	IDDSB	VDD = 5.25V, VIN = 5V, IO = 0mA	1, 2, 3	-55°C, +25°C, +125°C	-	2	mA
Functional Tests	FT	VDD = 4.75 and 5.25V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 5.25V, VIN = 1.95V or 3.68V and VDD = 4.75V, VIN = 0.95V or 3.32V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

AC's tested at worst case VDD, AC's guaranteed over full operating specifications.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ENCODER TIMING							
Encoder Clock Frequency	FEC	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	15	MHz
Send Clock Frequency	FESC	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	2.5	MHz
Data Rate	FED	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	1.25	MHz
Shift Clock Delay	TE1	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	125	ns
Sync Pulse Width	TE7	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	150	-	ns
Bipolar Output Delay	TE9	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	125	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

AC's tested at worst case VDD, AC's guaranteed over full operating specifications.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
DECODER TIMING							
Decoder Clock Frequency	FDC	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	15	MHz
Data Rate	FDD	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	1.25	MHz
Decoder Reset Setup Time	TDRS	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	75	-	ns
Sync Delay "ON"	TD6	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns
Take Data Delay "ON"	TD7	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns
Sync Delay "OFF"	TD9	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns
Take Data Delay "OFF"	TD10	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns
Valid Word Delay	TD11	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz (Note 1)	T_A = +25°C	-	5	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz (Note 1)	T_A = +25°C	-	8	pF
Operating Supply Current	IDDOP	VDD = 5.25V, VIN = VDD or GND, f = 1MHz, IO = 0mA	-55°C < T_A < +125°C	-	10	mA
ENCODER TIMING REQUIREMENTS						
Encoder Clock Rise Time	TECR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	8	ns
Encoder Clock Fall Time	TECF	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	8	ns
Master Reset Pulse Width	TMR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	150	-	ns
Serial Data Setup	TE2	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	75	-	ns
Serial Data Hold	TE3	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	75	-	ns
Enable Setup	TE4	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	90	-	ns
Enable Pulse Width	TE5	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	100	-	ns
Sync Setup	TE6	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	55	-	ns
Send Data Delay	TE8	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	0	50	ns
DECODER TIMING REQUIREMENTS						
Decoder Clock Rise Time	TDCR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	8	ns
Decoder Clock Fall Time	TDCF	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	8	ns
Decoder Reset Pulse Width	TDR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	150	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Master Reset Pulse Width	TDMR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	150	-	ns
Bipolar Data Pulse Width (Note 2)	TD1	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	TDC+10	-	ns
Sync Transition Span (Notes 2, 3)	TD2	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	18TDC	-	ns
One Zero Overlap (Note 2)	TD3	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	TDC-10	ns
Short Data Transition Span (Notes 2, 3)	TD4	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	6TDC	-	ns
Long Data Transition Span (Note 2, 3)	TD5	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	12TDC	-	ns
Serial Data Out Delay	TD8	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	80	ns

NOTES:

1. All measurements referenced to device ground.
2. TDC = Decoder Clock Period = 1/FDC
3. These parameters are given for information only and are typical values.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

IDDSB at VDD = 5.0V will be measured and recorded for each device within one hour (±15 minutes) after irradiation. The lot will be accepted only if the average of these IDDSB measurements is less than or equal to 5mA.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) GROUP B, SUBGROUP 5

Table 5 Intentionally left blank.

TABLE 6. APPLICABLE SUBGROUPS

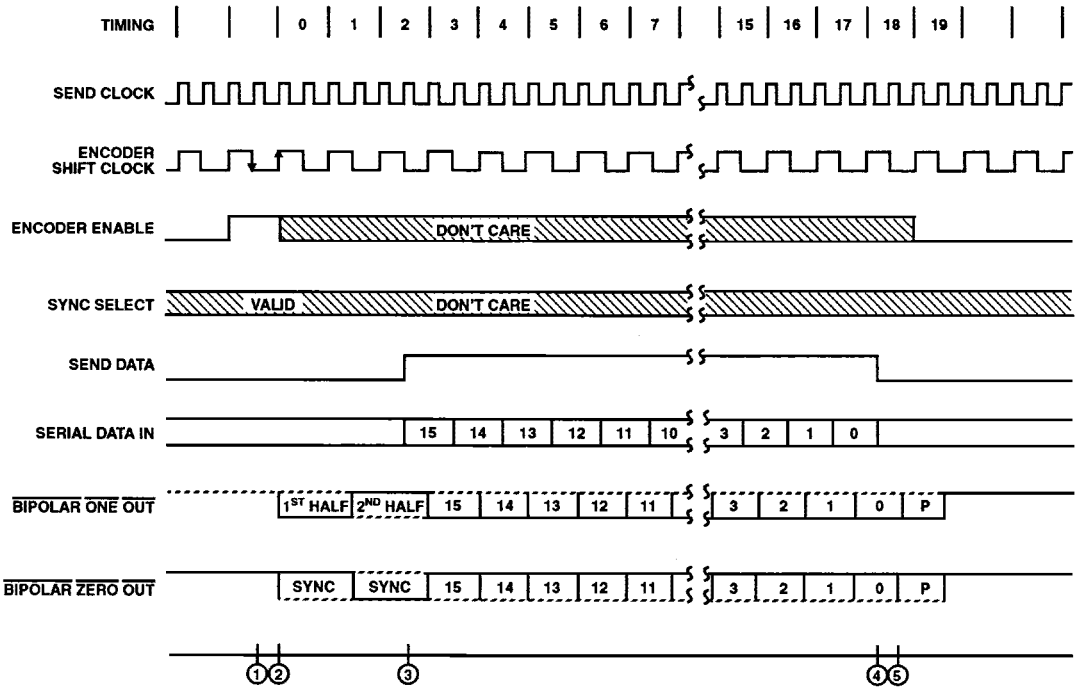
CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test	100%/5004	1, 7, 9
PDA	100%/5004	1, 7
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D Others	Samples/5004	1, 7
Group E Subgroup 2	Samples/5004	1, 7, 9

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK (1). This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word (2). When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods (3). During these sixteen periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK so it can be sampled on the low-to-high transition (3) - (4). After the sync and Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the ENCODER adds on an addtional bit which is the parity for that word (5). If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time (5) as shown to prevent a consecutive word from being encoded. At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the ENCODER in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



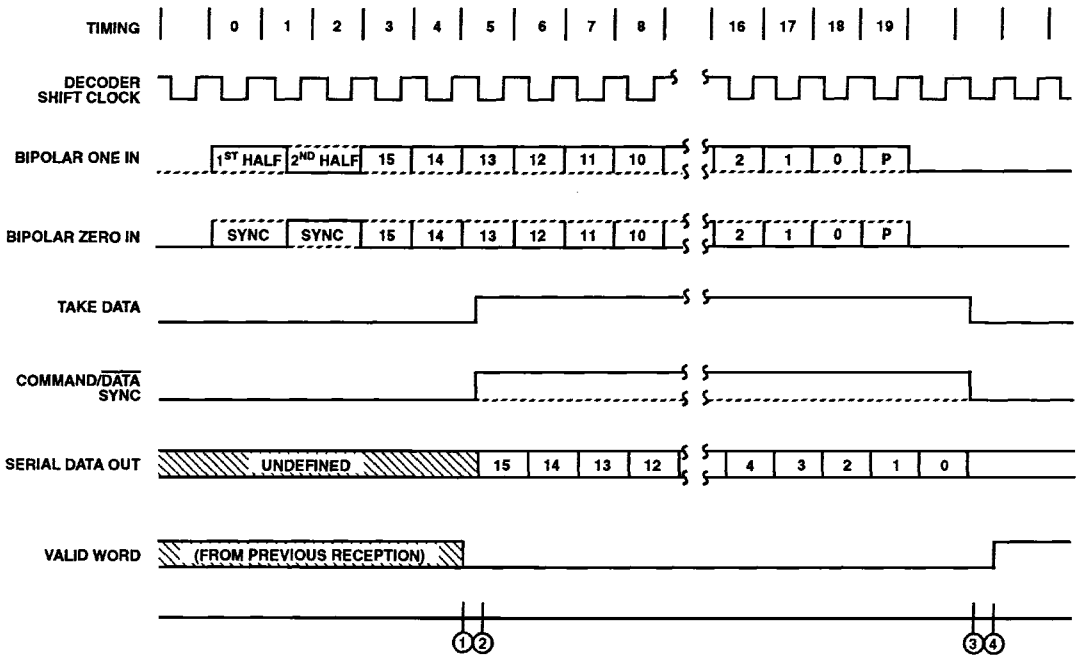
Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ONE OUT}}$ of an Encoder through an inverter to Unipolar Data Input).

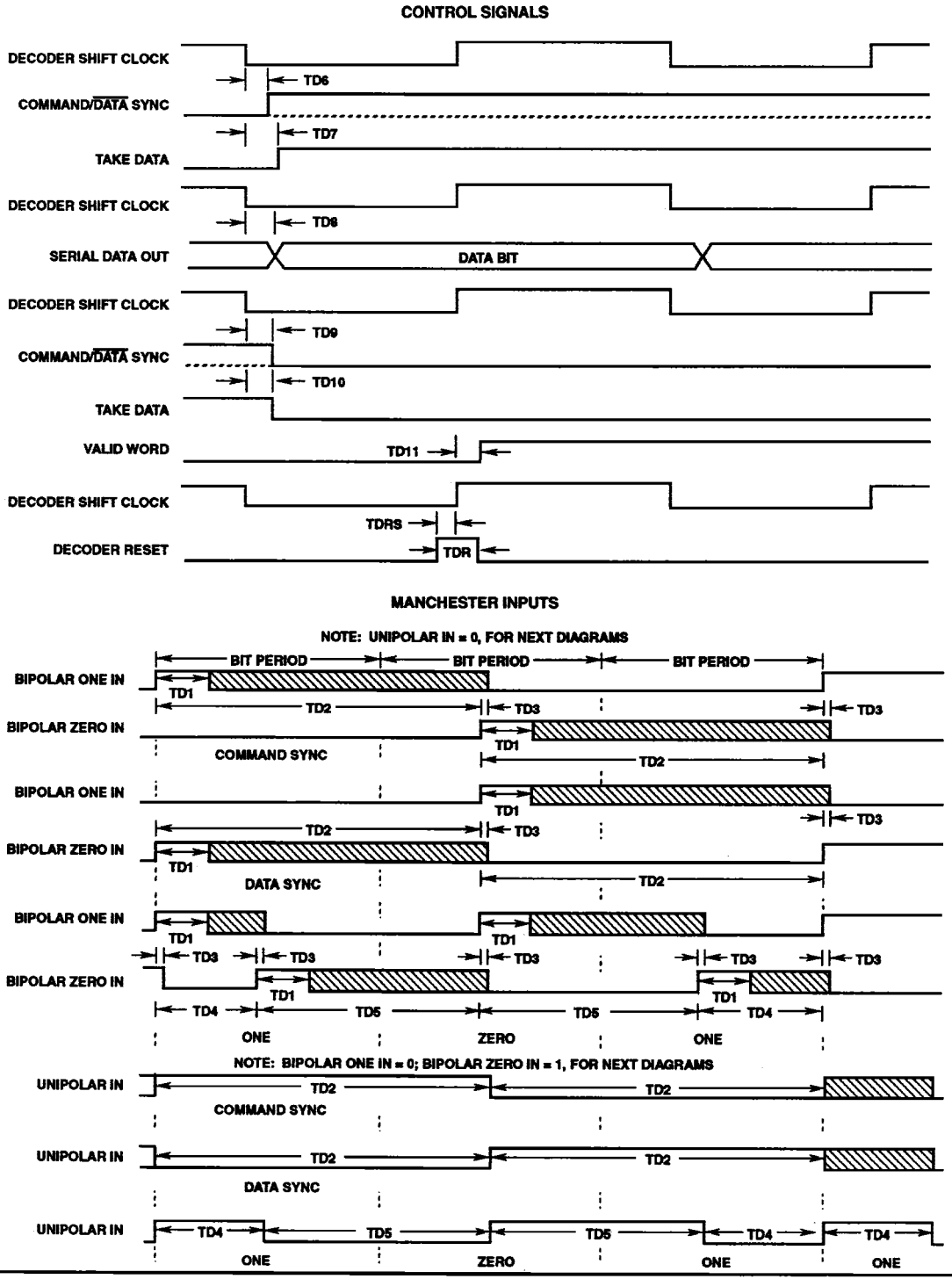
The Decoder is free running and countinuously monitors its data input lines for a valid sync character and two valid sync is recognized (1), the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high (2) and remain high for sixteen DECODER SHIFT CLOCK periods (3), otherwise it will remain low. The TAKE DATA output will go high and remain high (2) - (3). While the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock (2) - (3). Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted (3) the data is checked for odd parity. A high on VALID WORD output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown (1).

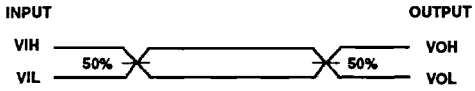
At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.



Decoder Timing

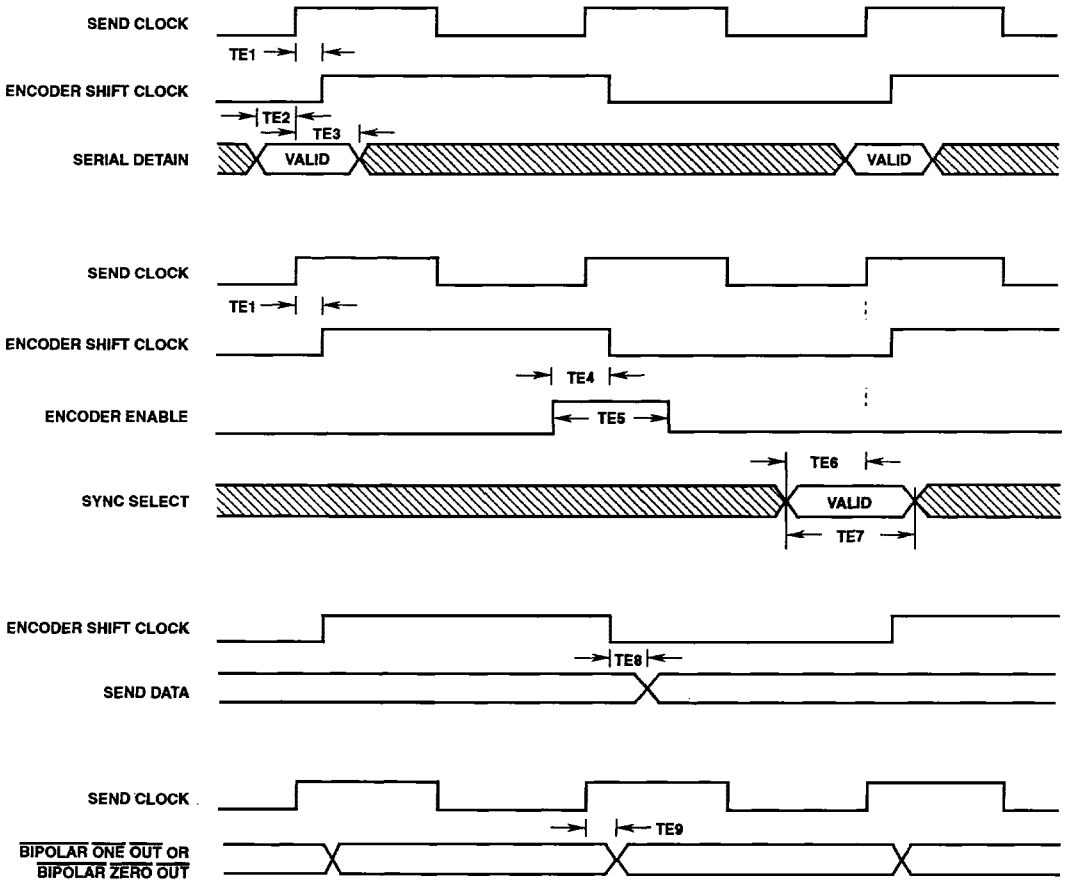


AC Testing Input, Output Waveform



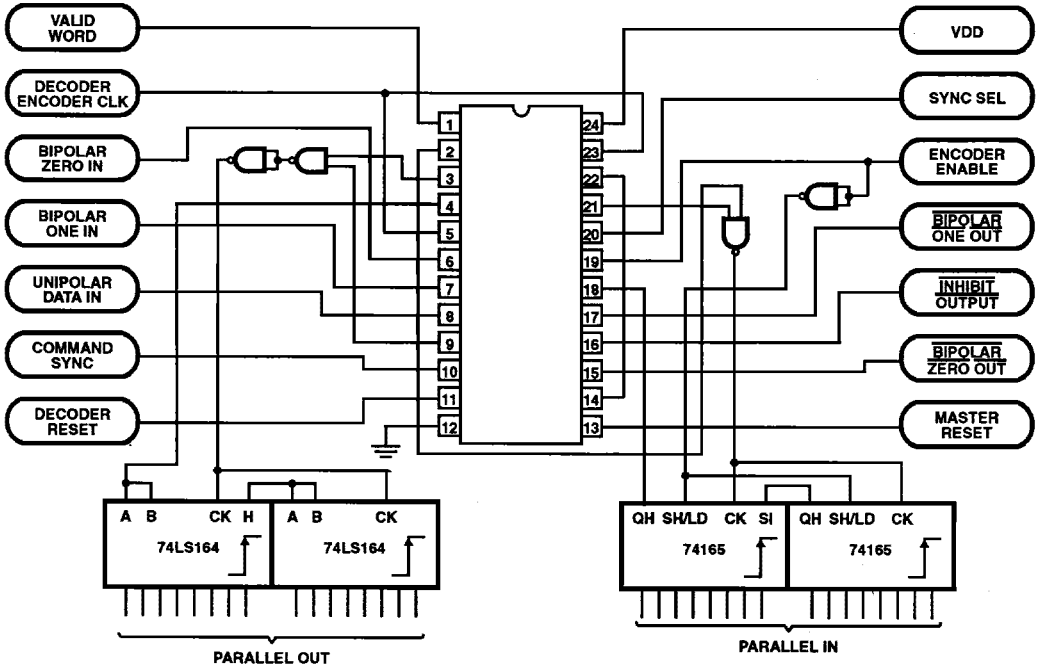
NOTE: AC Testing: All input signals must switch between VIL and VIH. Input rise and fall times are driven at 1ns/V.

Encoder Timing

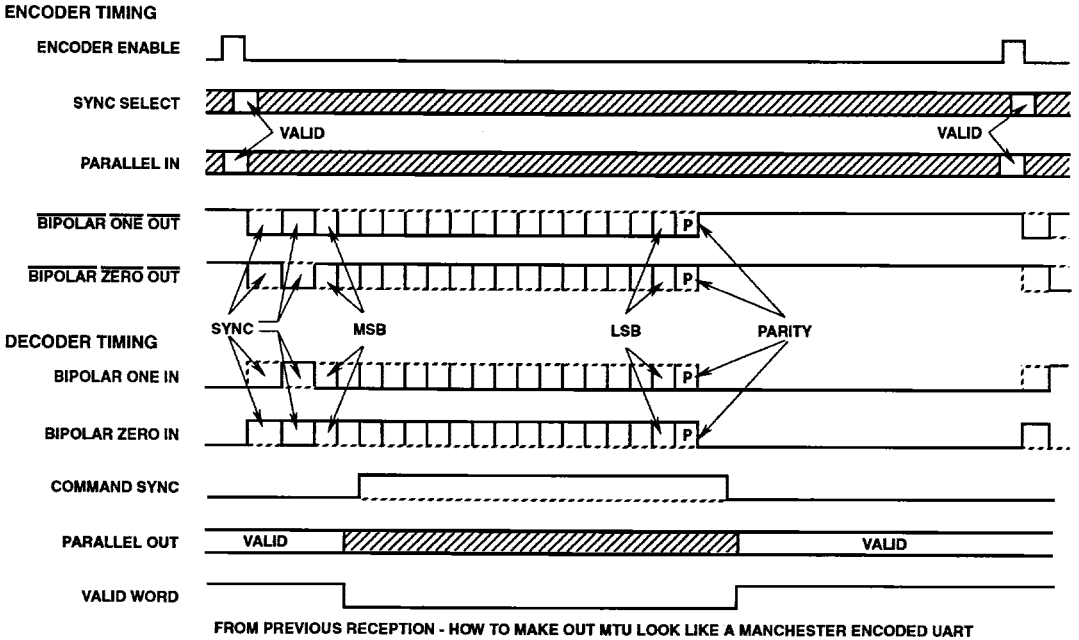


Applications

HOW TO MAKE OUR MTU LOOK LIKE A MANCHESTER ENCODED UART



TYPICAL TIMING DIAGRAM FOR A MANCHESTER ENCODED UART



FROM PREVIOUS RECEPTION - HOW TO MAKE OUT MTU LOOK LIKE A MANCHESTER ENCODED UART

MIL-STD-1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HS-15530RH supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words. Terminals respond with Status Words. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20ms. The word formats are shown in Figure 4. The special abbreviations are as follows:

- P — Parity, which is defined to be odd, taken across all 17 bits.
- R/T — Receive on logical zero, transmit on ONE.
- ME — Message Error if logical 1.
- TF — Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

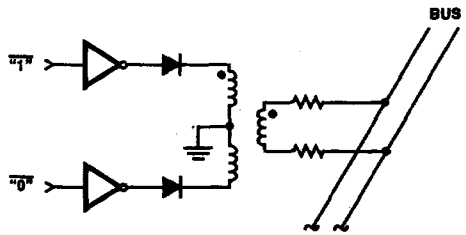


FIGURE 1. SIMPLIFIED MIL-STD-1553 DRIVER

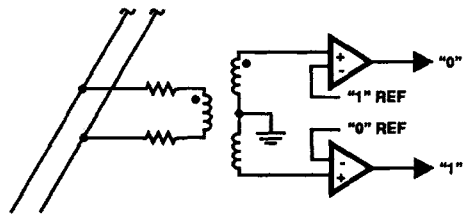


FIGURE 2. SIMPLIFIED MIL-STD-1553 RECEIVER

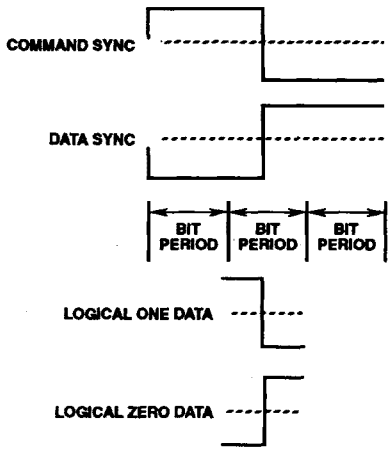


FIGURE 3. MIL-STD-1553 CHARACTER FORMATS

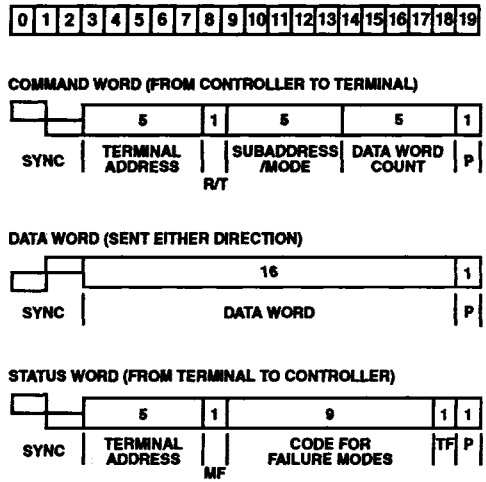
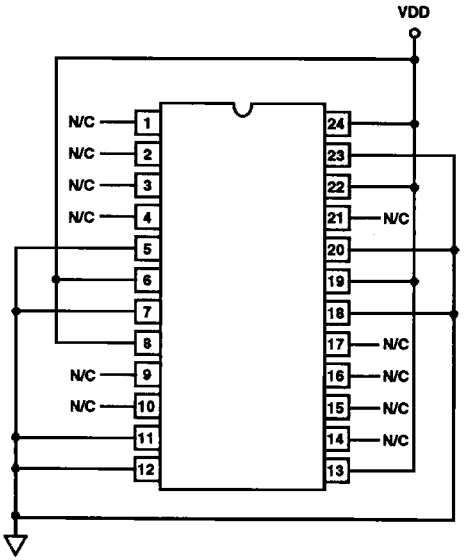


FIGURE 4. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HS-15530RH.

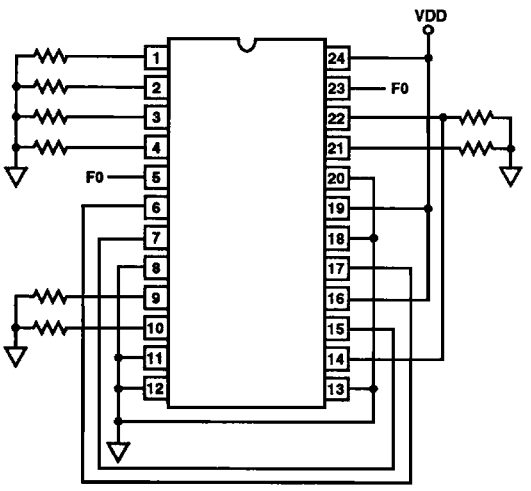
Burn-In Circuits



STATIC CONFIGURATION

NOTES:

VDD = 5.0V
IDD < 2mA
T_A min = +125°C

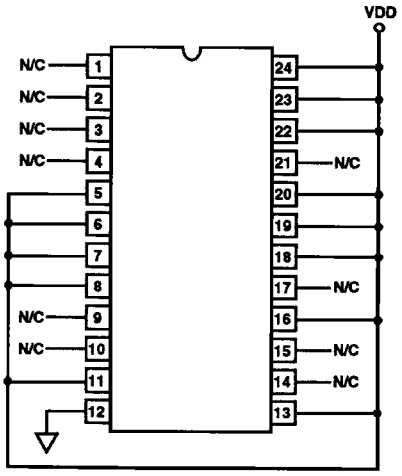


DYNAMIC CONFIGURATION

NOTES:

VDD = 5.0V
IDD < 10mA
T_A min = +125°C
All resistors 1.8kΩ 1/4 watt
F0 = 200KHz Square Wave, 50% Duty cycle
VIL = 0.5V
VIH = 4.5V

Irradiation Circuit



NOTES:

VDD = 5.0V
Group E Sample Size is 2 die/wafer from 20% of yielding wafers

Harris - '-8' Flow

Internal Visual Inspection	+25°C Electrical Tests +125°C, -55°C
Gamma Radiation Assurance Tests Method 1019	Group A Inspection Method 5005. 5% PDA (Note 3)
Customer Pre-Cap Visual Inspection (Note 1)	Brand
Temperature Cycling Method 1010 Condition C	Customer Source Inspection (Note 1)
Fine and Gross Leak Tests Method 1014	Group C Inspection Method 5005 (Note 1, 2)
Constant Acceleration Method 2001 Y1 30KG	Group D Inspection Method 5005 (Note 1, 2)
Initial Electrical Tests	External Visual Inspection Method 2009
Dynamic Burn-In 160 Hours, +125°C Method 1015 Condition D	Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable
4. '-8' Data Pack Contains:
   Assembly Attributes (post seal)
   Test Attributes (including Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper).

Metallization Topology

DIE DIMENSIONS:
3934 x 4953µm x 485µm ±25µm

METALLIZATION:
Type: Silicon-Aluminum
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy

WORST CASE CURRENT DENSITY:
$1.8 \times 10^5 A/cm^2$

Metallization Mask Layout

HS-15530RH