

LCD Dot Matrix Driver LSI

LH5021B/LH5022

T-51-17

LH5021B/LH5022 LCD Dot Matrix Driver LSI

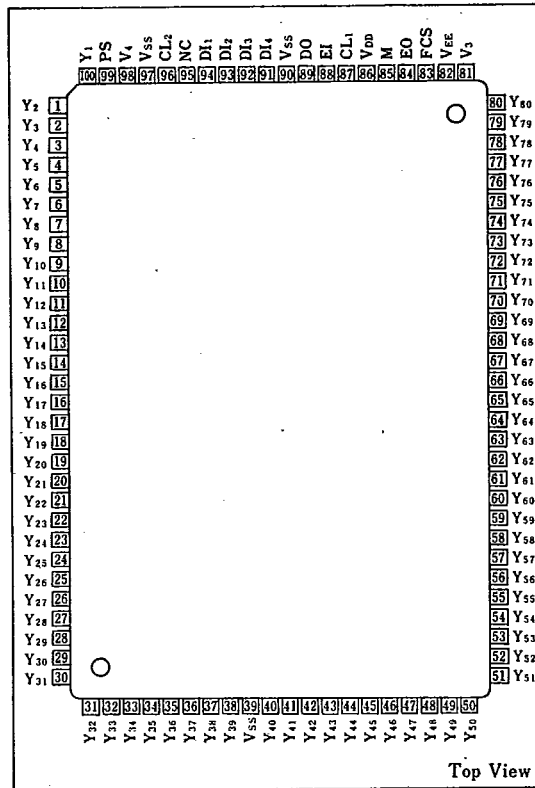
■ Description

LH5021B/LH5022 is an LCD driver LSI which can receive either serial input data or parallel input data. In case of the serial input mode, it can be connected in series. It converts character pattern data input to parallel data output with 80-bit latch circuit and provides character pattern waveforms output in accordance with mode select signal.

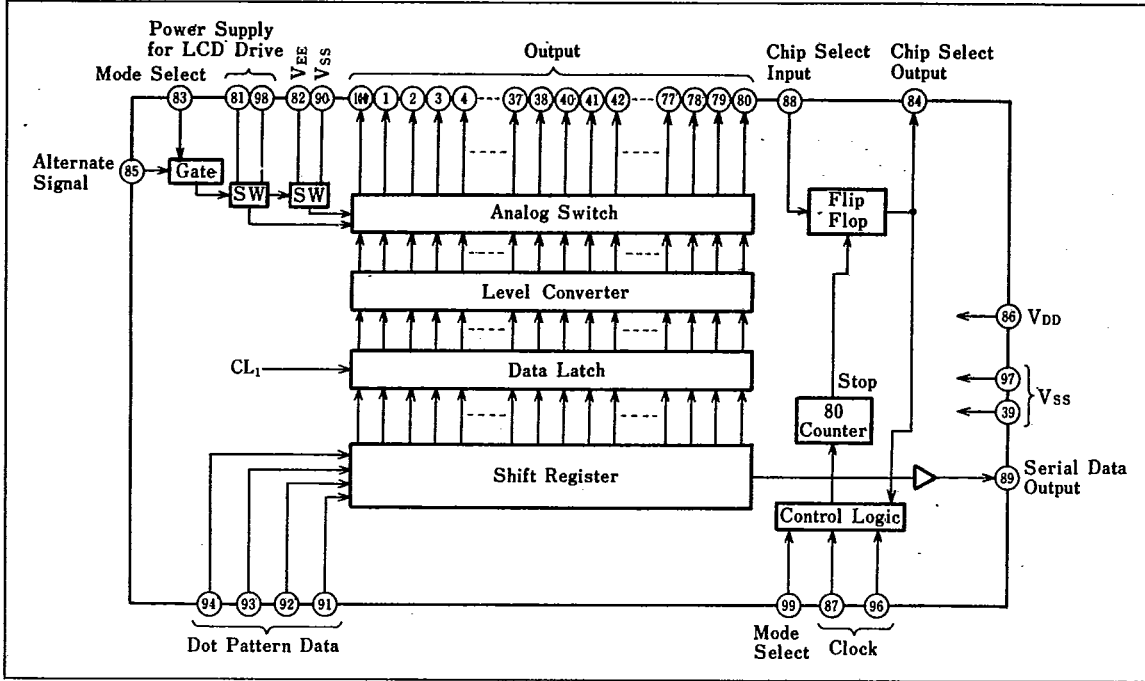
■ Features

1. CMOS process
2. 80-LCD driver circuit
3. 4 functions selectable as follows
 - (a) Segment signal drivers on the serial input mode
 - (b) Segment signal drivers with the chip-selectable function on the serial input mode
 - (c) Segment signal drivers with the chip-selectable function on the parallel input mode
 - (d) Common signal drives on the serial input mode
4. Auto count function ; in a chip selected state, counts 80 input data automatically and stops the internal clock CL₂
5. Power supply voltage : -5V (TYP.)
6. Display voltage
LH5021B : -17V (TYP.),
LH5022 : -24V (TYP.)
7. 100-pin quad-flat package

■ Pin Connections



Block Diagram



Pin Description

Pin name	Name	I/O	Functions																											
V_{DD}	Power supply	I	For logic circuit (-5V)																											
V_{EE}			For liquid crystal drive circuit (LH5021A: -17V, LH5022: -24V)																											
V_{SS}			GND																											
V_3, V_4	Segment output voltage supply	I	Durling non-select, however $V_{SS} > V_3 > V_4 > V_{EE}$																											
Y_1-Y_{80}	Segment output	O																												
CL_1	Clock	I	For data latch *It must be applied when 4 times the shift clock																											
CL_2			For data shift																											
FCS, PS	Mode select	I	<table border="1"> <thead> <tr> <th>FCS</th> <th>PS</th> <th>Mode</th> <th>Chip select</th> <th>DO out.</th> </tr> </thead> <tbody> <tr> <td>Low</td> <td>Low</td> <td>1-bit serial input segment driver</td> <td>No</td> <td>Yes</td> </tr> <tr> <td>Low</td> <td>High</td> <td>4-bit parallel input segment driver</td> <td>Yes</td> <td>High</td> </tr> <tr> <td>High</td> <td>Low</td> <td>1-bit serial input segment driver</td> <td>Yes</td> <td>High</td> </tr> <tr> <td>High</td> <td>High</td> <td>Common driver (serial input)</td> <td>No</td> <td>Yes</td> </tr> </tbody> </table>	FCS	PS	Mode	Chip select	DO out.	Low	Low	1-bit serial input segment driver	No	Yes	Low	High	4-bit parallel input segment driver	Yes	High	High	Low	1-bit serial input segment driver	Yes	High	High	High	Common driver (serial input)	No	Yes		
			FCS	PS	Mode	Chip select	DO out.																							
			Low	Low	1-bit serial input segment driver	No	Yes																							
			Low	High	4-bit parallel input segment driver	Yes	High																							
			High	Low	1-bit serial input segment driver	Yes	High																							
High	High	Common driver (serial input)	No	Yes																										
Note 1: In the serial input mode, data is supplied from the DI_1 pin.																														
Note 2: The relationship between data input during 4-bit parallel input and the Y output is as follows.																														
<ul style="list-style-type: none"> • DI_1 : $Y_1, Y_5, Y_9, \dots, Y_{73}, Y_{77}$ • DI_2 : $Y_2, Y_6, Y_{10}, \dots, Y_{74}, Y_{78}$ • DI_3 : $Y_3, Y_7, Y_{11}, \dots, Y_{75}, Y_{79}$ • DI_4 : $Y_4, Y_8, Y_{12}, \dots, Y_{76}, Y_{80}$ 																														
Note 3: When used as a common driver, the clock used for transfer is input to the CL_2 pin. CL_1 is internally fixed.																														
Note 4: To minimize current consumption, it is necessary to fix unused input pins to the same level as the V_{SS} pin or the V_{DD} pin.																														
M	Liquid crystal drive waveform AC conversion signal input	I	Common signal drive mode Segment signal drive mode																											
			<table border="1"> <thead> <tr> <th>Latch data</th> <th>M</th> <th>Y out.</th> <th>Latch data</th> <th>M</th> <th>Y out.</th> </tr> </thead> <tbody> <tr> <td>Low</td> <td>Low</td> <td>V_3</td> <td>Low</td> <td>Low</td> <td>V_3</td> </tr> <tr> <td>(non-display)</td> <td>High</td> <td>V_4</td> <td>(non-display)</td> <td>High</td> <td>V_4</td> </tr> <tr> <td>High</td> <td>Low</td> <td>GND</td> <td>High</td> <td>Low</td> <td>V_{EE}</td> </tr> <tr> <td>(display)</td> <td>High</td> <td>V_{EE}</td> <td>(display)</td> <td>High</td> <td>GND</td> </tr> </tbody> </table>	Latch data	M	Y out.	Latch data	M	Y out.	Low	Low	V_3	Low	Low	V_3	(non-display)	High	V_4	(non-display)	High	V_4	High	Low	GND	High	Low	V_{EE}	(display)	High	V_{EE}
Latch data	M	Y out.	Latch data	M	Y out.																									
Low	Low	V_3	Low	Low	V_3																									
(non-display)	High	V_4	(non-display)	High	V_4																									
High	Low	GND	High	Low	V_{EE}																									
(display)	High	V_{EE}	(display)	High	GND																									
DI_1-DI_4	Display data input	I	When used with a common driver and in the serial input mode, supply the data to the DI_1 pin. In this case, it is necessary to fix DI_2-DI_4 to the V_{SS} level or the V_{DD} level.																											
DO	Serial data output	O	When used in the chip select mode, it becomes high level.																											
EI	For chip select	I	Used only in the chip select mode.																											
EO		O	<ol style="list-style-type: none"> (1) The ($CL_1 \cdot CL_2$) timing causes EO to become low level. (2) After (1), the device is set to the select mode by inputting a high signal to EI, and the input data is read in according to the timing of the fall of CL_2. (3) When 80 items of input data (equivalent to 80 CL_2 clock cycles in the serial mode or 20 CL_2 clock cycles in the 4-bit parallel mode) have been read in, EO automatically becomes high level and data read in is terminated. EO is reset 1.5 cycles later. 																											

Pin name	Name	I/O	Functions
			<p>(4) When two or more devices are used in the chip select mode, EO of the first stage and EI of the second stage are connected and used.</p> <ol style="list-style-type: none"> EO of all devices connected is reset by (1) and goes to the non-select condition and waits for EI input. When a high signal is applied to EI of the initial device in the cascade connection, this device performs the operations in (2) and (3). Connecting EO of the initial devices to EI of the next devices causes the devices perform the operations in (2) and (3) after the initial device. This operation is repeated in the same manner for all subsequent devices. <p>In the non-select condition, the shift clock CL₂ stops internally, so power consumption becomes extremely small.</p>

Absolute Maximum Ratings

Parameter	Symbol	LH5021B	LH5022	Unit	Note
		Ratings	Ratings		
Applied voltage (logic)	V _{DD}	-7 to +0.3	-7 to +0.3	V	1
Applied voltage (Liquid crystal drive circuit)	V _{EE}	-20 to +0.3	-30 to +0.3	V	1
Input voltage (logic)	V _{IN}	V _{DD} -0.3 to +0.3	V _{DD} -0.3 to +0.3	V	1
Operating temperature	T _{opr}	-20 to +70	-20 to +70	°C	
Storage temperature	T _{stg}	-55 to +150	-55 to +150	°C	

Note 1: The maximum applicable voltage on any pin with respect to V_{SS}.

DC characteristics

LH5021B

(V_{SS}=0V, V_{DD}=-5V±10%, V_{EE}=-17±1V, T_a=-20 to +70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input "Low" voltage	V _{IL}				0.8V _{DD}	V
Input "High" voltage	V _{IH}		0.2V _{DD}			V
Output "Low" voltage	V _{OL}	I _{OL} =0.4mA			V+0.4	V
Output "High" voltage	V _{OH}	I _{OH} =0.4mA	-0.4			V
Voltage drop between Vi-Yi	V _{D1}	Apply 0.2mA to one of Y ₁ -Y ₈₀			1.1	V
Voltage drop between Vi-Yi	V _{D2}	Apply 0.2mA to each of Y ₁ -Y ₈₀			1.5	V
Input leakage current	I _{LI}				1.0	μA
Output leakage current	I _{LO}				10.0	μA
Current consumption for logic unit	I _{LOG}	Logic clock : 3.3 MHz		2.2	6.0	mA

LH5022

$$(V_{SS}=0V, V_{DD}=-4.5 \text{ to } -5.5V, V_{EE}=-21 \text{ to } -27V, \\ V_3=-2.5 \text{ to } -5.5V, V_4=-16.5 \text{ to } -23.5V, T_a=-20 \text{ to } +70^\circ\text{C})$$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input "Low" voltage	V_{IL}				$0.8V_{DD}$	V
Input "High" voltage	V_{IH}		$0.2V_{DD}$			V
Output "Low" voltage	V_{OL}	$I_{OL}=0.4\text{mA}$			$V_{DD}+0.4$	V
Output "High" voltage	V_{OH}	$I_{OH}=0.4\text{mA}$	-0.4			V
Voltage drop between V_1 - Y_1	V_{D1}	Apply 0.5mA to one of Y_1 - Y_{80} $V_3=2/12V_{EE}$, $V_4=10/12V_{EE}$			1.0	V
Voltage drop between V_1 - Y_1	V_{D2}	Apply 0.08mA to each of Y_1 - Y_{80} $V_3=2/12V_{EE}$, $V_4=10/12V_{EE}$			1.5	V
Input leakage current	$ I_{LI} $				1.0	μA
Output leakage current	$ I_{LO} $				10.0	μA
Current consumption for logic unit	I_{LOG}	Logic clock : 3.3 MHz			5.0	mA
		1-bit serial transfer : 3.3MHz 4-bit parallel transfer : 2.0MHz			10.0	mA

LH5022

$$(V_{SS}=0V, V_{DD}=-4.5 \text{ to } -5.5V, V_{EE}=-15 \text{ to } -24V, \\ V_3=-5 \text{ to } +1.5V, V_4=-11.5 \text{ to } -21V, T_a=-20 \text{ to } +70^\circ\text{C})$$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input "Low" voltage	V_{IL}				$0.8V_{DD}$	V
Input "High" voltage	V_{IH}		$0.2V_{DD}$			V
Output "Low" voltage	V_{OL}	$I_{OL}=0.4\text{mA}$			$V_{DD}+0.4$	V
Output "High" voltage	V_{OH}	$I_{OH}=0.4\text{mA}$	-0.4			V
Voltage drop between V_1 - Y_1	V_{D1}	Apply 0.35mA to one of Y_1 - Y_{80} $V_3=2/12V_{EE}$, $V_4=10/12V_{EE}$			1.0	V
Voltage drop between V_1 - Y_1	V_{D2}	Apply 0.06mA to each of Y_1 - Y_{80} $V_3=2/12V_{EE}$, $V_4=10/12V_{EE}$			1.5	V
Input leakage current	$ I_{LI} $				1.0	μA
Output leakage current	$ I_{LO} $				10.0	μA
Current consumption for logic unit	I_{LOG}	Logic clock : 3.3 MHz			5.0	mA
		1-bit serial transfer : 3.3MHz 4-bit parallel transfer : 2.0MHz			10.0	mA

AC Characteristics

(1) 1-bit Serial Input Segment Driver (PS=FCS="Low") ($V_{DD} = -5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20$ to $+70^\circ\text{C}$)

Parameter	Symbol	Conditions*1	MIN.	MAX.	Unit	Applicable pins
Clock frequency	t_c		300		ns	CL ₂
Clock "High" width	t_{cWH}		130		ns	CL ₂
Clock "Low" width	t_{cWL}		130		ns	CL ₁ , CL ₂
Data setup time	t_{SU}		70		ns	DI ₁
Data hold time	t_H		50		ns	DI ₁
Output delay	t_D	$C_L = 15\text{pF}$		230	ns	DO
Latch clock "High" width	t_{LWH}		130	*3	ns	CL ₁
Clock margin time (from CL ₁ ↓ to CL ₂ ↓)	t_{c12}		20		ns	CL ₁ , CL ₂
Clock margin time*2 (from CL ₂ ↓ to CL ₁ ↓)	t_{c21}		200		ns	CL ₁ , CL ₂
Clock margin time (from CL ₂ ↑ to CL ₁ ↑)	t_{p21}		20		ns	CL ₁ , CL ₂
Clock ↑, ↓ time	t_{cT}			50	ns	CL ₁ , CL ₂
Overlap time of CL ₂ "Low" and CL ₁ "High"	t_{ov}		130		ns	CL ₁ , CL ₂

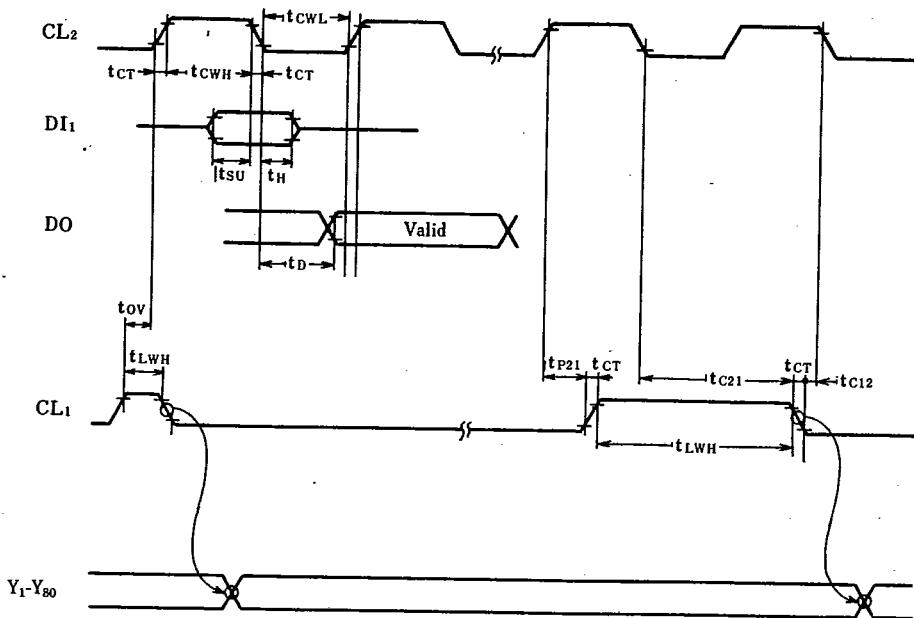
Test conditions

Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.2V_{DD}$, $0.8V_{DD}$

*1 LH5021B : $V_{EE} = -17V \pm 1V$, LH5022 : $V_{EE} = -24V \pm 3V$

*2 Internal shift register valid time

*3 $1.5t_c - t_{c12} - t_{p21} - 3t_{cT}$



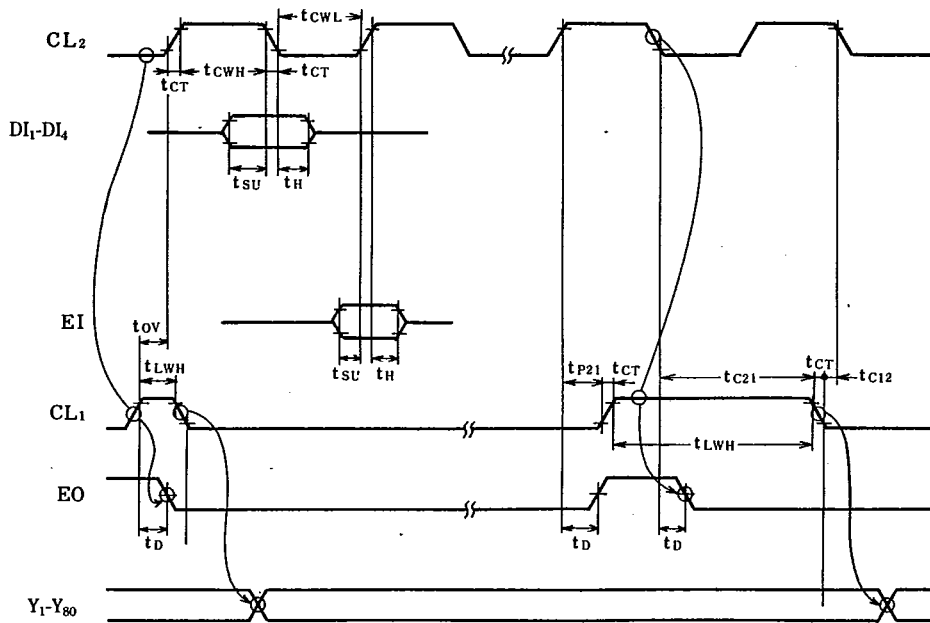
(2) 4-bit Input Segment Driver (PS="High", FCS="Low") ($V_{DD} = -5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$)

Parameter	Symbol	Conditions* ¹	MIN.	MAX.	Unit	Applicable pins
Clock frequency	t_c		500		ns	CL ₂
Clock "High" width	t_{cWH}		230		ns	CL ₂
Clock "Low" width	t_{cWL}		230		ns	CL ₁ , CL ₂
Data setup time	t_{sU}		70		ns	DI ₁ , DI ₂ , DI ₃ , DI ₄ , EI
Data hold time	t_H		50		ns	DI ₁ , DI ₂ , DI ₃ , DI ₄ , EI
Output delay	t_D	$C_L = 15pF$		230	ns	EO
Latch clock "High" width	t_{LWH}		130	*3	ns	CL ₁
Clock margin time (from CL ₁ ↓ to CL ₂ ↓)	t_{c12}		20		ns	CL ₁ , CL ₂
Clock margin time* ² (from CL ₂ ↓ to CL ₁ ↓)	t_{c21}		200		ns	CL ₁ , CL ₂
Clock margin time (from CL ₂ ↑ to CL ₁ ↑)	t_{p21}		20		ns	CL ₁ , CL ₂
Clock ↑, ↓ time	t_{cT}			50	ns	CL ₁ , CL ₂
Overlap time of CL ₂ "Low" and CL ₁ "High"	t_{ov}		130		ns	CL ₁ , CL ₂

Test conditions

Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.2V_{DD}$, $0.8V_{DD}$ *1 LH5021B : $V_{EE} = -17V \pm 1V$, LH5022 : $V_{EE} = -24V \pm 3V$

*2 Internal shift register valid time

*3 $1.5t_c - t_{c12} - t_{p21} - 3t_{cT}$ 

(3) Common Driver (PS="Low", FCS="High")

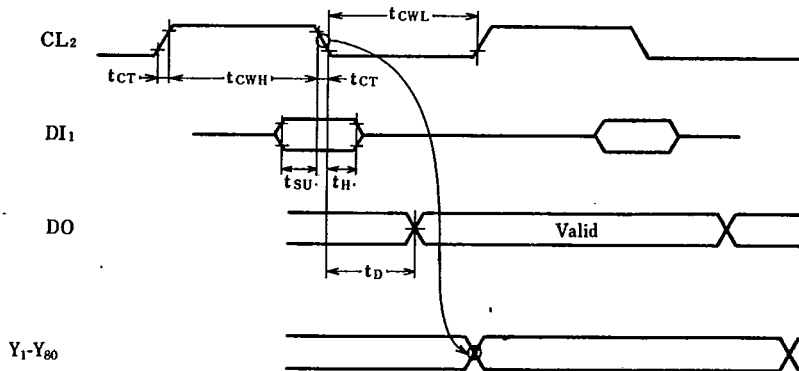
($V_{DD} = -5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$)

Parameter	Symbol	Conditions *1	MIN.	MAX.	Unit	Applicable pins
Clock frequency	t_c		1000		ns	CL ₂
Clock "High" width	t_{cWH}		130		ns	CL ₂
Clock "Low" width	t_{cWL}		830		ns	CL ₂
Data setup time	t_{su}		70		ns	DI ₁
Data hold time	t_h		50		ns	DI ₁
Output delay	t_D	$C_L = 15pF$		500	ns	DO
Clock ↑, ↓ time	t_{CT}			50	ns	CL ₂

Test conditions

Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.8V_{DD}$, $0.2V_{DD}$

*1 LH5021B : $V_{EE} = -17V \pm 1V$, LH5022 : $V_{EE} = -24V \pm 3V$



(4) 1-bit Serial Input Segment Driver (PS="Low", FCS="High")

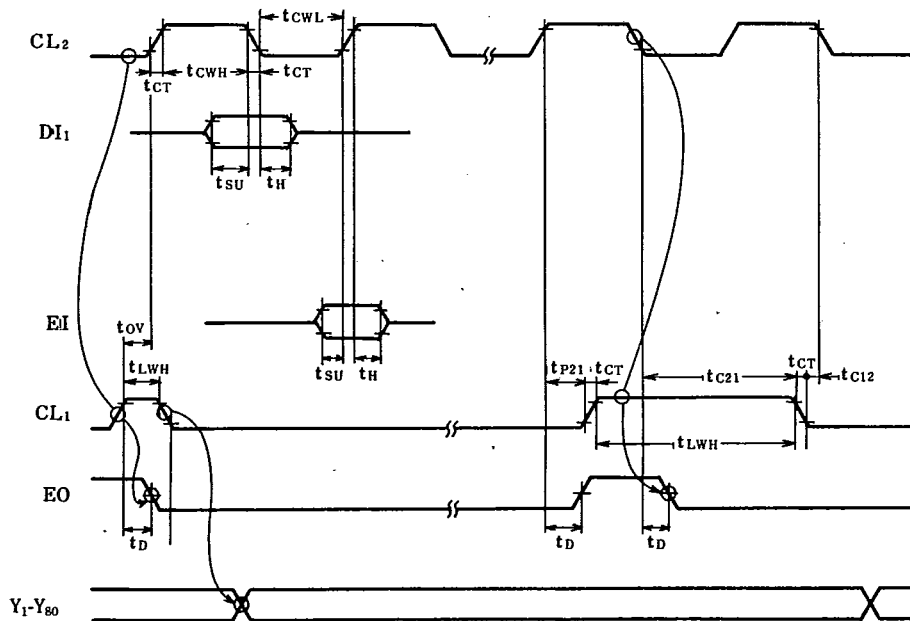
(V_{DD} = -5V ± 10%, V_{SS} = 0V, T_a = -20 to +70°C)

Parameter	Symbol	Conditions* ¹	MIN.	MAX.	Unit	Applicable pins
Clock frequency	t _c		380		ns	CL ₂
Clock "High" width	t _{cWH}		170		ns	CL ₂
Clock "Low" width	t _{cWL}		170		ns	CL ₁ , CL ₂
Data setup time	t _{SU}		70		ns	DI ₁ , EI
Data hold time	t _H		50		ns	DI ₁ , EI
Output delay	t _D	C _L = 15pF		230	ns	EO
Latch clock "High" width	t _{LWH}	LH5021B	140	*3	ns	CL ₁
		LH5022	130			
Clock margin time (from CL ₁ ↓ to CL ₂ ↓)	t _{C12}		20		ns	CL ₁ , CL ₂
Clock margin time* ² (from CL ₂ ↓ to CL ₁ ↓)	t _{C21}		200		ns	CL ₁ , CL ₂
Clock margin time (from CL ₂ ↑ to CL ₁ ↑)	t _{P21}		20		ns	CL ₁ , CL ₂
Clock ↑, ↓ time	t _{CT}			50	ns	CL ₁ , CL ₂
Overlap time of CL ₂ "Low" and CL ₁ "High"	t _{OV}		130		ns	CL ₁ , CL ₂

Test conditions

Input frequency : 0.8V_{DD}, 0.2V_{DD}; Input reference level : 0.8V_{DD}, 0.2V_{DD}; Output reference level : 0.2V_{DD}, 0.8V_{DD}*1 LH5021B : V_{EE} = -17V ± 1V, LH5022 : V_{EE} = -24V

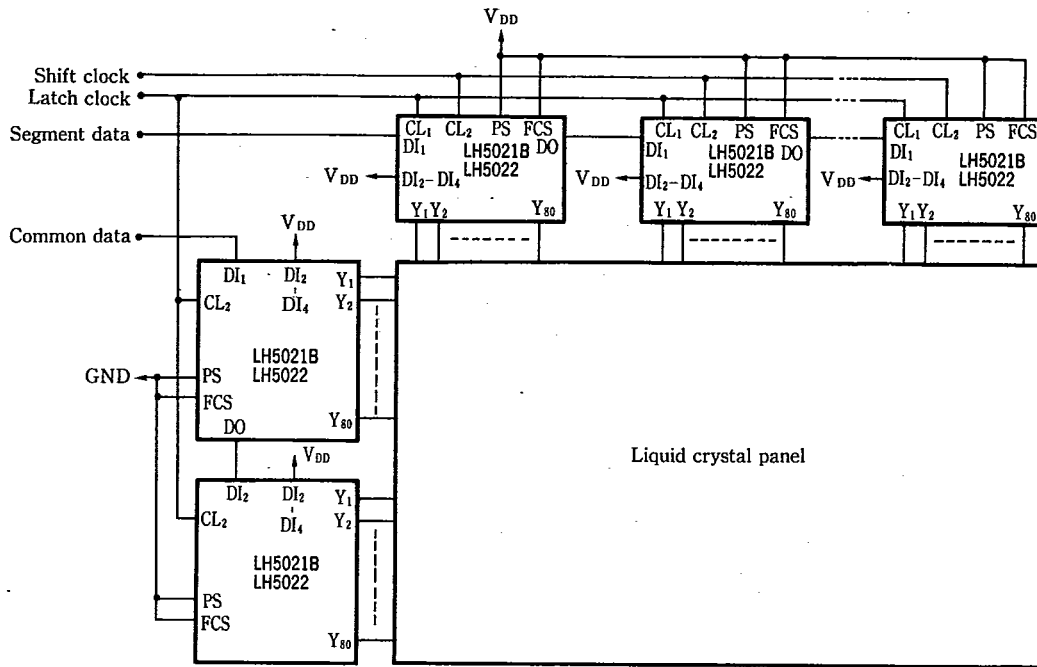
*2 Internal shift register valid time

*3 1.5t_c - t_{C12} - t_{P21} - 3t_{CT}

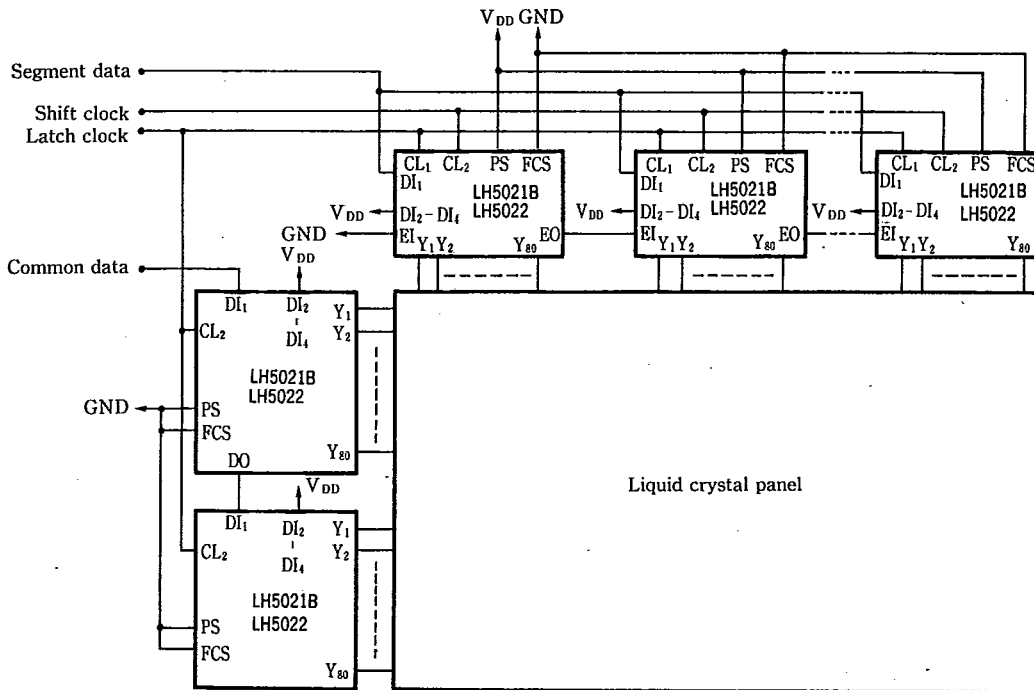
System Configuration Example

T-51-17

(1) 1-bit serial input segment driver and common driver



(2) 1-bit chip select segment driver and common driver



(3) 4-bit parallel input segment driver and common driver

