1. General Description

VVF3000 is a 16-bit general-purpose Digital Signal Processor (DSP) core designed for telecommunications and consumer electronics applications, and for low-power portable applications. Among the applications supported by VVF3000 are cellular telephones, digital cordless telephones, facsimile machines, and modems.

The VVS3001 development chip is based on the VVF3000 DSP core. It can be used for VVF3000-based hardware and software system development, and PINE In-Circuit-Emulator (PICE) operation.

VVF3000 is designed to be an engine for DSP-based application-specific ICs. It enables low-cost, low-power DSP processing with several levels of modularity in the RAM, ROM and I/O, permitting efficient DSP-based ASIC development. The core consists of the main blocks of a Central Processing Unit (CPU), including the ALU, multiplier, accumulators, RAM and ROM addressing units, and the program control logic. All other peripheral blocks, which are application-specific, are defined as part of the user-specific logic, implemented around the VVF3000 core on the same silicon die.

The VVF3000 has a balanced set of DSP and general microprocessor instructions to meet these requirements. The VVF3000 also features a wide range of operating voltages and user-defined amounts of RAM, ROM and registers.

The VVS3001 development chip includes the VVF3000 core, with maximal amount of internal RAM (2Kwords), and is operated with external ROM. It includes an on-chip wait state generator, clock generator and oscillator, and ROM protection logic. It also includes special program memory for test and evaluation (4 Kwords).

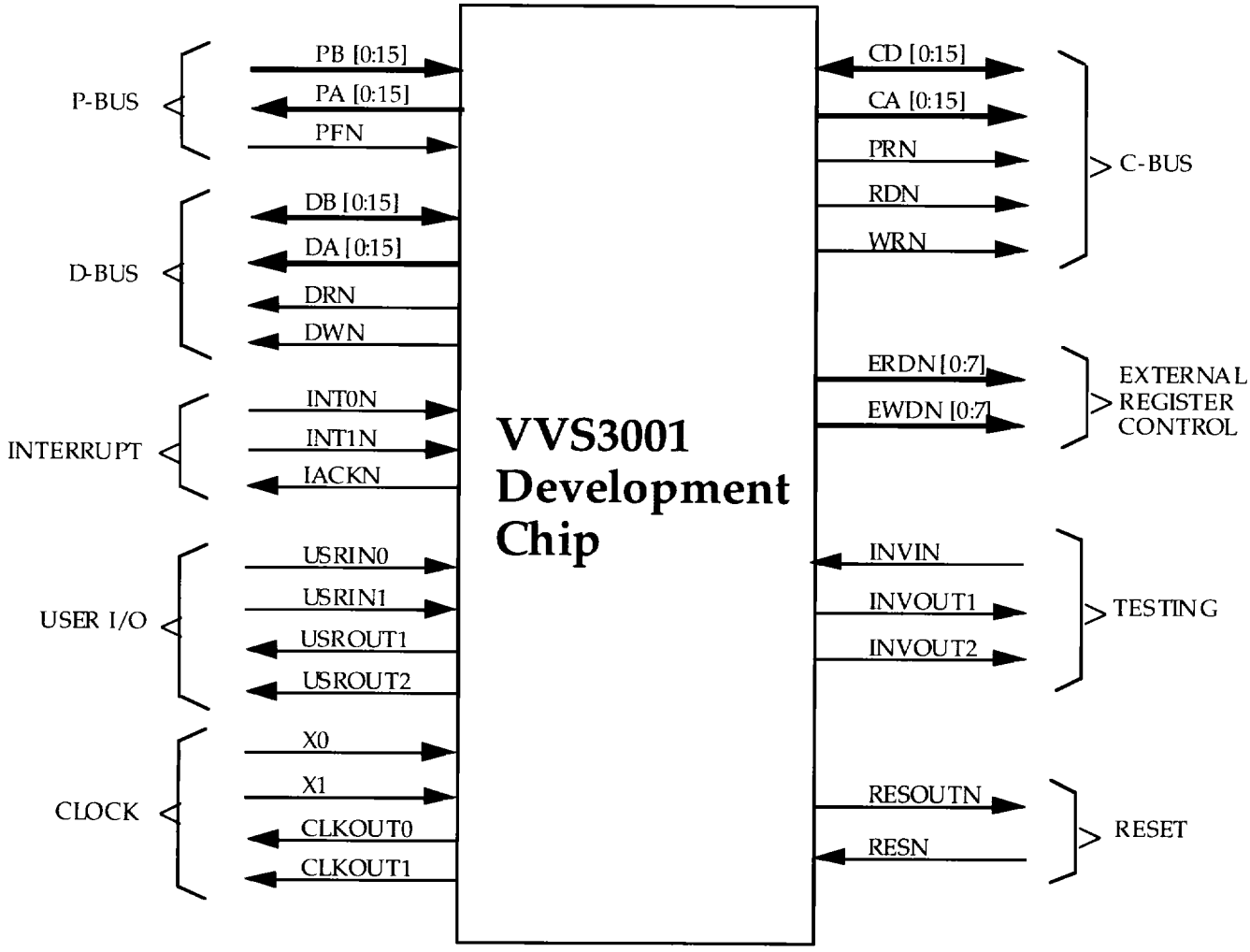


Figure 1: Functional Signal Groups

2. Features

2.1 Technology

- 0.6µ double metal CMOS technology
- A wide range of operating voltages: 2.7 - 5.5V
- 40ns cycle time @ 5V
- 180-pin Pin Grid Array (PGA) package

2.2 Architecture

- VVF3000 core
- 64 Kword Data memory space (RAM) - includes on-chip 2 Kwords of internal RAM
- 64 Kword Program memory space (ROM) - off-chip (4 Kwords of internal Devram)
- Programmable wait state generator
- Clock generator and oscillator
- ROM protection logic
- STOP and SLOW modes of operation for stopping the core or reducing clock speed respectively
- 17 stack levels
- Interrupts and exceptions
  - Reset
  - BPI (Break-Point Interrupt)
  - Two maskable interrupts
  - TRAP (software interrupt)

2.3 VVF3000 Core Features

- 16 x 16 bit 2's complement parallel multiplier with 32-bit product
- Single cycle multiply/accumulate instructions
- 36-bit ALU
- Two 36-bit accumulators
- Six general-purpose, 16-bit pointer-registers with two dedicated address arithmetic units for data memory indirect addressing, circular buffering, loop counters, and program memory indirect addressing
- Option for up to eight user-defined, 16-bit registers
- Zero Overhead Looping, REPEAT and BLOCK-REPEAT instructions with one nesting level
- Shifting capability
- Automatic saturation mode on overflow while reading content of accumulators
- Divide step support
- Normalize step support

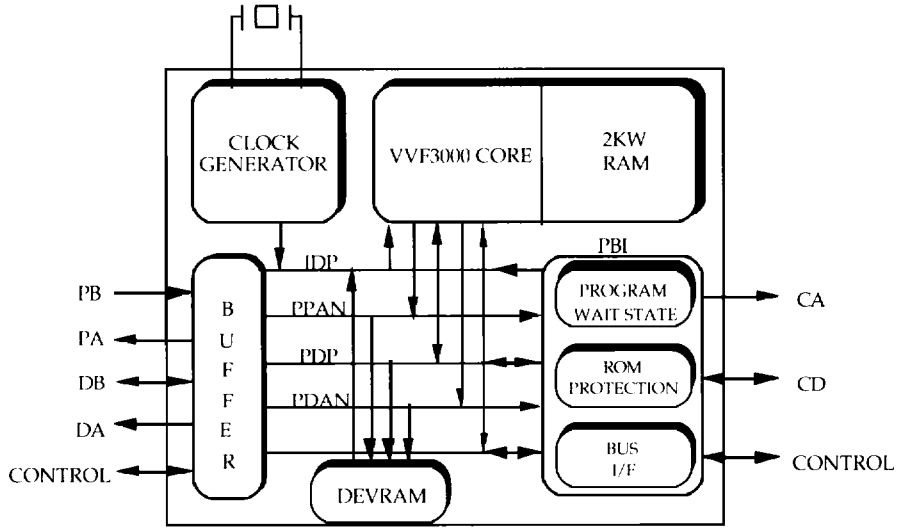


Figure 2: VVS3001 Development Chip Functional Block Diagram

Figure 3: Typical ASSP Prototype

3. General Description

The development chip includes the following modules: VVF3000 core, PBI (PINE Bus Interface), clock generator and I/O buffers.

3.1 VVF3000 Core

VVF3000 consists of three main execution units operating in parallel: the Computation Unit (CU), the Data Addressing Arithmetic Unit (DAAU) and the Program Control Unit (PCU). It has two banks of data RAM for parallel feeding of two inputs to the multiplier. The CU has a 16x16 multiplier, a 36-bit ALU, and two 36-bit accumulators. The VVF3000 programming model and instruction set are aimed at straightforward generation of efficient and compact code.

The pipeline method implements a three-level pipeline architecture, allowing instruction execution to overlap. Thus, the effective execution time for most instructions is one cycle. Each pipeline stage is completed before its result is needed by the next instruction.

(*) See detailed description in the VVF3000 data sheet.

3.2 Instruction Set

The following is a summary of the VVF3000 instruction set organized by instruction group. Most instructions are one-word instructions executed in a single cycle, except any instructions using a long immediate operand, which are two-word instructions and require two cycles.

3.2.1 Arithmetic and Logical Instructions

All arithmetic and logical instructions are single-cycle instructions except DIVS, NORM and any instruction using a long immediate operand.

ADD	Add
ADDH	Add to High Accumulator
ADDL	Add to Low Accumulator
AND	AND
CMP	Compare
DIVS	Division Step
MODA	Modify Accumulator Conditionally
CLR	Clear
CLRR	Clear and Round
COPY	Copy Other Accumulator
NEG	2's Complement
NOT	Logical Not
PACR	Product Move and Round
RND	Round
ROL	Rotate Left Through Carry
ROR	Rotate Right Through Carry
SHL	Shift Left
SHL4	Shift Left by 4
SHR	Shift Right
SHR4	Shift Right by 4
NORM	Normalize
OR	OR
SUB	Subtract
SUBH	Subtract from High Accumulator
SUBL	Subtract from Low Accumulator
XOR	Exclusive - OR

3.2.2 Multiply Instructions

All multiply instructions are single-cycle instructions except any instruction using a long immediate operand, which requires two cycles.

MPY	Multiply
MAC	Multiply and Accumulate Previous Product
MSU	Multiply and Subtract Previous Product
MPYS	Multiply Signed Short Immediate
SQR	Square
SQRA	Square and Accumulate Previous Product
SQRS	Square and Subtract Previous Product

3.2.3 Move Instructions

MOV is a single-cycle instruction. MOVP execution requires 3 cycles.

MOV	Move Date
MOVP	Move Program Memory

3.2.4 Loop Instructions

REP is a single-cycle instruction. BKREP execution requires 2 cycles.

BKREP	Block Repeat
REP	Repeat Next Instruction

3.2.5 Branch/Call Instructions

All branch/call instructions are 2-cycle instructions.

BR	Conditional Branch
BRR	Relative Conditional Branch
CALL	Conditional Call Subroutine
CALLR	Relative Conditional Call Subroutine
CALLA	Call Subroutine at Location Specified by the Accumulator
RET	Return Conditionally
RETI	Return from Interrupt

3.2.6 Control & Miscellaneous Instructions

All control instructions are single-cycle instructions, except TRAP, which is executed in 2 cycles.

DINT	Disable Interrupt
EINT	Enable Interrupt
LPG	Load the Page Bits
MODR	Modify Rn
NOP	No Operation
TRAP	Software Interrupt

3.3 PBI - PINE Bus Interface

This module includes the wait state generator, the bus interface unit which multiplexes the data and program buses, and bus transaction control. It consists of the external registers decoder and emulates the ROM protection of the internal PROM.

In addition, this unit includes memory-mapped registers for programming the system configuration (e.g. the wait states for each memory block).

3.3.1 Programmable Registers

Several addresses of the data memory space are reserved for system configuration and act like internal registers of the VVF3000 development chip. These addresses are memory mapped I/O.

This unit includes all the PBI programmable registers and associated logic to generate general signals needed by the PBI derived from the register contents (for details refer to the section on the PBI programming model).

3.3.2 Wait State Generator

VVF3000 is designed to interface with external memories and peripherals having different speeds, using a wait state mechanism. The wait state generator asserts wait states whenever needed, i.e. when the core issues requests for program or data transactions to/from slow devices, and whenever contention has occurred.

The following tables define the number of wait states asserted for each case when program fetches and data transactions are needed.

Program Fetch	Accessed Bus	Wait States
On-chip	P-bus	0 (no wait states for internal PROM)
Off-chip	C-bus	Programmable

Data Transfer	Accessed Bus	Wait States
On-chip	On-chip or D-bus	0 (no wait states for internal PROM)
Off-chip read	C-bus	Programmable
Off-chip write	C-bus	Programmable +1

Notes: Program on-chip means Program accessed through the P-bus
Program off-chip means Program accessed through the C-bus
Data on-chip means on-core / Data accessed through the D-bus
Data off-chip means Data accessed through the C-bus

3.3.3 Bus Interface Unit

The Bus Interface Unit (BIU) handles program and data transactions over the C-Bus. The unit supports:

- Control of off-chip program and data transactions
- Multiplexing of data/program address and data buses
- Contention resolution between concurrent off-chip data and program transactions

The first bus transaction over the C-bus is always determined according to the prioritized transaction type (data/program). Sometimes this transaction is a real transaction used by the core. Sometimes it is a dummy transaction (e.g. when external memory is not used, or when a non-prioritized memory type is used). The following table describes the transaction type performed in each cycle (data or program) and whether it is a dummy or a real cycle.

Priority	Ext. Prog. Fetch	Ext. Data Trans.	First Transaction Type	First Transaction Real/Dummy	Second Transaction Type	Second Transaction Real/Dummy
data	no	no	data	dummy	***	***
data	no	yes	data	real	***	***
data	yes	no	data	dummy	prog	real
data	yes	yes	data	real	prog	real
prog	no	no	prog	dummy	***	***
prog	no	yes	prog	dummy	data	real
prog	yes	no	prog	real	***	***
prog	yes	yes	prog	real	data	real

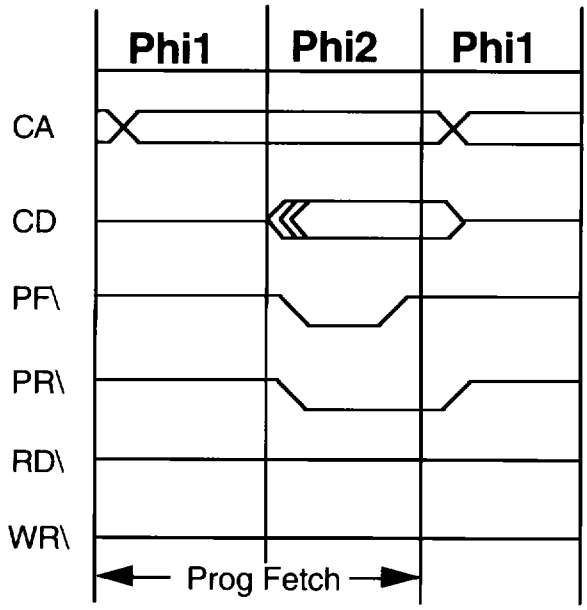
(***) - The cycle is not performed.

Notes:
1. The PBI will generate a dummy cycle even if the prioritized transaction type is for a Program address accessed through the P-bus or Data address accessed through the D-bus.
2. Dummy cycles with wait states (according to the PBI programming registers) are aborted after one cycle.

BIU operation examples are described in the following timing diagrams. For further information see the section on AC/DC characteristics.

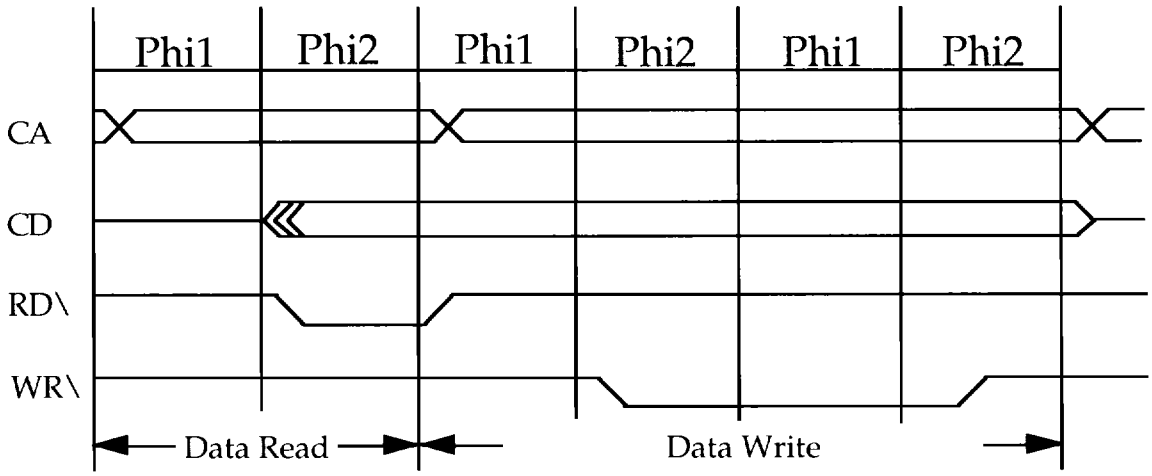
3.3.4 Off-Chip Program Fetch

When the core tries to fetch a program from off-chip memory via the C-bus, the BIU connects the internal program address and data buses to the C-Bus while issuing a PR\ signal. The following figure describes off-chip program fetch, where the program has priority over the data.



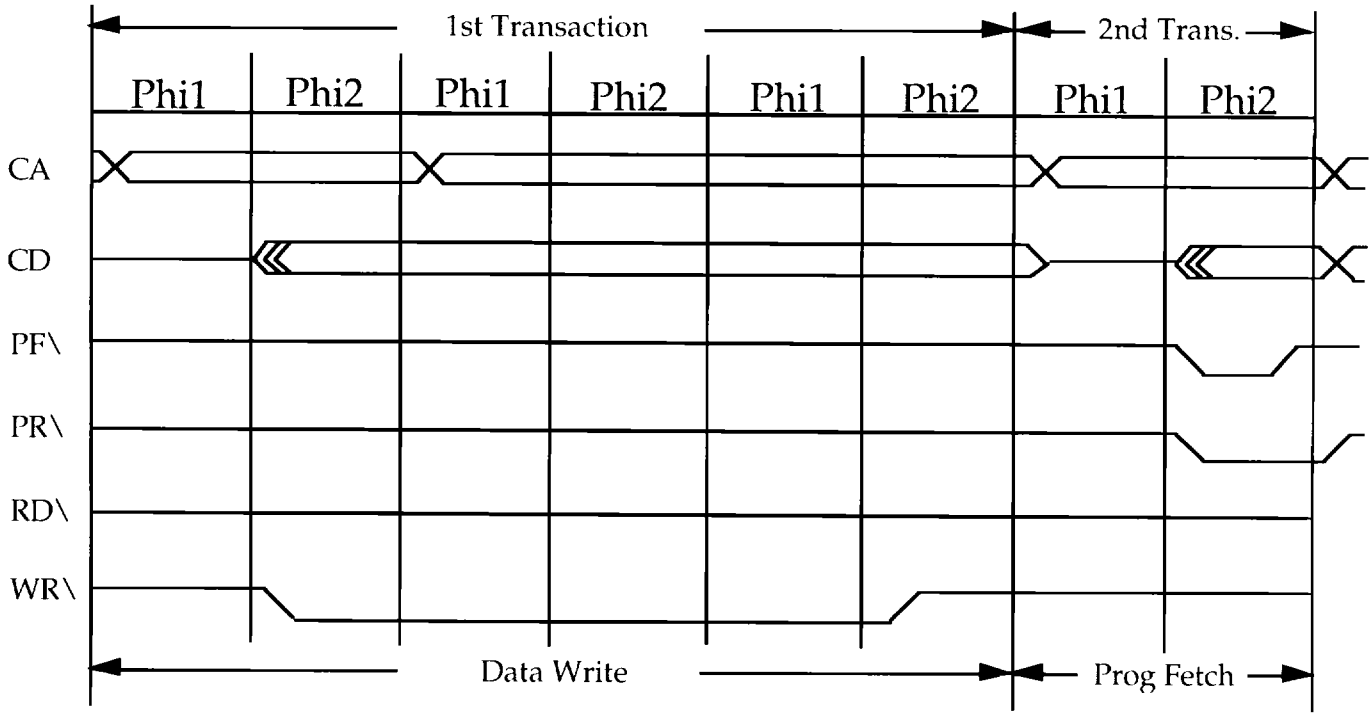
3.3.5 Off-Chip Data Transactions

When the core begins a data transaction, the BIU connects the internal data address and data buses to CA and CD, respectively. The BIU also issues a RD\ or WR\ (depending on the transaction direction). Note that the write cycle is one clock cycle longer than the read cycle. The following figure describes off-chip data read and write transactions, where data has priority over the program.



3.3.6 Contention Resolution

Contention occurs when both program and data are assigned access over the C-bus. When the BIU detects a contention, it performs the prioritized transaction first (dummy or real), and then starts the second transaction. The following diagram describes the signal timing, where data has priority over the program, the data has one wait state and the program has no wait state.



3.3.7 External Register Decoder

This unit generates individual read and write signals for each of the user-defined registers (External registers EXT0 - EXT7). These signals are multiplied by f2 at the I/O buffers module.

3.3.8 ROM Protection

The ROM protection mechanism is designed to protect the Program ROM (PROM) from being read without authorization. The VVF3000 development chip does not include any on-chip PROM. However, it emulates on-chip ROM of an application-specific VVF3000-based chip (COMBO). The first 28 Kwords of this ROM address space (0000-06FFFH) are protected from being read by an external program, connected to the multiplexed C-Bus.

3.3.9 Clock Generator

This module includes an internal oscillator, which generates the internal phases and CLKOUT signal. It has a programmable frequency divider for dividing the clock rate by 1 to 16 (SLOW mode), and for stopping the clock operation under a program control (STOP mode). It also generates reset signals for the chip and the RESOUTN signal.

3.3.10 I/O Buffers

The I/O drivers are TTL compatible.

3.4 Memory Organization

The memory configuration of the VVF3000 development chip is based on the VVF3000 core memory organization. The VVF3000 core supports two independent 64 Kword memory spaces: the program space (PROM) and the data space (XRAM and YRAM).

3.4.1 Program Memory

The VVF3000 core program memory space is 64 Kwords. The VVF3000 development chip uses external ROMs. Its program memory space can be configured in two ways, according to the PEXT input signal.

PEXT signal is low - Up to 32 Kword ROM (addresses 0000-07FFFH), zero wait-state access, on the P-Bus. This Program ROM emulates the on-chip ROM of an application-specific VVF3000-based chip (COMBO). Up to 32 Kword ROM (addresses 08000H-0FFFFH) with a programmable number of wait states (0 to 15). This ROM is accessed through the C-Bus (multiplexed program and data address space).

PEXT signal is high - Up to 64 Kword ROM with programmable number of wait-states (0 to 15). This ROM is accessed through the C-Bus (multiplexed program and data address space).

The program space starts at address 00010H. Addresses 0000H-0001H are used for Reset. Addresses 0008H-000FH are used for TRAP, BPI (breakpoint interrupt for debugging) and two maskable interrupts, respectively. Each interrupt address has been spaced apart by two locations so that branch instructions can be accommodated in those locations if desired. Addresses 0002H-0007H are reserved.

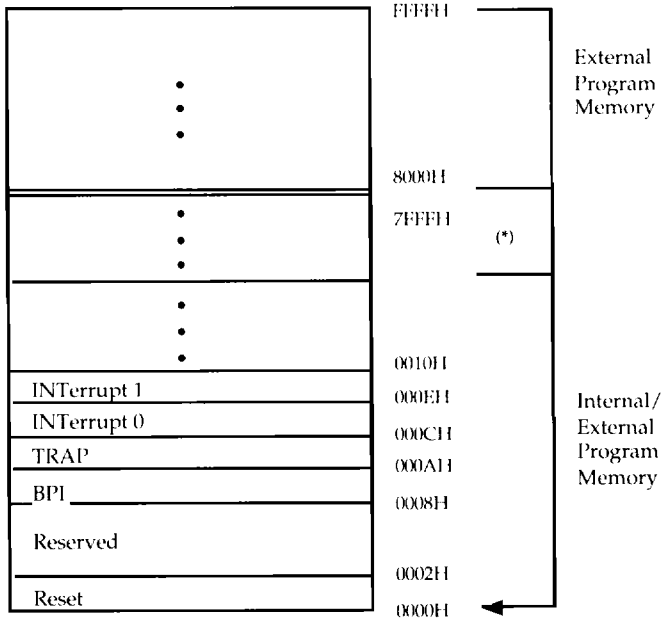


Figure 4: Program Memory Map

(*)The boundary between the internal/external program memory space is user definable, up to the limit of 32K words for the internal program memory space.

3.4.2 Data Memory

The VVF3000 core data memory space is 64 Kwords. The VVF3000 development chip includes 2 Kwords of on-chip RAM and supports up to 62 Kwords of external RAM.

The data space is divided into an X data space for the XRAM (from zero to 64511 [63K-1] 0000-0FBFFH) and a Y data space for the YRAM (from -1 to -1024). The data space range can also be considered as unsigned, in which case the YRAM space (0FC00H-0FFFFH) will be from 65,535 (64K) to 64512 (63K). The XRAM space has an internal space (on-chip data RAM/ROM) of 1K (0 to 1023) and an external space of 62K (1024 to 64,511 [63K-1]). The YRAM space is internal only.

The data memory space is divided into 8 blocks. Each block has 8 Kwords. The user must define for each block through which bus (D-bus or C-bus) the block will be accessed. Blocks accessed through the D-bus have zero wait-state access. Blocks accessed through the C-bus have a programmable number of wait-states (0 to 15).

The data RAM at addresses 0000H-03FFH and addresses 0FC00H-0FFFFH is implemented on-chip, as are the memory-mapped registers at addresses 0FBF0H-0FBFFH. These addresses are always zero wait-state access, regardless of the wait-states defined at the PBI registers. If the user needs more data space, external SRAM chips may be used.

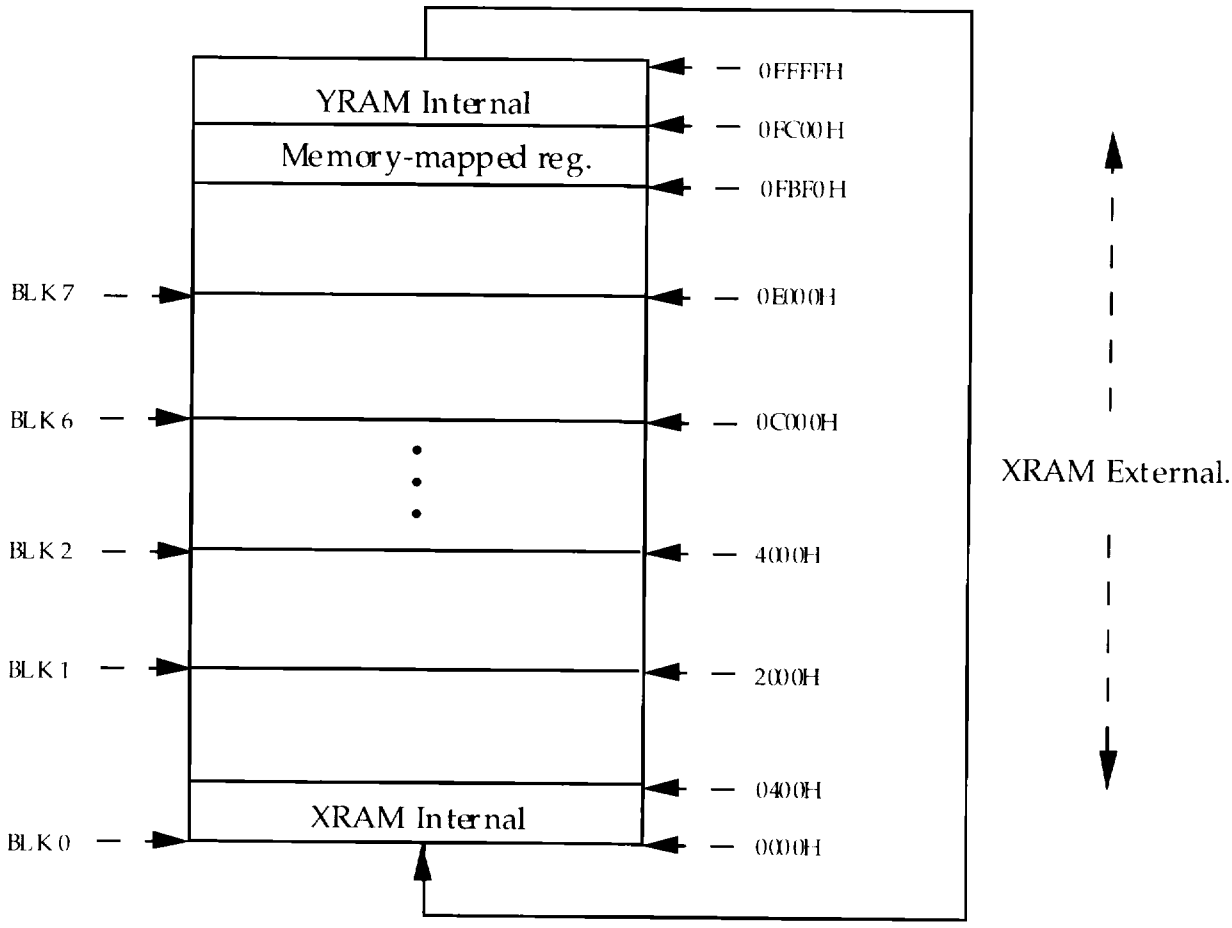


Figure 5: Data Memory Map

3.4.3 Program Devram Memory

3.4.3.1 VVF3000 Development Chip Special Devram Mode

Three pins are used as inputs to enable the Devram and control the on-chip memory. One output of the VVS3001 is used to switch the Devram from the data space after the program is loaded on-chip to the space in order to execute on-chip applications.

The pins are:

INVIN (G14)

INVOUT1 (F14)

INVOUT2 (E14)

USROUT0 (F13)

INVIN 0 => Enables Devram Mode (static signal).

1 => Standard Devchip.

In this mode, the VVS3001 is pin compatible with the devchip from DSP Group and can be used on the Pice Board or on the Pdkit. In this case, the DEVRAM is not visible.

INVOUT1 0 => Normal Mode.

1 => Stop the clock on the chip.

INVOUT2 0 => After the reset, this pin has to be 0. The Devram is seen as data memory on the pdp bus and can receive a program. The chip is on slow mode. It means that the on-chip clock is divided by 16.

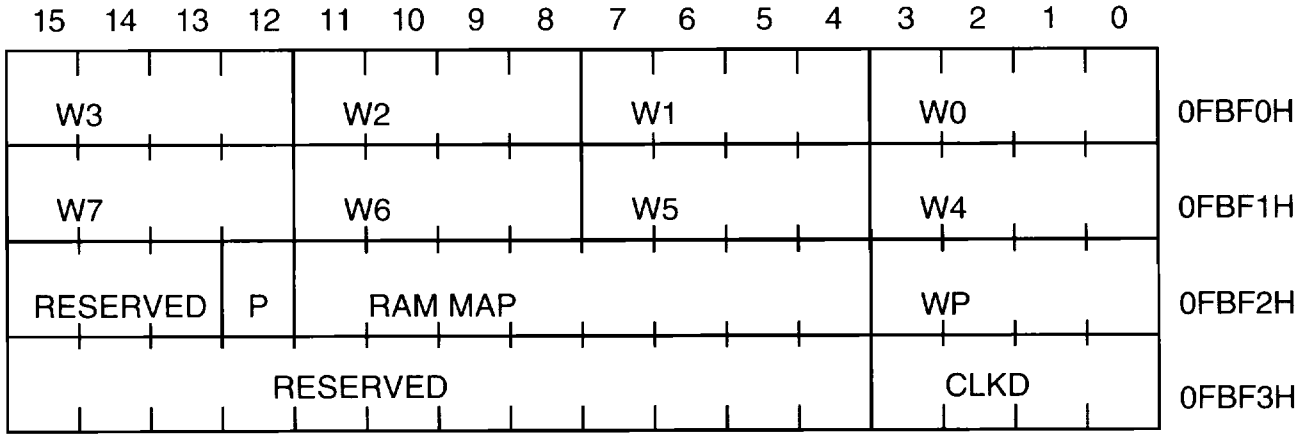
On our examples, we are using USROUT0 to control INVOUT2. After reset, USROUT0 is set to 0 and the VVF3000 can download code on the Devram. When the download phase is completed, the program has to change the polarity of USROUT0 by writing the correct value in the ST2 register. The clock division is bypass and the VVF3000 is fetching code from the Devram. External logic can be used to switch the Devram block from the pdp bus (data space) to the idp bus (program space).

3.4.3.2 Pice Board Modifications

On the Pice Board, we have connected the USROUT0 and INVOUT2 pins

3.5 PBI Programming Model

The PBI programming model consists of memory-mapped registers. These registers are used for setting the system configuration. The following figure describes the PBI registers, addresses and contents.



3.5.1 Field Descriptions

The following describes the different fields in the PBI registers. All bits are cleared at Reset except the reserved bits, which are undefined.

W0-W7 These 4-bit fields define the number of wait states the PBI will automatically generate when a data transaction is performed over the C-bus to the corresponding memory block, if assigned for access over C-bus by RAM MAP (See Figure 5).

RAM MAP Each bit in this 8-bit field defines the bus through which the block is accessed. '0' means access via the D-bus. '1' means access via the C-bus. LSB corresponds to block 0.

WP This 4-bit field defines the number of wait states the PBI generates when the core accesses off-chip PROM. (**)

P This bit defines the external C-bus transaction priority.

'0' means data priority. '1' means program priority.

CLKD This 4-bit field sets the division factor of the Clock Generator

0000 - 1

...

1111 - 16

RESERVED Write as don't care. Read as undefined.

(*) Data memory blocks mapping:

Block 0 0000H - 1FFFH
Block 1 2000H - 3FFFH
Block 2 4000H - 5FFFH
Block 3 6000H - 7FFFH
Block 4 8000H - 9FFFH
Block 5 0A000H - 0BFFFH
Block 6 0C000H - 0DFFFH
Block 7 0E000H - 0FFFFH

(**) Off-chip program ROM is defined as the ROM accessed through the multiplexed C-bus (address 08000H - 0FFFFH or address 0000H - 0FFFFH depending on the PEXT input pin value). Note that if the system configuration is defined as the first option, addresses 0000H-7FFFH have zero wait-state access).

3.6 Exceptions

3.6.1 Reset

Reset is a non-maskable interrupt that can be used at any time to put the VVF3000 into a known state. Reset is typically applied after power up when the machine is in a non-deterministic state. It is also used to exit STOP mode. When RESN signal is asserted, it initializes the clock generator. The signal rising edge initializes the PBI and the core (activating RESET signal to the core). This signal must be active low for at least 200ms. A reset out signal, RESOUTN, is generates by the RESN and internal reset signals. When the RESOUTN signal is de-asserted, the core reset is completed. When the core input RESET signal is deactivated, the core starts program execution from location 0000H. Reset affects various registers and status bits. However, when RESET is applied during STOP mode operation, the contents of the RAM and other registers are unaffected.

3.6.2 Interrupts

The VVF3000 core has three interrupts: two maskable interrupts (INT0 and INT1) and one non-maskable breakpoint interrupt (BPI). It also has one software interrupt (TRAP). The synchronized hardware interrupts are low level sensitive, and should be stable during CLKOUT high level.

Memory * Location	Interrupt Name & Function	Priority
0000H	RESET	1 highest
0008H	BPI External breakpoint interrupt	2
000AH	TRAP Software interrupt	3
000CH	INT0 External user interrupt0	4
000EH	INT1 External user interrupt1	5 lowest

* Start address for the interrupt/reset routine.

4. Pin Description

Signal Name	Pin Number	Type	Description
MEMORY BUSES AND CONTROL SIGNALS			
PA0	L8	O	Program address bus. PA15 (msb), PA0 (lsb). Reflects all program address transactions. Can be used for emulating on-chip program ROM of an application-specific VVF3000-based chip (COMBO).
PA1	M12	O	
PA2	N8	O	
PA3	N10	O	
PA4	N11	O	
PA5	N12	O	
PA6	N13	O	
PA7	P9	O	
PA8	P11	O	
PA9	P12	O	
PA10	P14	O	
PA11	R8	O	
PA12	R9	O	
PA13	R10	O	
PA14	R12	O	
PA15	R13	O	
PB0	C9	I	Program data bus. PB15 (msb), PB0 (lsb). This bus can be used for emulating on-chip program ROM of an application specific VVF3000-based chip (COMBO).
PB1	C10	I	
PB2	C11	I	
PB3	C12	I	
PB4	B10	I	
PB5	B11	I	
PB6	B13	I	
PB7	A9	I	
PB8	A11	I	
PB9	A12	I	
PB10	A13	I	
PB11	A14	I	
PB12	D10	I	
PB13	A15	I	
PB14	B15	I	
PB15	C15	I	
PFN	P10	O	Program fetch. This signal is active when performing program read, over P-bus or C-bus, at the end of the bus cycle.

Signal Name	Pin Number	Type	Description
DA0	C1	O	Data address bus. DA15 (msb), DA0 (lsb). Reflects all data address transactions. Can be used for emulating on-chip data address access of an application-specific VVF3000-based chip (COMBO).
DA1	N7	O	
DA2	N5	O	
DA3	P6	O	
DA4	P4	O	
DA5	R6	O	
DA6	R4	O	
DA7	M7	O	
DA8	R1	O	
DA9	M1	O	
DA10	K1	O	
DA11	N2	O	
DA12	L2	O	
DA13	N3	O	
DA14	L3	O	
DA15	M4	O	
DB0	K4	I/O	Data bus. DB15 (msb), DB0 (lsb). Valid during read/write from/to the off-core data memory addresses or during read/write from/to external registers. This bus is always output, except for read cycles from external registers or read memory over the D-bus.
DB1	H4	I/O	
DB2	F4	I/O	
DB3	G3	I/O	
DB4	E3	I/O	
DB5	E2	I/O	
DB6	H1	I/O	
DB7	F1	I/O	
DB8	A2	I/O	
DB9	A4	I/O	
DB10	A7	I/O	
DB11	B2	I/O	
DB12	B5	I/O	
DB13	B7	I/O	
DB14	C4	I/O	
DB15	C6	I/O	
DRN	D3	O	Data read. When low, this signal indicates that the processor is expecting data over the DB.
DWN	G2	O	Data write. When low, this signal indicates that the processor is writing data over the DB.

Signal Name	Pin Number	Type	Description
CA0	M9	O	Combo address. A multiplexed bus for data address and program address, where both memories emulate off-chip (external) memories.
CA1	N6	O	
CA2	N4	O	
CA3	P5	O	
CA4	P3	O	
CA5	R5	O	
CA6	R3	O	
CA7	M6	O	
CA8	P1	O	
CA9	L1	O	
CA10	J1	O	
CA11	M2	O	
CA12	K2	O	
CA13	M3	O	
CA14	K3	O	
CA15	L4	O	
CD0	J4	I/O	Combo data. A multiplexed bus for data read/write and program read, where both memories emulate off-chip (external) memories.
CD1	G4	I/O	
CD2	E4,E5	I/O	
CD3	F3	I/O	
CD4	F2	I/O	
CD5	D2	I/O	
CD6	G1	I/O	
CD7	E1	I/O	
CD8	A3	I/O	
CD9	A6	I/O	
CD10	A8	I/O	
CD11	B4	I/O	
CD12	B6	I/O	
CD13	C3	I/O	
CD14	C5	I/O	
CD15	C8	I/O	
PRN	D6	O	Program read. Active low output indicating program fetch through the C-bus.
RDN	D4	O	Data space. Active low output indicating data read from C-bus.
WRN	D5	O	Data write. Active low output indicating data write to C-bus.
PEXT	J12	I	External program. This input signal defines the program space mapping of the lower 32 kwords. When low, the lower 32 kwords are accessible using the P-bus. When high, all the 64 kwords are accessible using the C-bus. This signal should be stable during CLKOUT low level.

Signal Name	Pin Number	Type	Description
EXPANSION SUPPORT SIGNALS			
ERDN0	H13	O	External registers read. These signals indicate a read from the corresponding external register.
ERDN1	J13	O	
ERDN2	L13	O	
ERDN3	M13	O	
ERDN4	H14	O	
ERDN5	J14	O	
ERDN6	L14	O	
ERDN7	M14	O	
EWRN0	N14	O	External registers write. These signals indicate a write to the corresponding external register.
EWRN1	H15	O	
EWRN2	K15	O	
EWRN3	L15	O	
EWRN4	M15	O	
EWRN5	N15	O	
EWRN6	R15	O	
EWRN7	R14	O	
USROUT0	F13	O	User output pins. Discrete control signals that can be set/reset under software control (Bits 9,8 of ST2 register - OU1,OU0).
USROUT1	D12	O	
USRIN0	D13	I	User input signals. Discrete control signals that can be tested by the software (Bits 11,10 of ST2 register - IU1,IU0). These signals should be stable during CLKOUT low level.
USRIN1	E13	I	
EXCEPTION SIGNALS			
RESN	H12	I	Reset. When asserted, this signal initializes the clock generator. The signal rising edge initializes the core and the PBI. This signal must be active low for at least 200ms.
RESOUTN	G15	O	A reset out signal generated by the RESN and internal reset signals. When this signal is deactivated, the core reset is completed.
BPIN	H11	I	Break point interrupt. A synchronized, active low external interrupt request. This interrupt can not be masked. This signal should be stable during CLKOUT high level.
INT0N INT1N	F12 G12	I	Interrupt request. These signals are synchronized, active low external interrupt requests and can be internally masked. These signals should be stable during CLKOUT high.
IACKN	L12	O	Interrupt acknowledge. When low, this signal indicates the core is beginning to serve an interrupt request. The interrupt being serviced can be determined from the P-bus.
Signal Name	**Pin Number**	**Type**	**Description**

SUPPLY/ CLOCKS/ TESTING SIGNALS			
VCC	C2	P	Power supply pins
	H3	P	
	J3	P	
	P2	P	
	M5	P	
	R2	P	
	P7	P	
	M10	P	
	N9	P	
	P13	P	
	P15	P	
	K14	P	
	K12	P	
	B12	P	
	G13	P	
	D9	P	
	B9	P	
	E8	P	
	B8	P	
	A5	P	

GND	B1	P	Ground pins
	D1	P	
	H2	P	
	H5	P	
	J2	P	
	N1	P	
	R7	P	
	M8	P	
	M11	P	
	P8	P	
	R11	P	
	J15	P	
	K13	P	
	E12	P	
	C13	P	
	F15	P	
	D11	P	
	A10	P	
	D8	P	
	D7	P	
	C7	P	
	B3	P	
	A1	P	
CLKOUT0	E15	O	Clock out. These two pins should be shorted together externally.
CLKOUT1	D15		
XO	D14	O	Crystal out. Pin is used to connect crystal osc.
X1	C14	I	Crystal in. This pin is used to connect crystal osc. It can be used as an external clock input.
BYPASS	B14	I	Bypass mode. When this input is high, the clock division is bypassed. This signal should not be changed during operation.
INVIN	G14	I	These signals are used for testing.
INVOUT1	F14	I	
INVOUT2	E14	I	

5. Electrical Specifications

5.1 Absolute Maximum Ratings

Characteristic	Min.	Typ.	Max.	Unit
Operating free air temperature range	0		70	C
Storage temperature	-55		150	C
Vih high level input voltage			Vcc+0.5	V
Vil low level input voltage	-0.3			V

5.2 Recommended Operating Conditions

(Vcc = 5V +/- 10%)

Characteristic	Min.	Typ.	Max.	Unit
Vcc supply voltage	4.5	5	5.5	V
GND supply voltage		0		V
Vih high level input voltage	2.0			V
Vil low level input voltage		0	0.8	V

(Vcc = 3V +/- 10%)

Characteristic	Min.	Typ.	Max.	Unit
Vcc supply voltage	2.7	3.0	3.3	V
GND supply voltage		0		V
Vih high level input voltage	2.0			V
Vil low level input voltage		0	0.8	V

5.3 DC Characteristics

(Vcc = 5V +/- 10%)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIH	High level input voltage		2.0			V
	XI input		3.0			V
VIL	Low level input voltage				0.8	V
	XI input				0.3	V
VOH	High level output voltage	IOH = -400uA	2.4			V
VOL	Low level output voltage				0.5	V
	clkout (*)	IOH = 6mA			0.5	V
	all other outputs	IOH = 16mA				
IL	Input load current	0 =< VIN =< VCC	-20		20	uA
	Leakage current (output and I/O pins in hi-Z or input state)					
CIN	Input capacitance			6		pF
ICC	Active supply current	Ta = 25 deg C		100		mA
		VCC = 5V				
		f =25MHz				

(*) clkout means that pins CLKOUT0, CLKOUT1 should be shorted together externally.

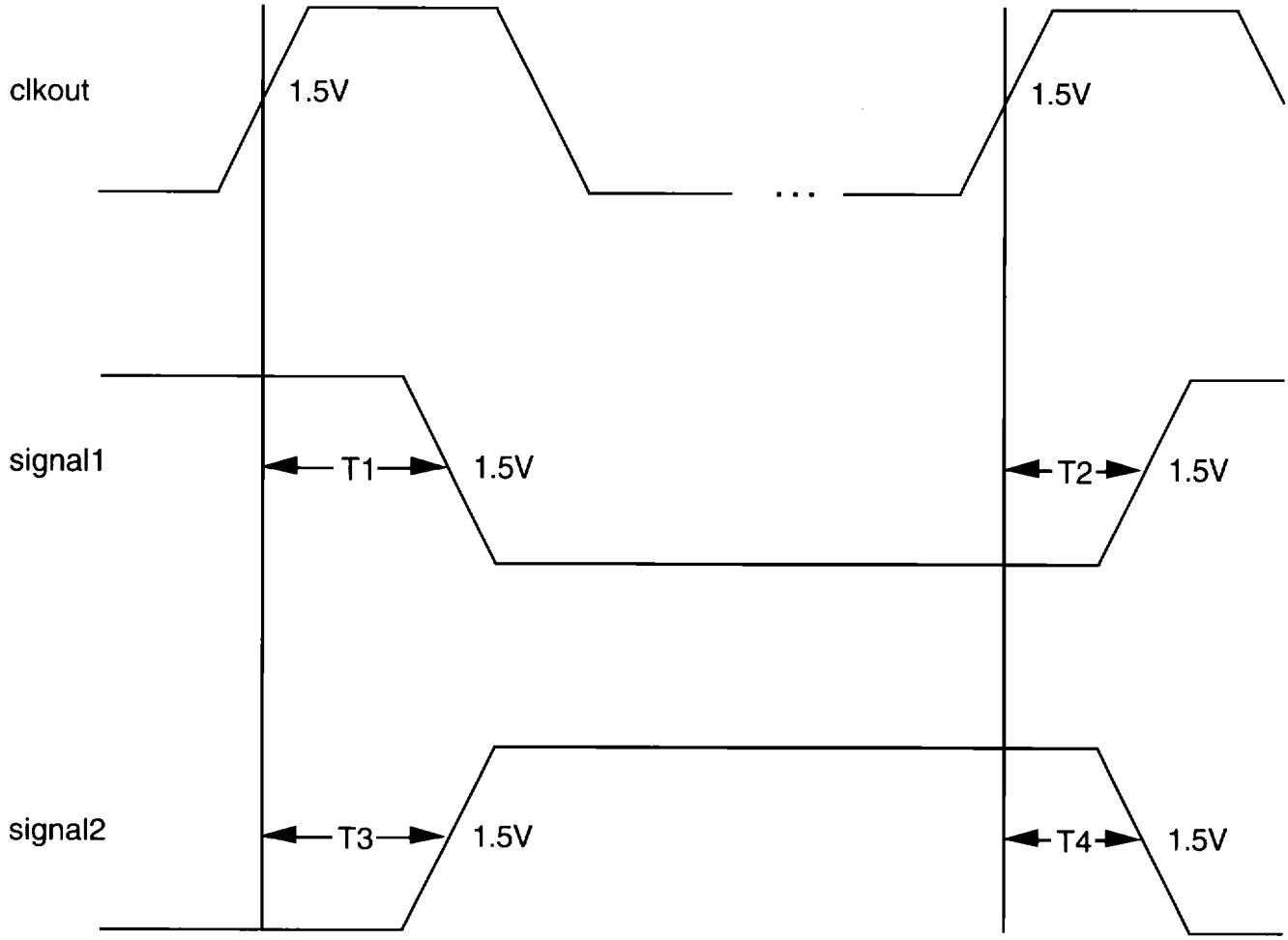
(Vcc = 3V +/- 10%)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIH	High level input voltage XI input		2.0 2.5			V V
VIL	Low level input voltage XI input				0.55 0.3	V V
VOH	High level output voltage	IOH = -400uA	2.0			V
VOL	Low level output voltage clkout (*) all other outputs	 IOH = 6mA IOH = 16mA			0.5 0.5	V V
IL	Input load current Leakage current (output and I/O pins in hi-Z or input state)	0 =< VIN =< VCC	-20		20	uA
CIN	Input capacitance			6		pF
ICC	Active supply current	Ta = 25 deg C VCC = 5V f =25MHz		30		mA

(*) clkout means that pins CLKOUT0, CLKOUT1 should be shorted together externally.

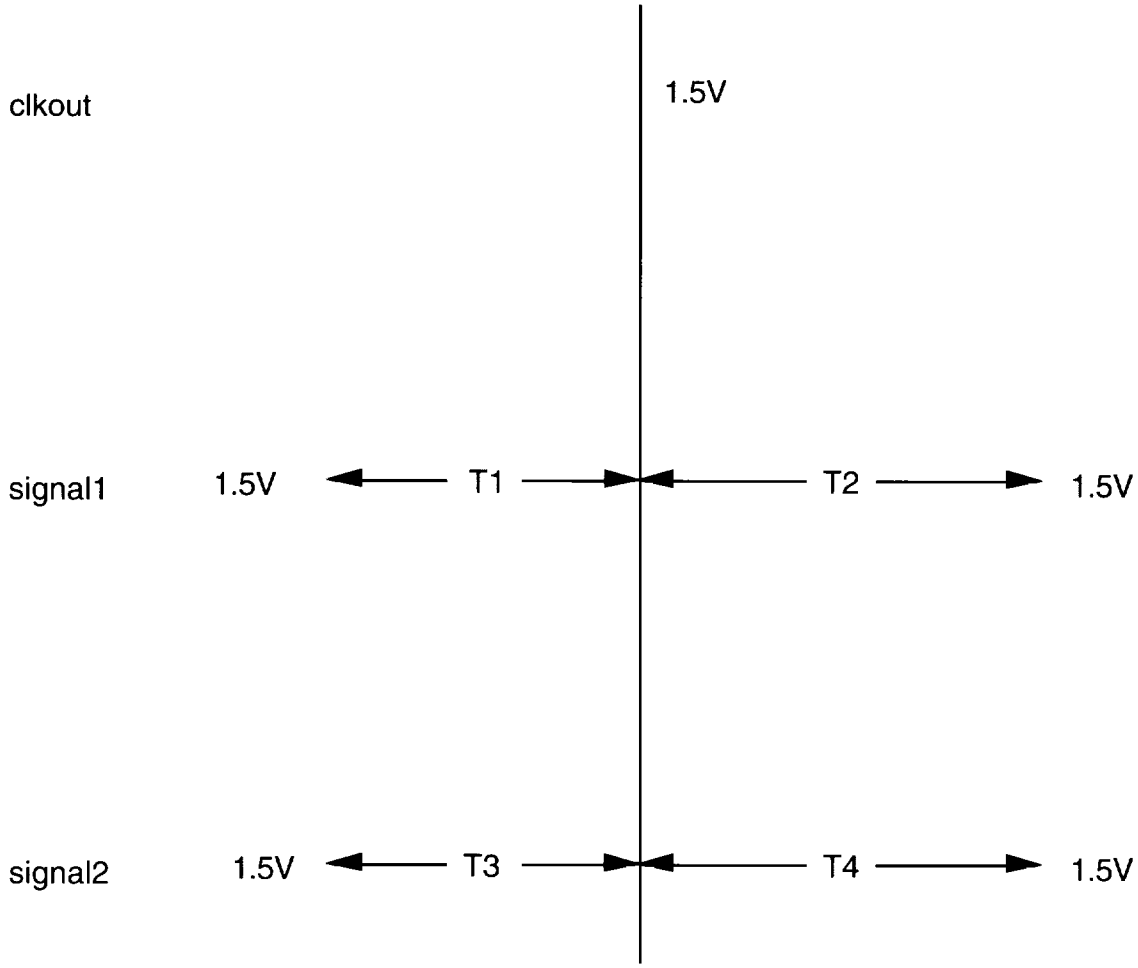
Notes:
All timing specifications given in this section refer to 1.5V on all the signals unless stated otherwise.
All timing parameters are given assuming a 100pF load on the CLKOUT signal.

Abbreviations:
LE Leading Edge
TE Trailing Edge.



T1 - signal1 valid time; T2 - signal1 hold time
T3 - signal2 valid time; T4 - signal2 hold time

Figure 6: Output Signals Specifications Standard



T1 - signal1 set-up time; T2 - signal1 hold time

T3 - signal2 set-up time; T4 - signal2 hold time

Figure 7: Input Signals Specification Standard

6. Timing Tables

6.1 Clocking and Reset

6.1.1 Oscillator

There are two basic clock oscillator configurations available as shown in Figure 8.

a. Crystal Controlled Oscillator XI and XO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 2N (N = 1 to 16, controlled by software).

Freq. Range	Rf	RI	C1	C2
10-40 MHz	10M	0	10pf	10pf

Freq. Range	Note
50-80 MHz	Internal memory access only.

b. External Oscillator XI is an external clock input signal. The external frequency is divided by 2N to give the instruction cycle time. XO is not used in this configuration and should not be loaded by any external load.

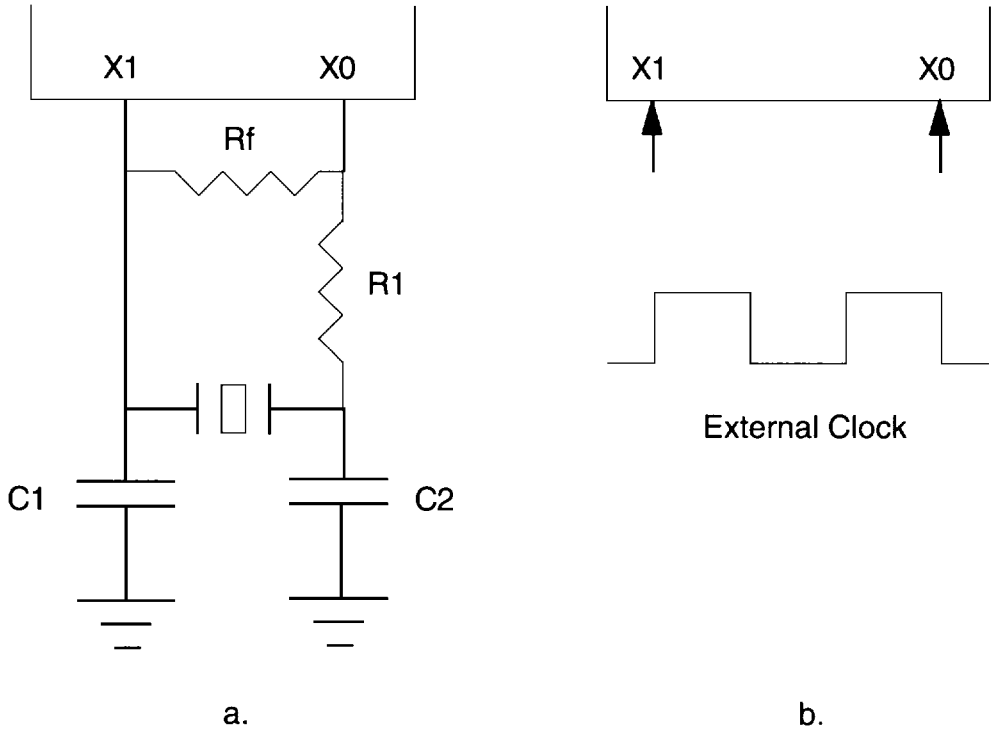


Figure 8: Clock Interface

6.1.2 Clock Out Timing Specifications

(Vcc = 5V +/- 10%)

Name	Diag.	Description	Reference/Conditions	Min.	Typ.	Max.	Units
Tclkoh	12	Clock out high time	From 1.5V LE CLKOUT to 1.5V of TE CLKOUT	1.7			ns
Tclkol	12	Clock out low time	From 1.5V TE CLKOUT to 1.5V of LE CLKOUT	2.9			ns
Tclkor	12	Clock out rise time	From 0.8V to 2.0V on LE CLKOUT				ns
Tclkof	12	Clock out fall time	From 2.0V to 0.8V on TE CLKOUT				ns
Tskr	12	Clock in to clock out rising skew	From VCC/2 LE XI to 1.5V LE of CLK-OUT				ns
Tskf	12	Clock in to clock out falling skew	From VCC/2 LE XI to 1.5V TE of CLK-OUT				ns

6.1.3 Clock Input Requirements

(Vcc = 5V +/- 10%)

Name	Diag.	Description	Reference/Conditions	Min.	Max.	Units
T	12	Clock in period	VCC/2 LE of XI to VCC/2 next LE	12.5		ns
tr	12	Clock in rise time	From 0.3V to 3.0V on LE XI		1.5	ns
tf	12	Clock in fall time	From 3.0V to 0.3V on TE XI		1.5	ns
th	12	Clock in high time	At 3.0V XI (both edges)	5.70		ns
tl	12	Clock in low time	At 0.3V XI (both edges)	5		ns

6.1.4 Reset (In and Out) Specifications

(Vcc = 5V +/- 10%)

Name	Diag.	Description	Reference/Conditions	Min.	Max.	Units
Tpwr	13	Power stable to TE of RESN	After VCC reaches 4.5V	150		ms
Trss	13, 14	RESN setup time	Before LE of clkout			ns
Trsw	14	RESN pulse width	At 1.5V both edges			ms
Trsov	14	RESOUTN valid time	After LE of resn		9.1	ns
Trsoh	13, 14	RESOUTN hold time	After LE of clkout	0		ns

6.1.5 Output Signals

(Vcc = 5V +/- 10%)

Name	Diag.	Description	Min.	Max.	Units
Tpav	1	Program address valid		7.5	ns
Tpah	1	Program address hold	0		ns
Tpfv	1	Program fetch valid		2.1	ns
Tpfh	1	Program fetch hold	0		ns
Tdav	2	Data address valid		7.9	ns
Tdah	2	Data address hold	0		ns
Tdrv	2	Data read valid		2.3	ns
Tdrh	2	Data read hold	0		ns
Tdwv	3	Data write valid		3.1	ns
Tdwh	3	Data write hold	0		ns
Terdv	10	External register read valid		2.1	ns
Terdh	10	External register read hold	0		ns
Tewrv	11	External register write valid		2.5	ns
Tewrh	11	External register write hold	0		ns
Tusrov		Usrout valid		4.5	ns
Tusroh		Usrout hold	0		ns
Tiackv		Interrupt acknowledge valid		2.7	ns
Tiackh		Interrupt acknowledge hold	0		ns
Tcav	4-9	Com. address valid		7.7	ns
Tcah	4-9	Com. address hold	0		ns
Tprv	4,5	Program read valid		2.7	ns
Tprh	4,5	Program read hold	0		ns
Trdv	6,7	Read valid		2.3	ns
Trdh	6,7	Read hold	0		ns
Twrv	8,9	Write valid		3.1	ns
Twrh	8,9	Write hold	0		ns
Tdbv	3	Data valid		14.3	ns
Tdbh	3,11	Data hold	0		ns
Tdbexv	11	Data valid for external registers		14.7	ns
Tdbf	2,10	Data floating			ns
Tdbnf	2,10	Data not floating			ns
Tcdv	8,9	Com. data valid		6.1	ns
Tcdh	8,9	Com. data hold	0		ns
Tcdf	4-9	Com. data floating			ns
Tcdnf	8,9	Com. data not floating			ns

6.1.6 Input Signal Requirements

(Vcc = 5V +/- 10%)

Name	Diag.	Description	Min.	Max.	Units
Tpbs	1	Program bus setup	9		ns
Tpbh	1	Program bus hold	0		ns
Tdbis	2,10	Data in setup	13.55		ns
Tdbih	2,10	Data in hold	0		ns
Tusris		USRIN0,1 setup	9.3		ns
Tusrih		USRIN0,1 hold	0		ns
Tbpis		BPI setup	9		ns
Tbpih		BPI hold	0		ns
Tints		INT0,1 setup	9		ns
Tinth		INT0,1 hold	0		ns
Tcdis	4-7	Com. data in setup	8		ns
Tcdih	4-7	Com. data in hold	0		ns
Tpexts		PEXT setup	9		ns
Tpexth		PEXT hold	0		ns

6.2 Timing Diagrams

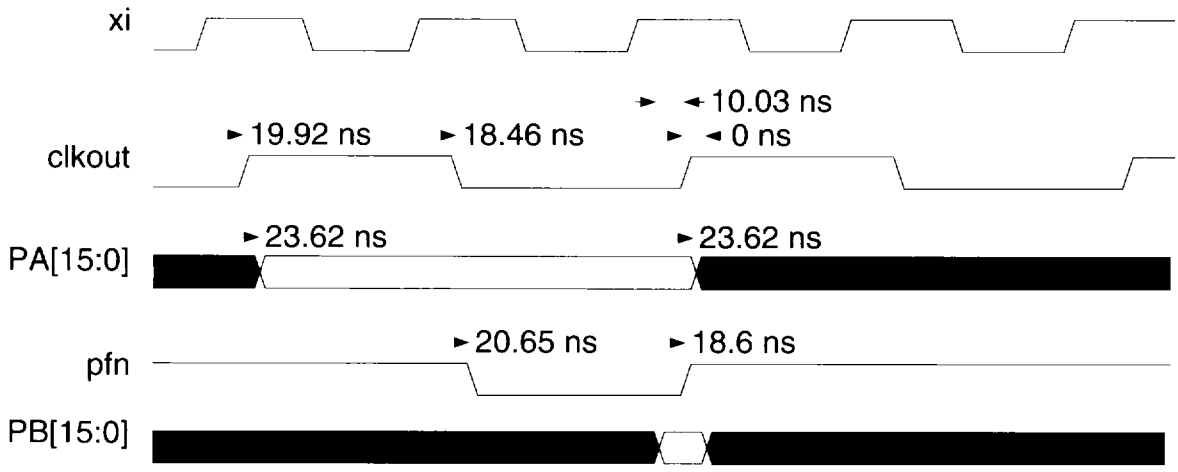


Diagram 1. Program Read pb Bus

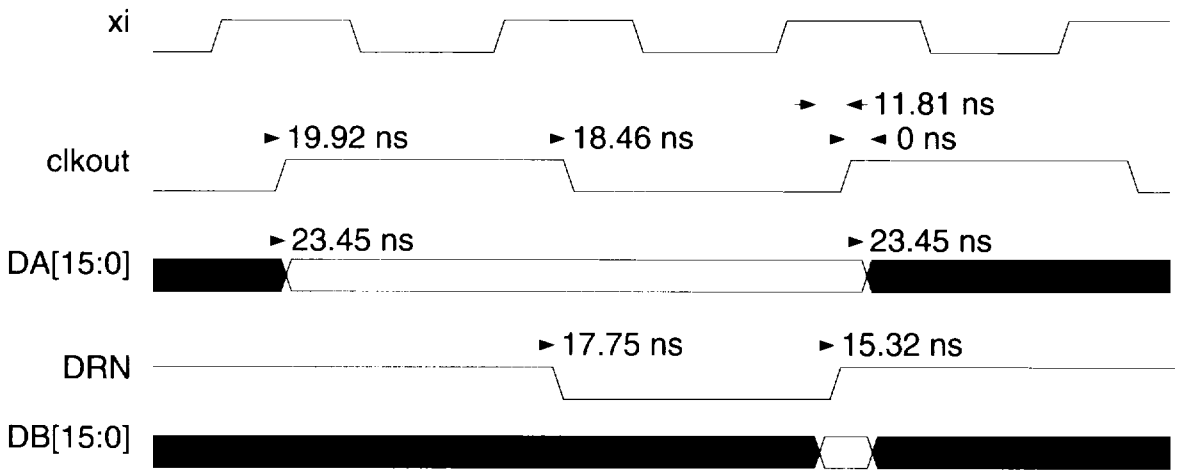


Diagram 2. Data Read db Bus

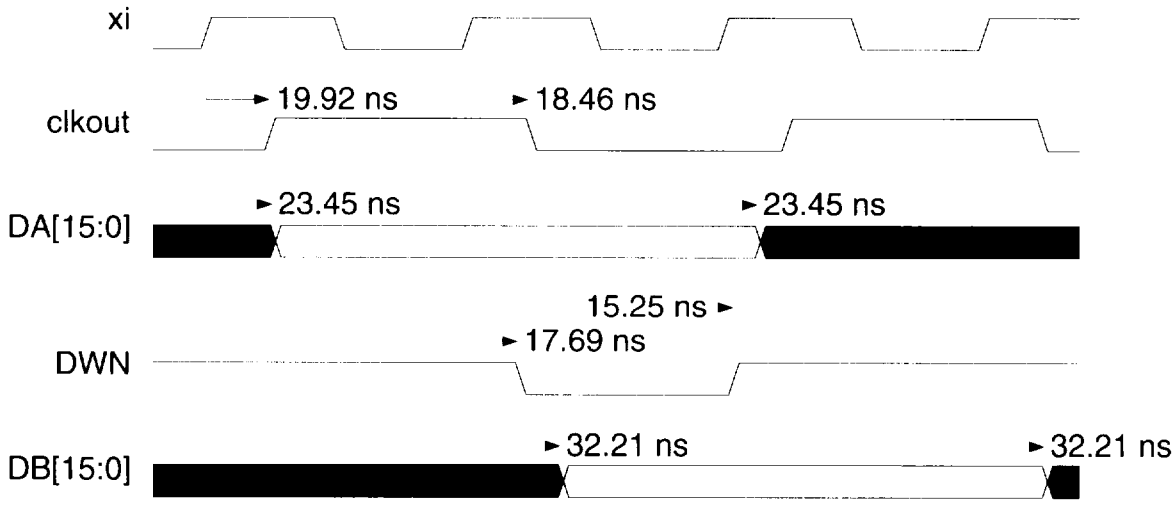


Diagram 3: Data Write db BUS

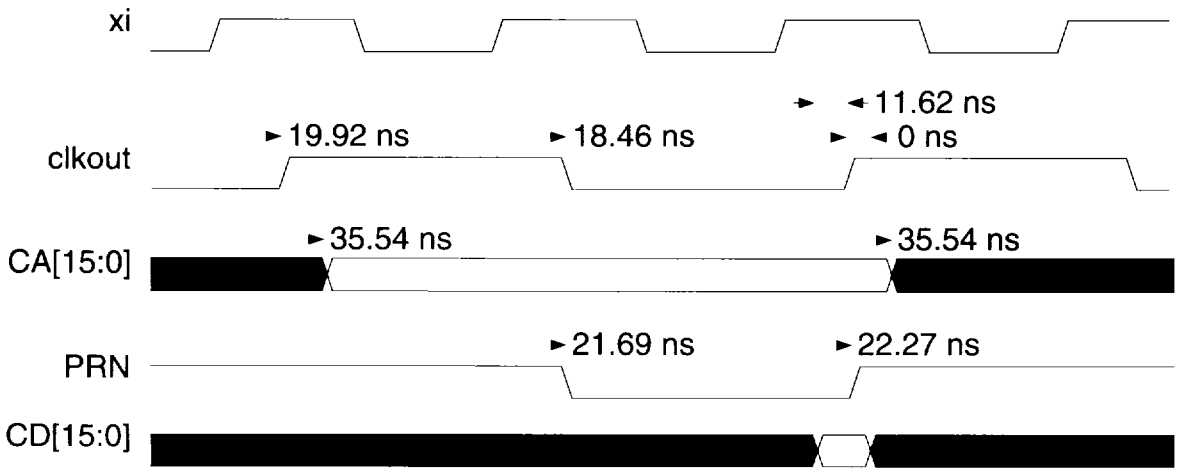


Diagram 4. Program Read cd Bus (No Wait States)

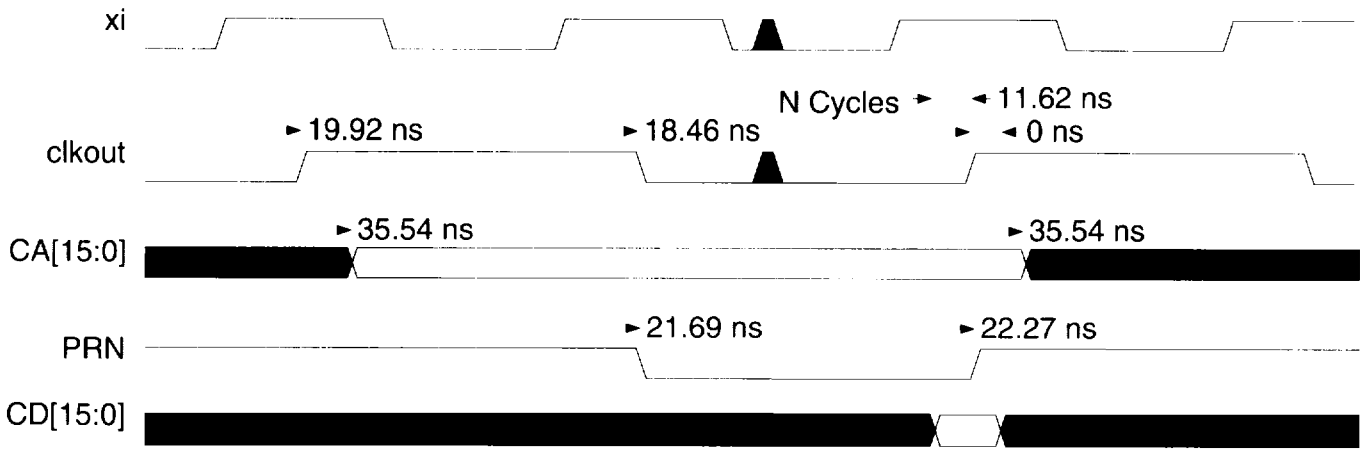


Diagram 5. Program Read cd Bus (N Wait States)

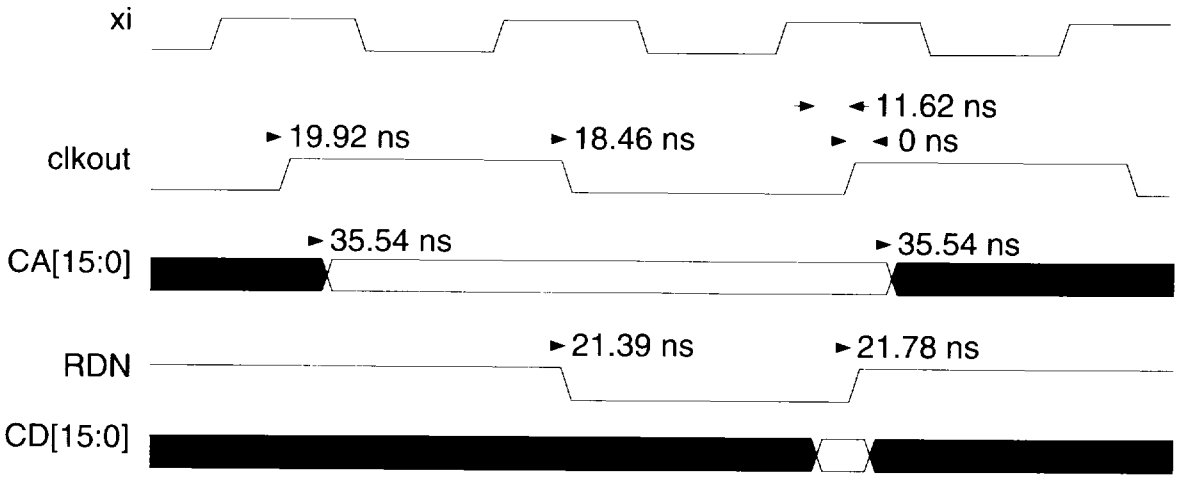


Diagram 6. Data Read cd Bus (No Wait States)

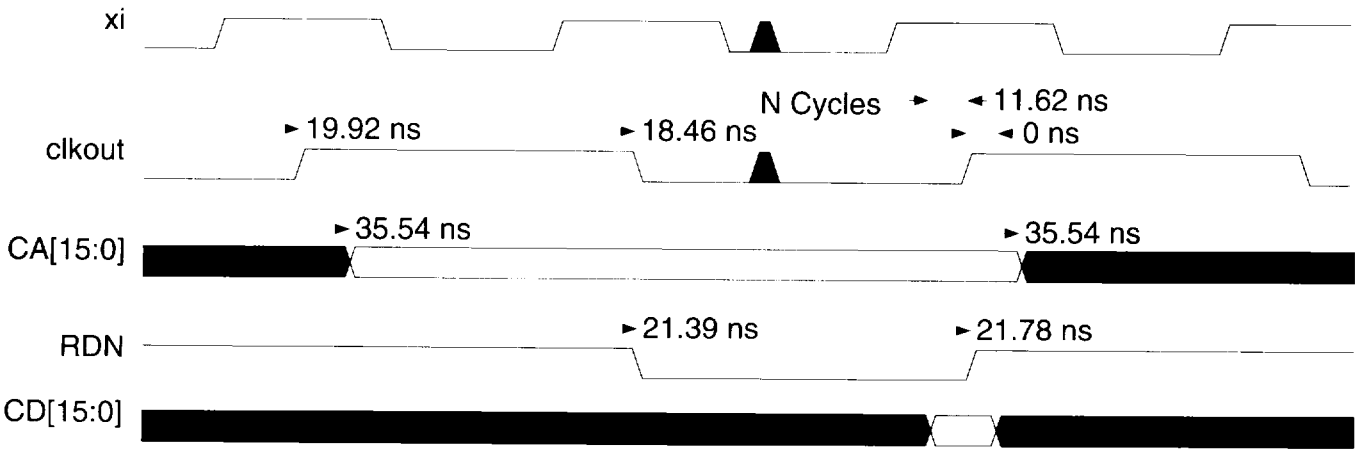


Diagram 7. Data Read cd Bus (N Wait States)

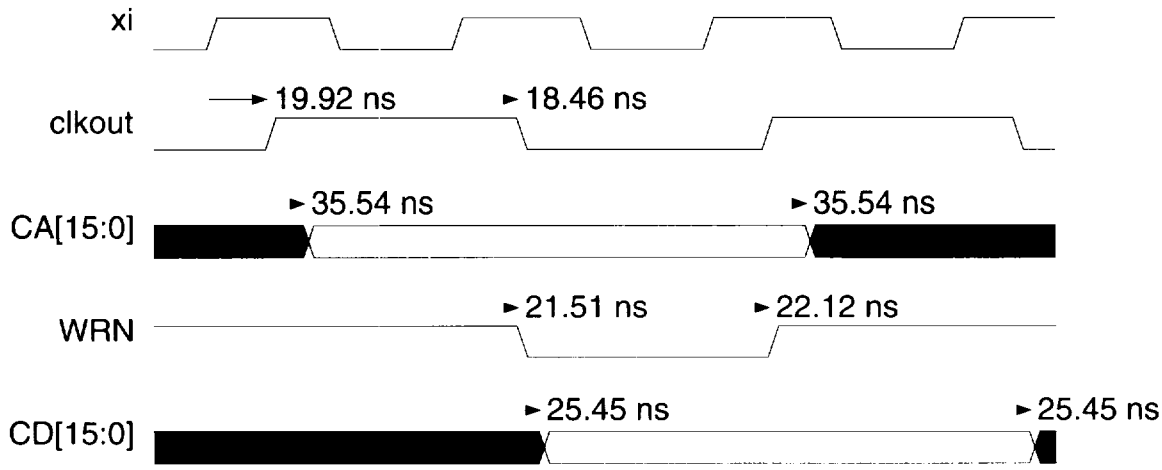


Diagram 8. Data Write cd Bus (No Wait States)

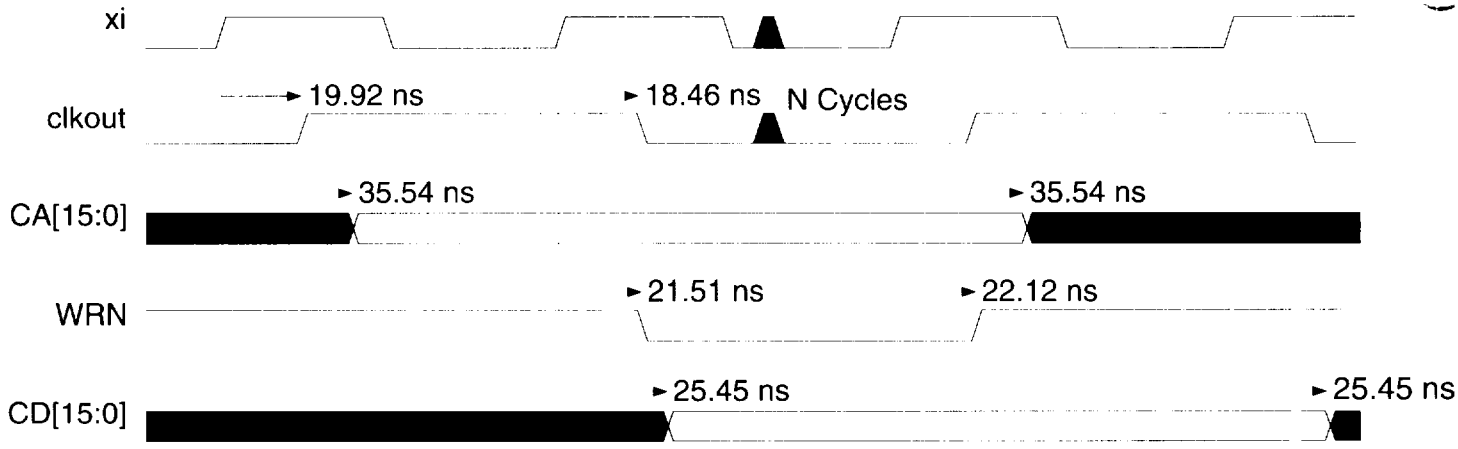


Diagram 9. Data Write cd Bus (N Wait States)

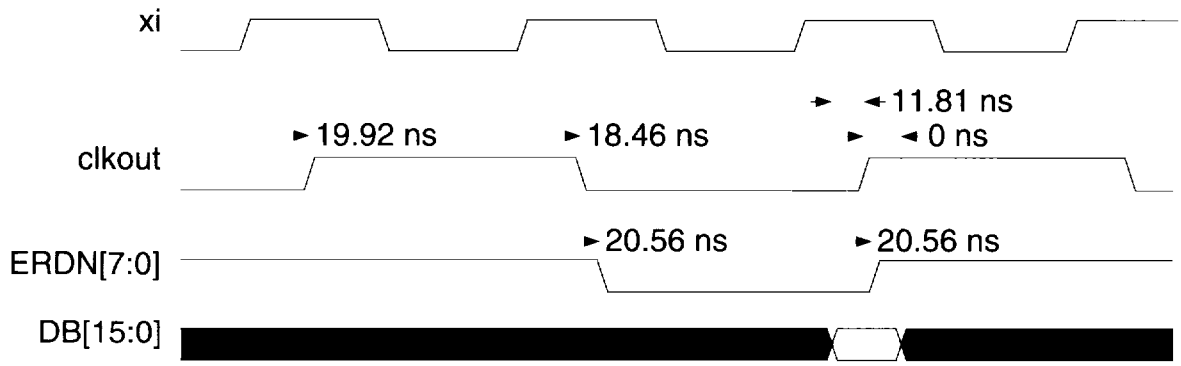


Diagram 10. External Register Read

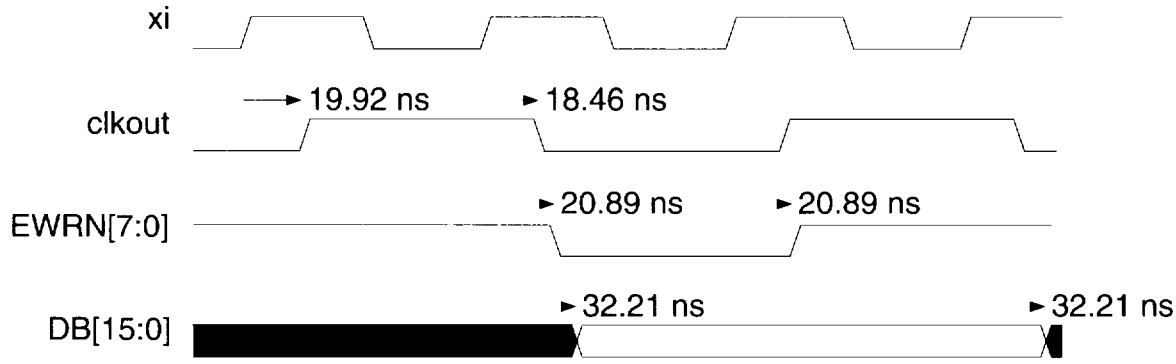


Diagram 11. External Register Write

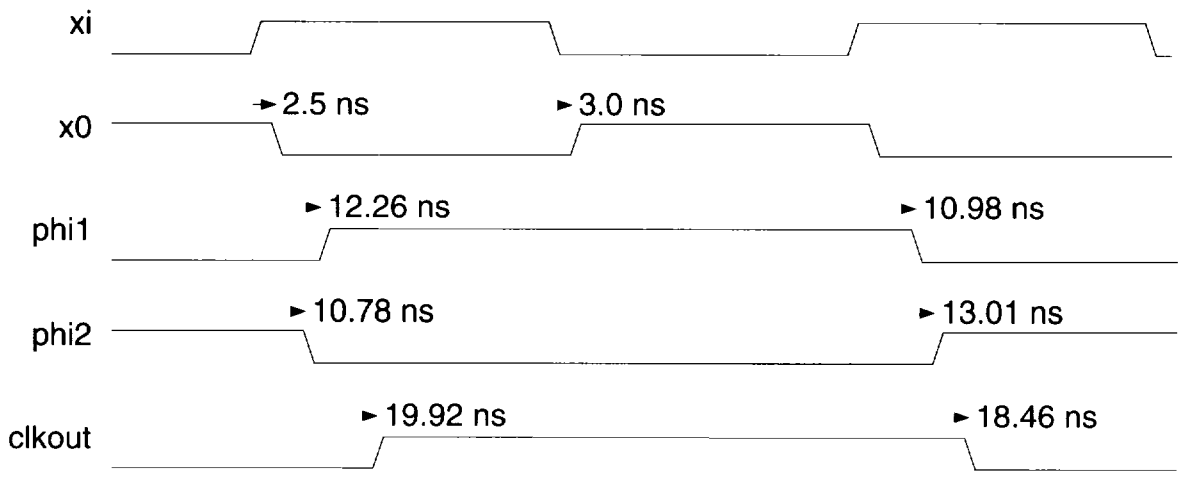


Diagram 12. Clock Waveforms

7. Package and Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	DA8	VDD	CA6	DA6	CA5	DA5	VSS	PA11	PA12	PA13	VSS	PA14	PA15	EWRN7	EWRN6
P	CA8	VDD	CA4	DA4	CA3	DA3	VDD	VSS	PA7	PFN	PA8	PA9	VDD	PA10	VDD
N	VSS	DA11	DA13	CA2	DA2	CA1	DA1	PA2	VDD	PA3	PA4	PA5	PA6	EWRN0	EWRN5
M	DA9	CA11	CA13	DA15	VDD	CA7	DA7	VSS	CA0	VDD	VSS	PA1	ERDN3	ERDN7	EWRN4
L	CA9	DA12	DA14	CA15				PA0				IACKN	ERDN2	ERDN6	EWRN3
K	DA10	CA12	CA14	DB0								VDD	VSS	VDD	EWRN2
J	CA10	VSS	VDD	CD0								PEXT	ERDN1	ERDN5	VSS
H	DB6	VSS	VDD	DB1	VSS						BPIN	RESN	ERDN0	ERDN4	EWRN1
G	CD6	DWN	DB3	CD1								INTIN	VDD	INVIN	RESOUT
F	DB7	CD4	CD3	DB2								INTON	USROUT0	INVOUT1	VSS
E	CD7	DB5	DB4	CD2	CD2			VDD				VSS	USRIN1	INVOUT2	CLKOUT0
D	VSS	CD5	DRN	RDN	WRN	PRN	VSS	VSS	VDD	PB12	VSS	USROUT1	USRIN0	X0	CLKOUT1
C	DA0	VDD	CD13	DB14	CD14	DB15	VSS	CD15	PB0	PB1	PB2	PB3	VSS	XI	PB15
B	VSS	DB11	VSS	CD11	DB12	CD12	DB13	VDD	VDD	PB4	PB5	VDD	PB6	BYPASS	PB14
A	VSS	DB8	CD8	DB9	VDD	CD9	DB10	CD10	PB7	VSS	PB8	PB9	PB10	PB11	PB13

dsp bottom xy	signal name
A1	VSS
A2	DB8
A3	CD8
A4	DB9
A5	VDD
A6	CD9
A7	DB10
A8	CD10
A9	PB7
A10	VSS
A11	PB8
A12	PB9
A13	PB10
A14	PB11
A15	PB13
B1	VSS
B2	DB11
B3	VSS
B4	CD11
B5	DB12
B6	CD12
B7	DB13
B8	VDD
B9	VDD
B10	PB4
B11	PB5
B12	VDD
B13	PB6
B14	BYPASS
B15	PB14
C1	DA0
C2	VDD
C3	CD13
C4	DB14
C5	CD14
C6	DB15
C7	VSS
C8	CD15

dsp bottom xy	signal name
E1	CD7
E2	DB5
E3	DB4
E4	CD2
E5	NC
E6	
E7	
E8	VDD
E9	
E10	
E11	
E12	VSS
E13	USRIN1
E14	INVOUT2
E15	CLKOUT0
F1	DB7
F2	CD4
F3	CD3
F4	DB2
F5	
F6	
F7	
F8	
F9	
F10	
F11	
F12	INTON
F13	USROUT0
F14	INVOUT1
F15	VSS
G1	CD6
G2	DWN
G3	DB3
G4	CD1
G5	
G6	
G7	
G8	

dsp bottom xy	signal name
J1	CA10
J2	VSS
J3	VDD
J4	CD0
J5	
J6	
J7	
J8	
J9	
J10	
J11	
J12	PEXT
J13	ERDN1
J14	ERDN5
J15	VSS
K1	DA10
K2	CA12
K3	CA14
K4	DB0
K5	
K6	
K7	
K8	
K9	
K10	
K11	
K12	VDD
K13	VSS
K14	VDD
K15	EWRN2
L1	CA9
L2	DA12
L3	DA14
L4	CA15
L5	
L6	
L7	
L8	PA0

dsp bottom xy	signal name
N1	VSS
N2	DA11
N3	DA13
N4	CA2
N5	DA2
N6	CA1
N7	DA1
N8	PA2
N9	VDD
N10	PA3
N11	PA4
N12	PA5
N13	PA6
N14	EWRN0
N15	EWRN5
P1	CA8
P2	VDD
P3	CA4
P4	DA4
P5	CA3
P6	DA3
P7	VDD
P8	VSS
P9	PA7
P10	PFN
P11	PA8
P12	PA9
P13	VDD
P14	PA10
P15	VDD
R1	DA8
R2	VDD
R3	CA6
R4	DA6
R5	CA5
R6	DA5
R7	VSS
R8	PA11

dsp

bottom	signal
C9	PB0
C10	PB1
C11	PB2
C12	PB3
C13	VSS
C14	XI
C15	PB15
D1	VSS
D2	CD5
D3	DRN
D4	RDN
D5	WRN
D6	PRN
D7	VSS
D8	VSS
D9	VDD
D10	PB12
D11	VSS
D12	USROUT1
D13	USRIN0
D14	X0
D15	CLKOUT1

dsp

bottom	signal
G9	
G10	
G11	
G12	INTIN
G13	VDD
G14	INVIN
G15	RESOUT
H1	DB6
H2	VSS
H3	VDD
H4	DB1
H5	VSS
H6	
H7	
H8	
H9	
H10	
H11	BPIN
H12	RESN
H13	ERDN0
H14	ERDN4
H15	EWRN1

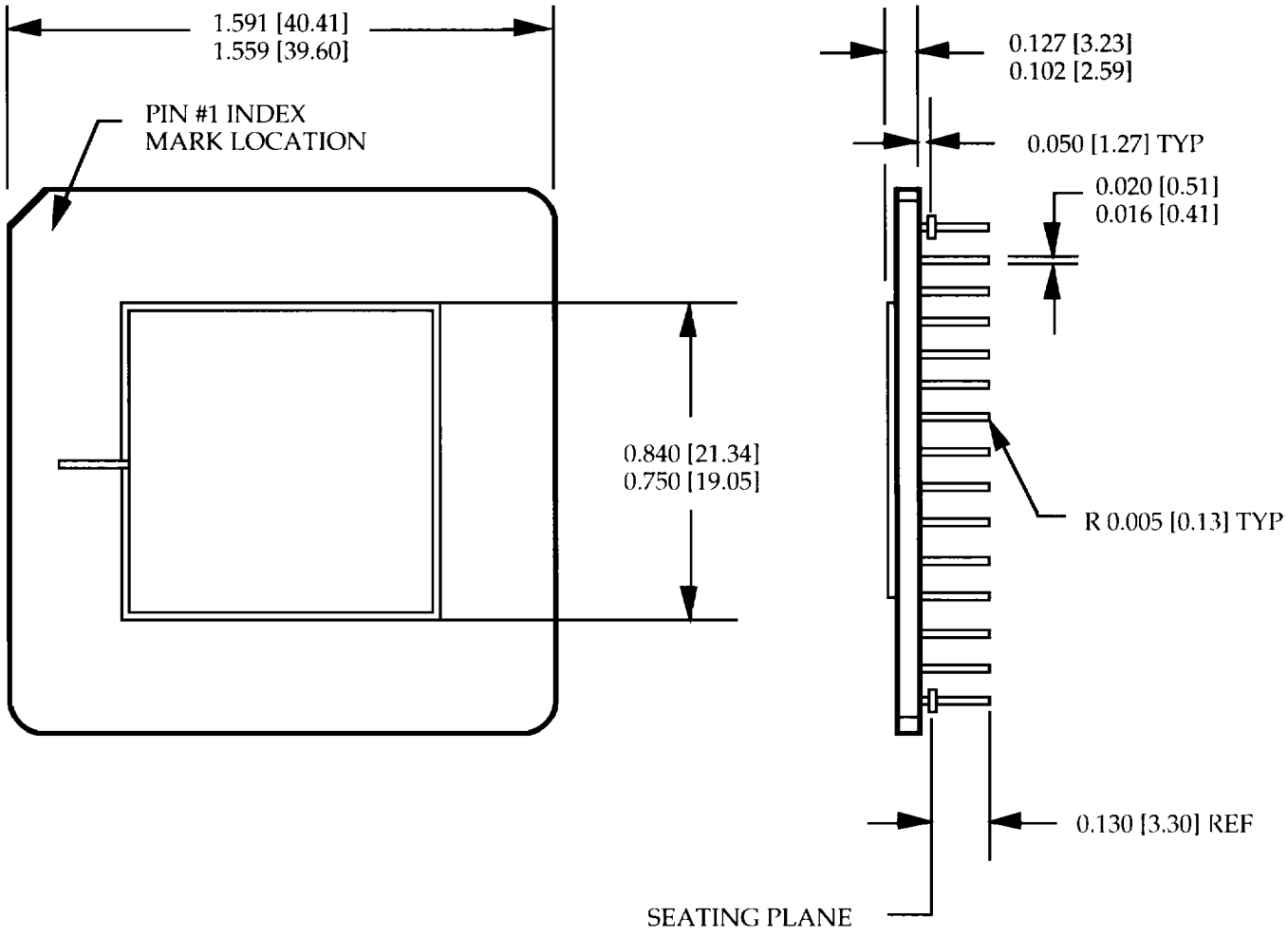
dsp

bottom	signal
L9	
L10	
L11	
L12	IACKN
L13	ERDN2
L14	ERDN6
L15	EWRN3
M1	DA9
M2	CA11
M3	CA13
M4	DA15
M5	VDD
M6	CA7
M7	DA7
M8	VSS
M9	CA0
M10	VDD
M11	VSS
M12	PA1
M13	ERDN3
M14	ERDN7
M15	EWRN4

dsp

bottom	signal
R9	PA12
R10	PA13
R11	VSS
R12	PA14
R13	PA15
R14	EWRN7
R15	EWRN6

Figure 9: Pin Assignment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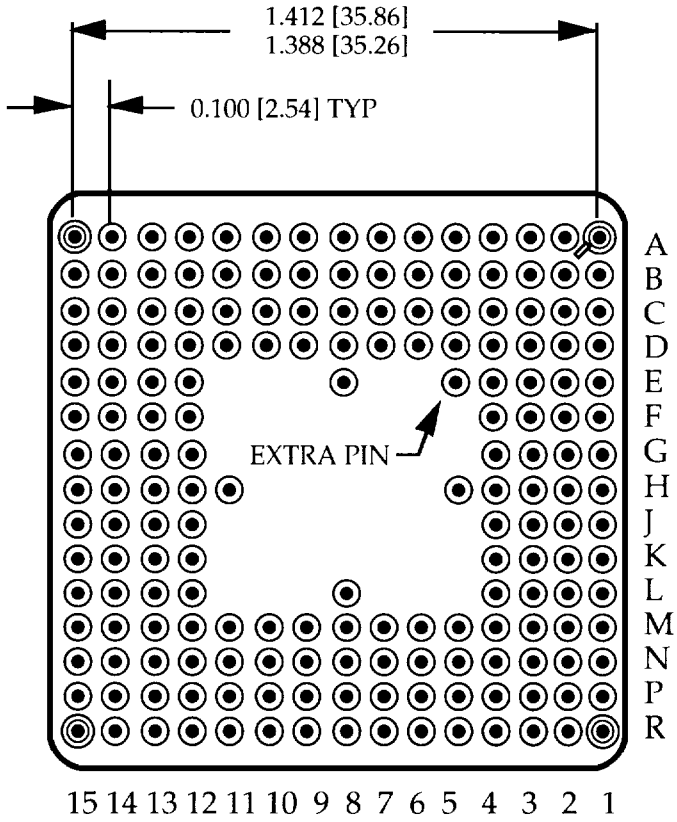
1.559 [39.60]
PIN #1 INDEX
MARK LOCATION
0.840 [21.34]
0.750 [19.05]
0.127 [3.23]
0.102 [2.59]
0.050 [1.27] TYP
0.020 [0.51]
0.016 [0.41]
R 0.005 [0.13] TYP
0.130 [3.30] REF
SEATING PLANE



NOTES:
1. Dimensions are in inches [millimeters].
2. Tolerances to be +/- 0.005 [+/- 0.13].
3. Lead Finish: Gold Plating 60 microinches minimum thickness over 100 microinches nominal thickness of Nickel
4. Material: AL203
5. Lead Material: Kovar.
6. 180 Ceramic pin grid array.
Cavity up - 15 x 15 matrix
DWG No: 25-70014REV: .D

Figure 10: Mechanical Data

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