VTC Inc.
Value the Customer™

VM7800

4, 6, OR 10-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH MULTIPLE SERVO WRITE CAPABILITY

960801

August,1996

FEATURES

- High Performance
  - *Read Gain Options* = 150 - 300 V/V Typical
  - Input Noise = 0.55nV/$\sqrt{Hz}$ Typical
  - Head Inductance Range = 0.2 – 5 µH (0.5 µH typical)
  - IW Rise/Fall Times = 9 ns (L_H = 1 µH, I_W = 20 mA b-p)
  - Write Current Range 5 - 35 mA
  - Low Input Capacitance = 14 pF Typical
  - Head Voltage Swing = 8.8 Vpp Typical
- PECL Write Data Inputs
- Multi-Channel Servo Write Available
- Very Low Power Dissipation = 1 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Single Power Supply = 5 V ± 10%
- Write Unsafe Detection
- *Fast Write-to-Read Recovery Time*
- Available in 4, 6, or 10-Channels

DESCRIPTION

The VM7800 is a high-performance read/write preamplifier designed for use in high-end disk drives. It provides write current control, data protection circuitry, and a low-noise read preamplifier for ten channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 1mW.

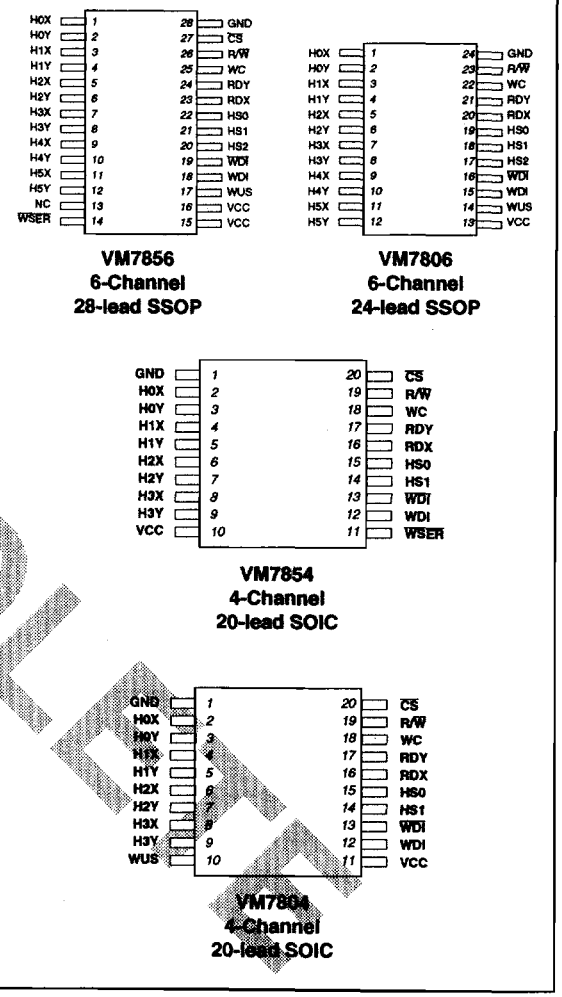
Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in write mode.

Very low-power dissipation from the +5V supply is achieved through use of high-speed bipolar processing and innovative circuit design techniques.

In multi-channel servo write mode, multiple heads can be written simultaneously. The 4- and 6-channel VM7800 devices have an active low servo-write enable ($\overline{WSER}$) and, when active, write all heads simultaneously. The 10-channel VM7800 device has an active high servo-write enable (WSER) and, when active, writes all even or odd heads simultaneously depending on the state of the head select zero pin (HS0). An internal resistor pulls up or down pin $\overline{WSER}$/WSER so that when it is left open, the chip will be in normal single head write mode.

The VM7800 is available in several different packages. Not all of the VM7800 features are available in every package style. Please contact VTC for package availability.

CONNECTION DIAGRAMS



For additional connection diagrams see the last page of this datasheet.

ABSOLUTE MAXIMUM RATINGS

Power Supply:
V_{CC} ..... -0.3V to +7V
Write Current I_W 60mA
Input Voltages:
Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V
Output Current:
RDX, RDY: I_O .....-10mA
WUS: I_{WUS} ..... +12mA
Junction Temperature ..... 150°C
Storage Temperature Tstg ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
20-lead SOIC ..... 90°C/W
24-lead SSOP ..... 100°C/W
28-lead SSOP ..... 100°C/W
36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} .....+5V ± 10%
Write current (I_W) ..... 5 to 35mA
Head Inductance (L_H) ..... 0.2 to 5µH
Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7800 addresses up to ten two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins WSER/$\overline{\text{WSER}}$, HS0, $\overline{\text{CS}}$ and R/$\overline{\text{W}}$, as shown in Tables 1 and 4. Tables 2 and 3 shows the head select during servo write mode. Internal resistor pull-high provided on pins $\overline{\text{CS}}$ and R/$\overline{\text{W}}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

The write mode configures the VM7800 as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of a selected head on each high-to-low transition on pin WDI (write data input).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally-generated 2.5 V reference voltage is present at the WC pin. The magnitude of the write current (0-pk ±10%) is:

$$I_W = K_W/R_{WC} + 0.2mA = 50/R_{WC} + 0.2mA \qquad \textit{(eq. 1)}$$

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power-up. Additionally, the write unsafe circuitry will flag any of the conditions below as a high level on the open collector output pin WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Multi-write mode
- No write current
- WDI frequency too low
- Device in read or sleep mode

Multi-Channel Servo Write Mode

In this mode, the operation is the same as described above except that multiple channels are written at the same time (see tables 1 - 3). Pin WSER/$\overline{\text{WSER}}$ would be high/low to enable the multi-write feature. Pin HS0 is used on the 10-channel VM7800 to select which bank of five heads are written simultaneously.

Read Mode

The read mode configures the VM7800 as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC-coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between the write mode and the read mode, thereby substantially reducing the recovery time delay to the subsequent pulse detection circuitry.

Idle Mode

When $\overline{\text{CS}}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to 1mW typical for sleep mode, In sleep mode, the reader outputs are high impedance. This allows multiple chip connection by simply wiring the reader outputs together.

Table 1: Mode Select

R/$\overline{\text{W}}$	*$\overline{\text{CS}}$*	*WSER*	*$\overline{\text{WSER}}$*	*MODE*
0	0	0	1	Write Single
0	0	1	0	Write Servo
1	0	X	X	Read
X	1	X	X	Idle

Table 2: Head Selection in Servo Write Mode (WSER = high) 10-Channel

HS0	*WSER*	*HEAD*
0	1	0, 2, 4, 6, 8
1	1	1, 3, 5, 7, 9

Table 3: Head Selection in Servo Write Mode ($\overline{\text{WSER}}$ = low) 4 and 6-Channel

CHANNELS	*$\overline{\text{WSER}}$*	*HEAD*
4	0	0, 1, 2, 3
6	0	0, 1, 2, 3, 4, 5

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

Table 4: Head Selection

HS3	*HS2*	*HS1*	*HS0*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS3	I*	Head Select: selects one of up to ten heads
H0X - H9X H0Y - H9Y	I/O	X, Y Head Terminals
WDI, $\overline{WDI}$	I*	Write Data Inputs: PECL input signal, negative transition toggles direction of head current.
$\overline{CS}$	I	Chip select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write select: high level selects read mode, low-level indicates writes unsafe condition
WUS	O*	Write unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX-RDY	O*	Read Data Output: differential output data
VCC		+5 volt supply**
GND		Ground
WSER	I*	Servo Write: a high level enables servo mode for 10-channel VM7800
$\overline{WSER}$	I*	Servo Write: a low level enables servo mode for 4 and 6-channel VM7800

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	mA
VCC Supply Current	I_{CC}	Read Mode		58	70	mA
		Write Mode, Normal	44 + I_W	57 + I_W	70 + I_W	
		Write Mode, Servo	65 +5*I_W	100 +5*I_W	120 +5*I_W	
		Sleep Mode		9.5	12	
Power Supply Power Dissipation	PD	Read Mode		320	385	mW
		Write Mode, I_W = 20mA, Normal		421	495	
		Write Mode, Servo		1100	1210	
		Sleep Mode		52	66	
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	V_{IH} = V_{CC} - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	V_{IH} = V_{CC} - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_H < 0.2mA	3.3	3.6	3.9	V

WRITE CHARACTERISTICS *Recommended operating conditions apply unless otherwise specified;* $L_H = 1\mu H$, $R_H = 30\Omega$, $I_W = 20mA$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$V_{CC} = 5V$, $I_W = 5 - 30mA$	41	50	59	V
Write Current Range	I_W	$9.95K > R_{WC} > 1.42K\Omega$	5		35	mA
Write Current Tolerance	ΔI_{WI}	$V_{CC} = 5V$, $5 < I_W < 30mA$	-18		+18	%
		$V_{CC} = 5V$, $30mA < I_W < 35mA$	-20	-8	+5	%
Write Current Supply Sensitivity	$\Delta I_W/V$	$V_{CC} = 5V \pm 10\%$	-6	3	+6	%
Differential Head Voltage Swing	V_{DH}	Open head	7	8.8		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		2.8			kΩ
Unselected Head Current	I_{UH}	$I_W = 20mA$		0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			$V_{CC} - 2.7$		V

Note 1: Typical values are given at $V_{CC} = 5V$ and $T_A = 25°C$.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* (Note 1)	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	168	200	232	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	30	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p	55	75		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.55	0.65	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		14	16	pF
Differential INput Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	800		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45			dB
Channel Separation	CS	Unselected channels: V_{IN} = 20mVp-p @ 5MHz V_{IN} = 0 on selected head	45			dB
Output Offset Voltage	V_{OS}		-200		+200	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read/Write Mode		V_{CC} - 2.7		
RDX, RDY Common Mode Output Voltage Difference	ΔV_{OCM}	100mVp-p @ 5MHz on V_{CC}	-350		+350	mV
Single-Ended Output Resistance	R_{SEO}	f = MHz		15	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

Servo Five Channels Write

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Matching Between Channels	ΔI_W	5mA < I_W < 35mA			22	%
Duty Cycle (25mA/head)					20	%
Write Current Tolerance		5mA < I_W < 35mA, V_{CC} = 5V	-24		+24	%

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.04	0.2	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.3	0.5	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W			0.6	µs
HS0 - HS3 any Head Delay	t_{HS}	HS0 - HS3 to 90% of 100mV, 10MHz read signal envelope			0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6		3.6	µs
WUS Unsafe to Safe Delay	t_{D2}	I_W = 35mA			1.0	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points			30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0			1.0	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.5	4	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		9	12	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

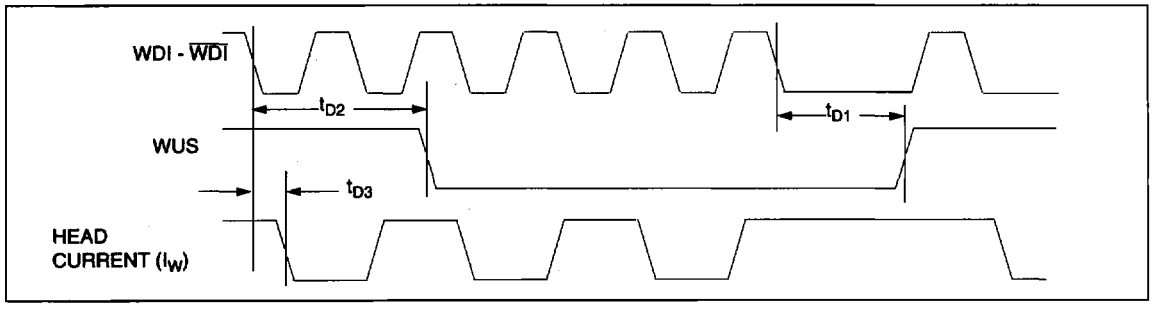
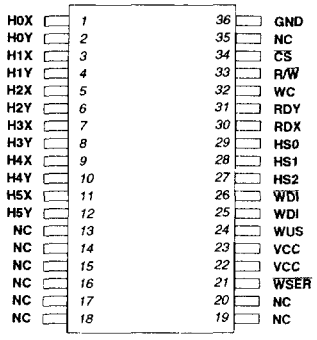
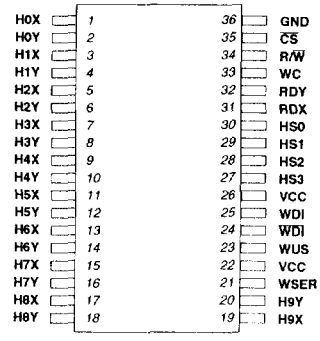


Figure 1: Write Mode Timing Diagram

ADDITIONAL CONNECTION DIAGRAMS



VM7856
6-Channel
36-lead SOIC



VM78510
10-Channel
36-lead SOIC