

**SN55461 THRU SN55464  
SN75461 THRU SN75463  
DUAL PERIPHERAL DRIVERS**  
D2218, DECEMBER 1976—REVISED MAY 1990

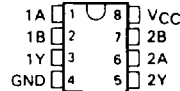
**PERIPHERAL DRIVERS FOR HIGH-VOLTAGE,  
HIGH-CURRENT DRIVER APPLICATIONS**

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching
- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) with Copper Lead Frame for Cooler Operation and Improved Reliability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

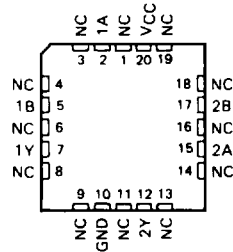
**SUMMARY OF SERIES 55461/75461**

DEVICE	LOGIC	PACKAGES
SN55461	AND	FK,JG
SN55462	NAND	FK,JG
SN55463	OR	FK,JG
SN55464	NOR	FK,JG
SN75461	AND	D,P
SN75462	NAND	D,P
SN75463	OR	D,P

SN55461, SN55462,  
SN55463, SN55464 . . . JG PACKAGE  
SN75461, SN75462,  
SN75463 . . . D OR P PACKAGE  
(TOP VIEW)



SN55461, SN55462,  
SN55463, SN55464, . . . FK PACKAGE  
(TOP VIEW)



NC — No internal connection

**description**

These dual peripheral drivers are functionally interchangeable with SN55451B through SN55454B and SN75451B through SN75453B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than those devices can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic), with the output of the gates internally connected to the bases of the n-p-n output transistors.

Series SN55461 drivers are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; Series SN75461 drivers are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**PRODUCTION DATA** documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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**SN55461 THRU SN55464  
SN75461 THRU SN75463  
DUAL PERIPHERAL DRIVERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55461 SN55462 SN55463 SN55464	SN75461 SN75462 SN75463	UNIT
Supply voltage, $V_{CC}$ (see Note 1)	7	7	V
Input voltage	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	V
Off-state output voltage	35	35	V
Continuous collector or output current (see Note 3)	400	400	mA
Peak collector or output current ( $t_w \leq 10$ ms, duty cycle $\leq 50\%$ , see Note 3)	500	500	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range, $T_A$	-55 to 125	0 to 70	°C
Storage temperature range	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds	FK package	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260 °C

- NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.  
2. This is the voltage between two emitters of a multiple-emitter transistor.  
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

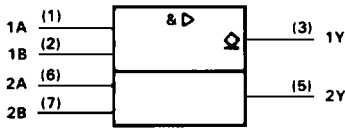
	SN55461 THRU SN55464			SN75461 THRU SN75463			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, $V_{IH}$	2			2			V
Low-level input voltage, $V_{IL}$				0.8			V
Operating free-air temperature, $T_A$	-55			125			0 70 °C



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# SN55461, SN75461 DUAL PERIPHERAL POSITIVE-AND DRIVERS

## logic symbol†



† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, JG, and P packages.

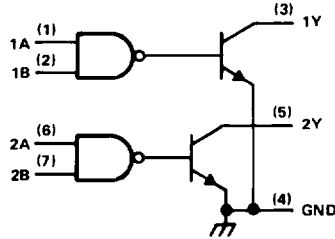
**FUNCTION TABLE  
(EACH DRIVER)**

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

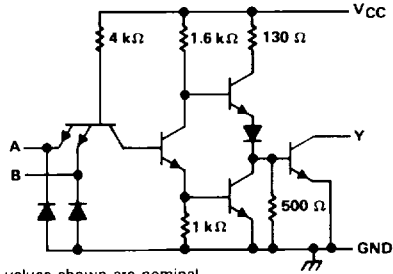
positive logic:

$$Y = AB \text{ or } \overline{A} + \overline{B}$$

## logic diagram (positive logic)



## schematic (each driver)



Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS†	SN55461		SN75461		UNIT
		MIN	TYP‡	MAX	MIN	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$	-1.2		-1.5		V
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}$ , $V_{OH} = 35 \text{ V}$		300		100	$\mu\text{A}$
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 100 \text{ mA}$	0.25	0.5	0.25	0.4	V
	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 300 \text{ mA}$	0.5	0.8	0.5	0.7	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$		1		1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$		40		40	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$	-1	-1.6	-1	-1.6	mA
$I_{CCH}$ Supply current, outputs high	$V_{CC} = \text{MAX}$ , $V_I = 5 \text{ V}$	8	11	8	11	mA
$I_{CCL}$ Supply current, outputs low	$V_{CC} = \text{MAX}$ , $V_I = 0$	56	76	56	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

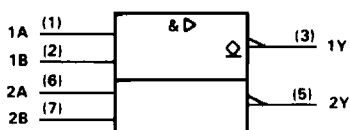
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{pLH}$ Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$ , $C_L = 15 \text{ pF}$ , $R_L = 50 \Omega$ , See Figure 1		30	55	ns	
$t_{pHL}$ Propagation delay time, high-to-low-level output			25	40	ns	
$t_{TLH}$ Transition time, low-to-high-level output				8	20	ns
$t_{THL}$ Transition time, high-to-low-level output				10	20	ns
$V_{OH}$ High-level output voltage after switching	SN55461		$V_S - 10$		mV	
	SN75461		$V_S - 10$			

**TEXAS  
INSTRUMENTS**

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# SN55462, SN75462 DUAL PERIPHERAL POSITIVE-NAND DRIVERS

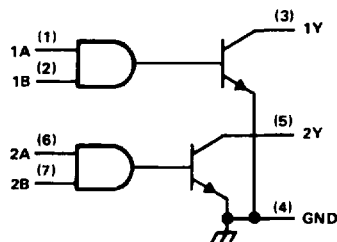
logic symbol†



† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)



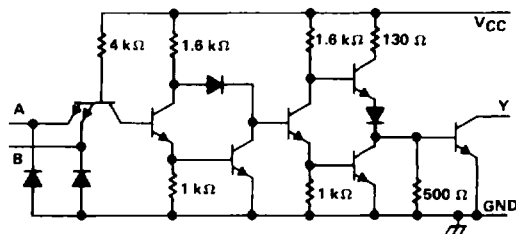
FUNCTION TABLE  
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:

$$Y = \overline{AB} \text{ or } \overline{A} + \overline{B}$$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS†	SN55462			SN75462			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$	-1.2		-1.5	-1.2		-1.5	V
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $V_{OH} = 35 \text{ V}$			300			100	$\mu\text{A}$
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = \text{MIN}$ , $I_{OL} = 100 \text{ mA}$	0.25		0.5	0.25		0.4	V
	$V_{CC} = \text{MIN}$ , $V_{IH} = \text{MIN}$ , $I_{OL} = 300 \text{ mA}$	0.5		0.8	0.5		0.7	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$			40			40	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$	-1.1		-1.6	-1.1		-1.6	mA
$I_{CCH}$ Supply current, outputs high	$V_{CC} = \text{MAX}$ , $V_I = 0$		13	17		13	17	mA
$I_{CCL}$ Supply current, outputs low	$V_{CC} = \text{MAX}$ , $V_I = 5 \text{ V}$		61	76		61	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

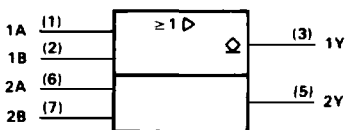
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$ , $C_L = 15 \text{ pF}$ , $R_L = 50 \Omega$ , See Figure 1	45	65		ns
$t_{PHL}$ Propagation delay time, high-to-low-level output		30	50		ns
$t_{TLH}$ Transition time, low-to-high-level output		13	25		ns
$t_{THL}$ Transition time, high-to-low-level output		10	20		ns
$V_{OH}$ High-level output voltage after switching	SN55462 SN75462	$V_S = 30 \text{ V}$ , See Figure 2	$I_O \approx 300 \text{ mA}$ ,	$V_S - 10$	mV

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# SN55463, SN75463 DUAL PERIPHERAL POSITIVE-OR DRIVERS

## logic symbol†



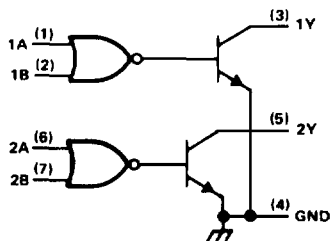
†This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for D, JG, and P packages.

**FUNCTION TABLE  
(EACH DRIVER)**

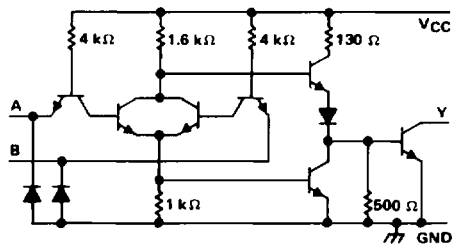
A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:  
 $Y = A + B$  or  $\overline{A} \overline{B}$

## logic diagram (positive logic)



## schematic (each driver)



Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS†	SN55463		SN75463		UNIT
		MIN	TYP‡	MAX	MIN	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$	-1.2	-1.5	-1.2	-1.5	V
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}$ , $V_{IH} = \text{MIN}$ , $V_{OH} = 35 \text{ V}$		300		100	$\mu\text{A}$
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 100 \text{ mA}$	0.25	0.5	0.25	0.4	V
	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 300 \text{ mA}$	0.5	0.8	0.5	0.7	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$		1		1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$		40		40	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$		-1		-1	mA
$I_{CCH}$ Supply current, outputs high	$V_{CC} = \text{MAX}$ , $V_I = 5 \text{ V}$	8	11	8	11	mA
$I_{CCL}$ Supply current, outputs low	$V_{CC} = \text{MAX}$ , $V_I = 0$	58	76	58	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

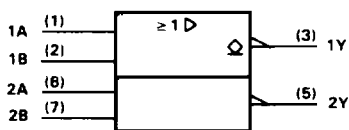
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$I_O = 200 \text{ mA}$ , $C_L = 15 \text{ pF}$ , $R_L = 50 \Omega$ , See Figure 1		30	55	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output			25	40	ns
$t_{TLH}$ Transition time, low-to-high-level output			8	25	ns
$t_{THL}$ Transition time, high-to-low-level output			10	25	ns
$V_{OH}$ High-level output voltage after switching	SN55463	$V_S = 30 \text{ V}$ , See Figure 2	$I_O = 300 \text{ mA}$ ,	$V_S - 10$	mV
	SN75463			$V_S - 10$	

**TEXAS  
INSTRUMENTS**

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# SN55464 DUAL PERIPHERAL POSITIVE-NOR DRIVER

## logic symbol†



† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the JG package.

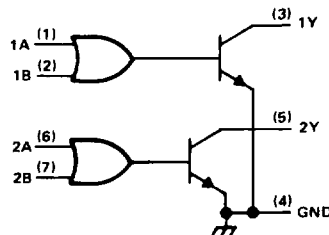
**FUNCTION TABLE  
(EACH DRIVER)**

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

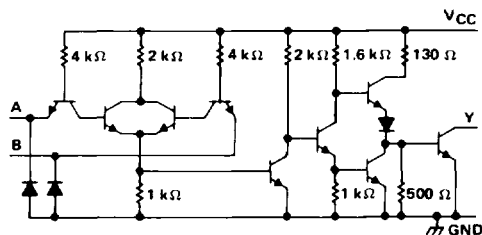
positive logic:

$$Y = \overline{A + B} \text{ or } \overline{A} \overline{B}$$

## logic diagram (positive logic)



## schematic (each driver)



Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS†	SN55464			UNIT	
		MIN	TYP‡	MAX		
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$	-1.2	-1.5		V	
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $V_{OH} = 35 \text{ V}$			300	$\mu\text{A}$	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = \text{MIN}$ , $I_{OL} = 100 \text{ mA}$	0.25	0.5		V	
	$V_{CC} = \text{MIN}$ , $V_{IH} = \text{MIN}$ , $I_{OL} = 300 \text{ mA}$	0.5	0.8			
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1	mA	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$			40	$\mu\text{A}$	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-1	-1.6	mA
$I_{CCH}$ Supply current, outputs high	$V_{CC} = \text{MAX}$ , $V_I = 0$			14	19	mA
$I_{CCL}$ Supply current, outputs low	$V_{CC} = \text{MAX}$ , $V_I = 5 \text{ V}$			67	85	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

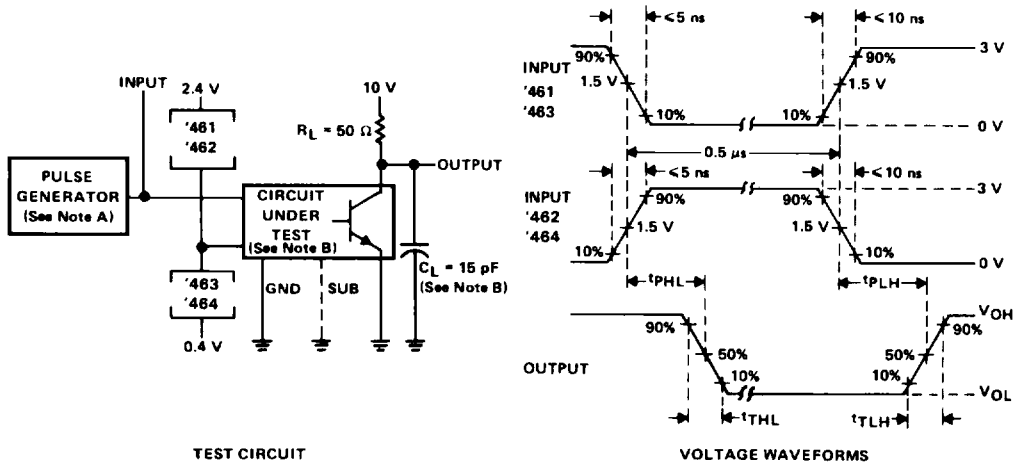
## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{PLH}$ Propagation delay time, low-to-high-level output	$I_O = 200 \text{ mA}$ , $C_L = 15 \text{ pF}$ , $R_L = 50 \Omega$ , See Figure 1		40	65	ns	
$t_{PHL}$ Propagation delay time, high-to-low-level output			30	50	ns	
$t_{TLH}$ Transition time, low-to-high-level output				8	20	ns
$t_{THL}$ Transition time, high-to-low-level output				10	20	ns
$V_{OH}$ High-level output voltage after switching	SN55464	$V_S = 30 \text{ V}$ , $I_O = 300 \text{ mA}$ ,		$V_S - 10$	mV	
	SN75464	See Figure 2		$V_S - 10$		

TEXAS  
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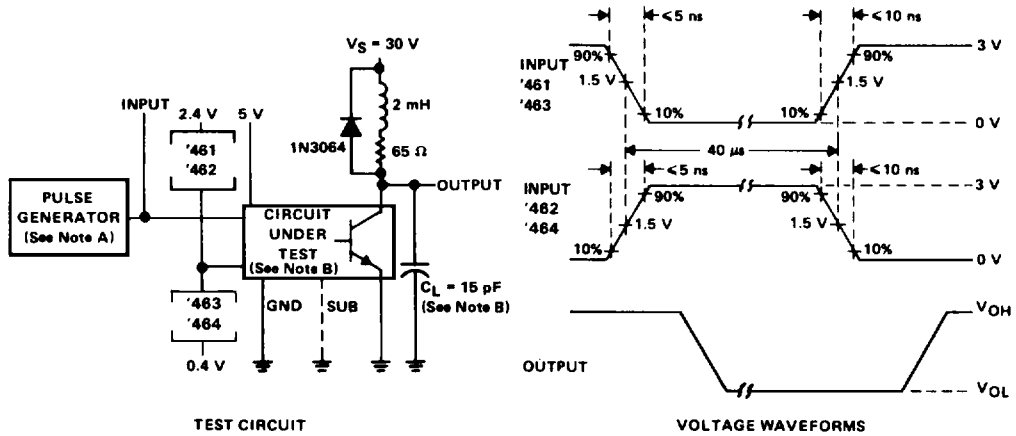
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_{out} = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES



NOTES: A. The pulse generator has the following characteristics:  $PRR \leq 12.5 \text{ kHz}$ ,  $Z_o = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST