

T1-DS1/E1-CEPT Framer Formater

Description

The 29C96 is a programmable CMOS device interfacing with T1 (DS1) or E1 (CEPT) transceivers. The 29C96 supports following frame formats :

- DS1 : 4 frames (DMI), D4 (G704), ESF (G704), SLC-96 (DMI), DDS (DMI)
- CEPT : double frame, CRC4

In CEPT mode the modified CRC4 multiframe alignment algorithm of G706 (Appendix B) recommendation is supported in order to allow interworking of equipments with and without CRC4 capability. Line coding is ZCS (zero suppression mode), B8ZS (T1) or HDB3 (CEPT). Several signalling modes are supported by the 29C96 :

- DS1 : Transparent 0 to 16 states robbed bit signalling mode or Common Channel signalling (channel 24 CCS) mode.
- CEPT : Transparent, IRSM or Channel associated mode.

signalling source can be external (input pin) or internal (signalling RAM). The 29C96 allows CLEAR CHANNEL capabilities in DS1 for mixed voice and data channels. The 29C96 synchronizer/formatter handles alarm generation and detection, error detection and counting, and performance monitoring. The host microprocessor controls operations of the

29C96 via the 8 bits data bus/7 bits address bus by reading the internal addressable registers or via an interrupt sequence. The 29C96 offers line control capabilities with a variety of LOOP BACK modes. Monitoring of ZCS/B8ZS/HDB3, out of frame and CRC errors can be programmed through registers and control lines. The 29C96 handles different types of alarms (YELLOW alarm, BLUE alarm and multiframe alarm). The system interface includes independant serial in/out ports for signalling data and data-link, associated with a variety of Frame, Superframe, signalling and Data-link synchronization signals. The 29C96 can interface up to four PCM buses or 1 to 128 time slots. The 29C96 can transfer T1 or CEPT frames to a 24 or 32 time slots bus with the dedicated clocks. Each incoming or outgoing data from T1/CEPT frame can be written or read at any time slot of any PCM bus. All unselected PCM time slots are put in high-Z mode. Each incoming data from frame can be replaced by a programmable MASK code. Each outgoing data from PCM can be replaced by a programmable IDLE code, by the AIS (ALARM INDICATION SIGNAL) code, patched with signalling data or form a CLEAR CHANNEL (transparent transmission). Programming of the 29C3xx transceiver is done through a dedicated '29C3xx port.'

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Features

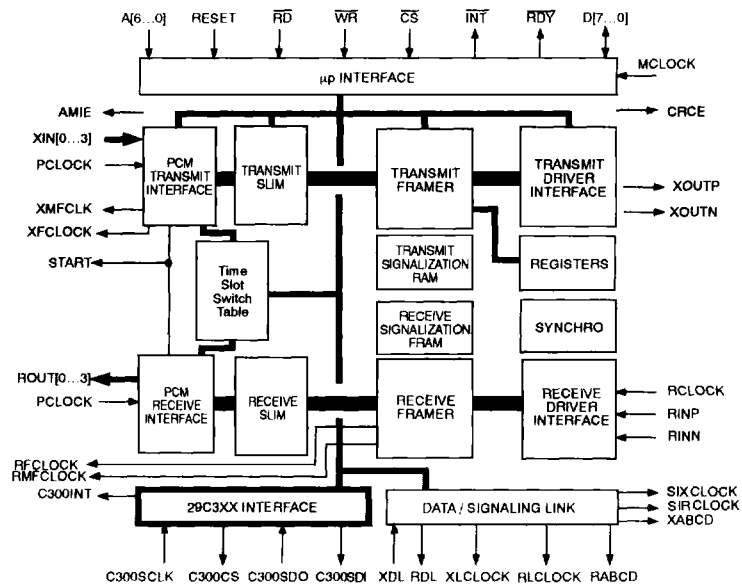
- T1/CEPT compatible frame formater
- AMI or inverted AMI encoding with selectable "0" suppression mode :
 - B8ZS (T1)
 - HDB3 (E1 : CEPT)
 - ZCS
- Supports common and individual signalling modes in T1 and CEPT modes.
- Supports the following modes for T1/DS1 :
 - 4 frames (193N),
 - D4,
 - DDS,
 - ESF,
 - SLC-96
- Supports the following modes for CEPT :
 - Double frame
 - CRC4 (Modified CRC4 alignment algorithm in G706 supported),

Applications

- Computer to PBX interfaces (DMI)
- T1/CEPT digital trunk interfaces
- Digital cross-connect interfaces
- High speed computer to computer data links

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Functional Block Diagram



Description

PCM Interface

Transmit/receive PCM block is in charge of data transfer between the SLIM memory and PCM interface. This interface includes 4 × programmable serial bus (CEPT or T1), it can be connected to 29C94 HDLC controller or to 29C95 ECMA102 controller. It includes :

- 4 × parallel/serial (PISO) adaptators for receiver
- 4 × serial/parallel (SIPO) adaptators for transmitter
- 1 × 128 × 8 buffer for receiver
- 1 × 128 × 8 buffer for transmitter
- 1 finish state machine used to transfer data between SIPOs and 128 × 8 buffer.

SLIM Memory

The SLIM memory is interfacing between FRAMER and PCM interface. Both receiver and transmitter include a [32 × 8] × 2 SLIM RAM. This memory is in charge of network clock jitter absorbtion.

Framer

Framer is interfacing between SLIM memory and DRIVER interface clock. It is in charge of data/F/signalization framing and unframing. In case of internal programming all signalization data is read/written from/to 2 internal 32 × 8 banks.

Driver Interface Block

This block is interfacing between the FRAMER and DRIVER interface. It can be connected to 29C3xx driver and it is in charge of :

- data encoding/decoding (B8ZS/HDB3/ZCS),
- CRC calculation/checking

29C3xx Interface

This block is in charge of 29C3xx programming through a dedicated interface (see 29C3xx datasheet). It includes a parallel/serial adaptor and hardware logic

in order to control the 29C3xx in Host Mode Operation (CLKE).

Data Link/signalling Block

This block is in charge of interfacing between data link/external signalling source and FRAMER. It includes :

- clock generation (XLCLOCK, SIXCLOCK),
- serial/parallel adaptation

µP Interface

This block is in charge of interfacing various microprocessors through an 8-bit data bus and a 7-bit address bus.

Time Slot Switch Registers

The total number of time slots/channels handled at

PCM interface is 128. The TSSR is in charge of channel assignation between the PCM interface and the FRAMER, the 29C96 can only process 32 time slots in CEPT mode and 24 time slots in T1 mode.

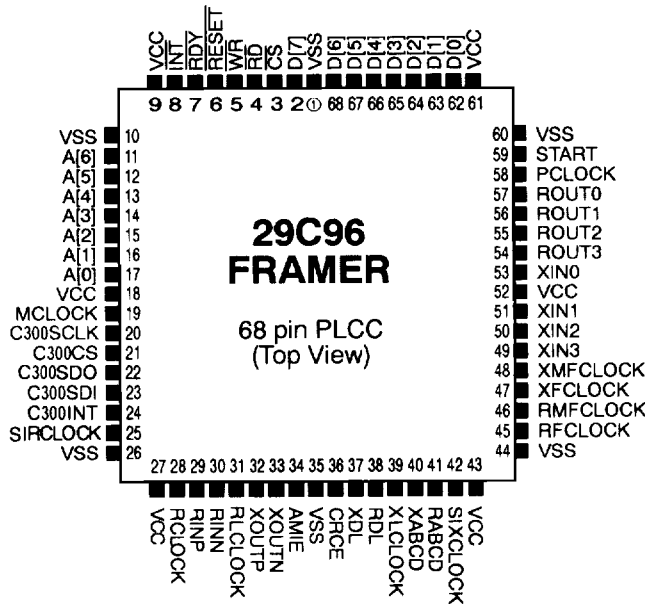
Signalization RAM

The SIGNALIZATION RAM is a $2 \times 32 \times 8$ RAM on both side providing/storing signalization data to/from the FRAMER when the Internal signalization source mode is programmed.

Synchro Block

This block is in charge of circuit synchronization using frame and multiframe signalling.

Pinout



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PIN	NAME	TYPE	DESCRIPTION
1	VSS	SUPPLY	GROUND
2,62..68	D[7:0]	I/O	8 bit microprocessor data bus. Bi-directional.
3	CS	I	Chip-select (active low) : selects the 29C96 addressing and allows data transfer through D0-D7 data bus.
4	RD	I	READ (active low) : enables data transfer from 29C96 to D0-D7 data bus.
5	WR	I	WRITE (active low) : enables data transfer from D0-D7 data bus to 29C96.
6	RESET	I	Active low. A '0' applied on this pin initializes registers.
7	RDY	O	READY : a high to low transition on this pin indicates that the 29C96 is ready to transfer information to/from the data bus. When the 29C96 is not selected, this pin is floating.
8	INT	O	INTERRUPT REQUEST. When low, this pin indicates that the 29C96 is requesting an interrupt to the host microprocessor.
9	VCC	SUPPLY	5 V \pm 10 %
10	VSS	SUPPLY	Ground
11 - 17	A[6:0]	I	ADDRESS BUS. 7 bits address bus
18	VCC	SUPPLY	5 V \pm 10 % Supply
19	MCLOCK	I	Microprocessor clock. Minimum frequency 10 MHz.
20	C300SCLK	O	29C300 interface. Serial clock, must be connected to pin 27 of 29C3xx primary rate transceiver.
21	C300CS	O	29C300 interface. Chip select, must be connected to pin 26 of 29C3xx primary rate transceiver.
22	C300SDO	I	29C300 interface. Serial data out, must be connected to pin 25 of 29C3xx primary rate transceiver.
23	C300SDI	O	29C300 interface. Serial data in, must be connected to pin 24 of 29C3xx primary rate transceiver.
24	C300INT	I	29C300 interface. Interrupt request, must be connected to pin 23 of 29C3xx primary rate transceiver.
25	SIRCLOCK	O	Datalink receive clock.
26	VSS	SUPPLY	Ground.
27	VCC	SUPPLY	5 V \pm 10 % Supply.
28	RCLOCK	I	Receive line clock : 1.544 MHz primary clock (T1)/2.048 MHz primary clock (CEPT).
29	RINP	I	AMI positive receive data input.
30	RINN	I	AMI negative receive data input.
31	RLCLOCK	O	Signalling clock output.
32	XOUTP	O	AMI positive transmit data output.
33	XOUTN	O	AMI negative transmit data output.
34	AMIE	O	The 29C96 detects an AMI error when this mode is selected.
35	VSS	SUPPLY	Ground.
36	CRCE	O	CRC error, valid in ESF or CRC4 modes only.
37	XDL	I	Transmit data link input for FDL bit in ESF mode and D bits in DDS.SLC, IRSM modes.

PIN	NAME	TYPE	DESCRIPTION
38	RDL	O	Receive data link output for FDL bits in ESF mode and D bits in DDS, SLC, IRSM modes.
39	XLCLOCK	O	Data link transmit clock for XDL.
40	XABCD	I	Transmit signalling data input : data input for ABCD signalling bits.
41	RABCD	O	Receive signalling data output : data output for ABCD signalling bits.
42	SIXCLOCK	O	Transmit signalling clock for XABCD.
43	VCC	SUPPLY	5 V \pm 10 % Supply.
44	VSS	SUPPLY	Ground.
45	RFCLOCK	O	Receive frame synchronization pulse : low to high transition occurs with the first bit of a frame. Period of this pulse is 125 μ s. Duration of high level is one time slot.
46	RMFCLOCK	O	Receive multiframe synchronization pulse : low to high transition occurs with the first bit of a multiframe and high to low transition occurs on the first bit of the second frame. Period of this pulse is 1.5 ms (D4), 3.0 ms (ESF), 6.0 ms (SLC), 250 μ s (DOUBLEFRAME) or 2 ms (CRC4). Duration of high level is 125 μ s.
47	XFCLOCK	O	Transmit frame synchronization pulse : low to high transition occurs with the first bit of a frame. Period of this pulse is 125 μ s. Duration of high level is one time slot.
48	XMFCLOCK	O	Transmit multiframe synchronization pulse : low to high transition occurs with the first bit of a multiframe and is active during the first frame, high to low transition occurs on the first bit of the second frame. Period of this pulse is 1.5 ms (D4), 3.0 ms (ESF), 6.0 ms (SLC), 250 μ s (DOUBLEFRAME) or 2 ms (CRC4). Duration of high level is 125 μ s.
49	XIN3	I	PCM3 transmit data input.
50	XIN2	I	PCM2 transmit data input.
51	XIN1	I	PCM1 transmit data input.
52	VCC	SUPPLY	5 V \pm 10 % Supply.
53	XIN0	I	PCM0 transmit data input.
54	ROUT3	O	PCM3 receive data output.
55	ROUT2	O	PCM2 receive data output.
56	ROUT1	O	PCM1 receive data output.
57	ROUT0	O	PCM0 receive data output.
58	PCLOCK	I	PCM0, 1, 2, 3 transmit/receive interface clock : 1.544 MHz (T1) or 2.048 MHz (CEPT) PCM clock. This clock can be doubled (3.088/4.096 MHz) or quadrupled (6.196/8.192 MHz).
59	START	I/O	PCM transmit synchronization start pulse.
60	VSS	SUPPLY	Ground.
61	VCC	SUPPLY	5 V \pm 10 % Supply.

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Registers

1. Register Mapping

R/W : Read and Write register.
 R : Read only register.
 W : Write only register.

T/C : Register exists in T1 and CEPT.
 C : Register exists in CEPT only.
 T : Register exists in T1 only.

NAME	ADDRESS		MODE	DESCRIPTION	TYPE
	HEX	DEC			
ALARM	00	0	T/C	ALARM REGISTER	R
ERROR	01	1	T/C	ERROR REGISTER	R
MSR	02	2	T/C	MEMORY STATUS REGISTER	R
SSR	03	3	T/C	SYNCHRONIZATION STATUS REGISTER	R
TCR	04	4	T/C	TRANSMIT CONTROL REGISTER	R/W
MODE	05	5	T/C	MODE REGISTER	R/W
LSCR	06	6	T/C	LOOPBACK and SIGNALLING REGISTER	R/W
LCR	07	7	T/C	LINE CONTROL REGISTER	R/W
FCR	08	8	T/C	FRAMER CONTROL REGISTER	R/W
MASK0	09	9	T/C	MASK REGISTER 0	R/W
MASK1	0A	10	T/C	MASK REGISTER 1	R/W
MASK2	0B	11	T/C	MASK REGISTER 2	R/W
TDLR or TSBR	0C	12	T C	TRANSMIT DATA LINK REGISTER (T1) TRANSMIT SPARE BITS REGISTER (CEPT)	R/W R/W
RDLR or RSBR	0D	13	T C	RECEIVE DATA LINK REGISTER (T1) RECEIVE SPARE BITS REGISTER (CEPT)	R/W R/W
IDLE	0E	14	T/C	IDLE REGISTER	R/W
ICR0	0F	15	T/C	IDLE CHANNELS REGISTER 0	R/W
ICR1	10	16	T/C	IDLE CHANNELS REGISTER 1	R/W
ICR2	11	17	T/C	IDLE CHANNELS REGISTER 2	R/W
ICR3	12	18	T/C	IDLE CHANNELS REGISTER 3	R/W
RMR	13	19	T/C	RECEIVE MASK REGISTER	R/W
MCR0	14	20	T/C	MASK CHANNELS REGISTER 0	R/W
MCR1	15	21	T/C	MASK CHANNELS REGISTER 1	R/W
MCR2	16	22	T/C	MASK CHANNELS REGISTER 2	R/W
MCR3	17	23	T/C	MASK CHANNELS REGISTER 3	R/W
CLAR	18	24	T/C	CHANNEL LOOPBACK ADDRESS REGISTER	R/W
XBR	19	25	C	EXTRA BITS REGISTER	R/W
PMR	1A	26	T/C	PCM MODE REGISTER	R/W
CCR0	1B	27	T	CLEAR CHANNEL REGISTER 0	R/W
CCR1	1C	28	T	CLEAR CHANNEL REGISTER 1	R/W
CCR2	1D	29	T	CLEAR CHANNEL REGISTER 2	R/W
MXT	1E	30	T/C	29C300 REGISTER	R/W
CEC0	20	32	T/C	CRC ERROR COUNTER 0	R/W
CEC1	21	33	T/C	CRC ERROR COUNTER 1	R/W
FEC0	22	34	T/C	FRAMING BIT ERROR COUNTER 0	R/W
FEC1	23	35	T/C	FRAMING BIT ERROR COUNTER 1	R/W
AEC0	24	36	T/C	AMI ERROR COUNTER 0	R/W
AEC1	25	37	T/C	AMI ERROR COUNTER 1	R/W
TSR1..32	40..5F	64..95	T/C	TRANSMIT SIGNALLING REGISTER 1..32	W
RSR1..32	40..5F	64..95	T/C	RECEIVE SIGNALLING REGISTER 1..32	R
TSSR1..32	60..7F	96..127	T/C	TIME SLOT SWITCHING REGISTER 1..32	R/W

2. Registers Description

2.1 ALARM REGISTER ALARM RESET = 0 @ = 00H R

Ya	FTEMPO	Ys	LFA	DSYNC	LSMA	C300 BUSY	C300 INT
bit 0	1	2	3	4	5	6	7

- .Ya : Ya=1 Upon detection of a REMOTE FRAME ALARM (YELLOW ALARM). Detection depends on framing mode (D4, ESF, SLC96, DOUBLE FRAME, CRC4)
- .FTEMPO FTEMPO=1 When BFA is not found within 100ms.
T1 : If FTEMPO=1 and LCR.FORCE=1 and there is more than 1 candidate BFA will be locked to the next candidate automatically.
- .Ys Ys=1 upon detection of a REMOTE MULTIFRAME ALARM.
- .LFA T1 mode : Loss of frame alignment, LFA=1 when 2 out of 4 framing bits have been received with error status (Ft bits in 4-frame/D4/SLC96, FAS bits in ESF).
CEPT mode : Loss of frame alignment, LFA=1 when 3 consecutive Frame alignment Signals in time slot 0 are received with error status.
- .DSYNC T1 mode : Loss multiframe alignment, DSYNC=1 when 2 out of the 4 multiframe bits have been received with error status (Fs bits in D4/SLC96) or when 4 "channel 24" multiframe patterns are received with error status within 12 frames in DDS format.
CEPT mode : Loss of multiframe alignment, DSYNC=1 when 915 over 1000 CRC4 multiframe patterns are received with error status. (Valid in CRC4 mode only).
- .LSMA CEPT mode (LSMA) : Loss of multiframe signalling alignment, LSMA=1 when 2 CAS multiframe patterns are received with error status.
- .C300BUSY C300BUSY=1 Upon detection of C300 serial interface busy.
- .C300INT C300INT=1 When a new message from 29C3xx has been loaded in MXT register.

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2.2 ERROR REGISTER ERROR RESET = 0 @ = 01H R

AMIE	CAND	XSMU	XSMO	LSTART	CRCE	ECRC0	ECRC1
bit 0	1	2	3	4	5	6	7

- .AMIE AMIE=1 Upon detection of AMI error.
- .CAND T1 mode : CAND = 1 When there is no candidate for synchronization.
- .XSMU XSMU=1 When the slip memory detects an underflow condition.
- .XSMO XSMO=1 When the slip memory detects an overflow condition.
- .LSTART LSTART=1 when START pulse have not been detected on PCM side for several times.
- .CRCE CRCE=1 when the computed CRC6 or CRC4 of the previous frame does not match the received CRC6 or CRC4.
- .ECRC0 ECRC0=1 when remote computed CRC4 of the previous submultiframe 0 does not match the transmitted CRC4.
- .ECRC1 ECRC1=1 when remote computed CRC4 of the previous submultiframe 1 does not match the transmitted CRC4.

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2.3 MEMORY STATUS REGISTER MSR RESET = 0 @ = 02H R

RSBR/RDLR	TSBR/TDLR	EBRF	XRACK	SRF	AEC	CEC	FEC
bit 0	1	2	3	4	5	6	7

- .RSBR/RDLR RSBR(CEPT) = 1 indicates that the Receive Spare Bit Register is full.
RDLR(T1) = 1 indicates that the Receive Data Link Register is full.
- .TSBR/TDLR TSBR(CEPT) = 1 indicates that the Transmit Spare Bit Register is empty.
TDLR(T1) = 1 indicates that the Transmit Data Link Register is empty.
- .EBRF CEPT only : EBRF = 1 indicates that transmit and/or receive Extra Bit Register is empty and/or full depending on bit3 and bit4 of Extra Bit Register.
- .XRACK XRACK = 1 when transmit signalling RAM is ready to be updated.
- .SRF SRF = 1 when the content of receive signalling RAM has been completely received.
- .AEC AEC = 1 when AMI error counter reaches the maximum count.
- .CEC CEC = 1 when CRC error counter reaches the maximum count.
- .FEC FEC=1 when FRAMING error counter reaches the maximum count.

2.4 SYNCHRONIZATION STATUS REGISTER SSR RESET = 00 @ = 03H R

SYNC	VERR	BFA	CRC4	CRCE0	CRCE1	ECRC0	ECRC1
bit 0	1	2	3	4	5	6	7

- SSR-SYNC frame alignment (CEPT) in received data.
- SSR-VERR multiframe alignment (without CRC controller)
- SSR-BFA basic frame alignment done
- SSR-CRC4 set to '1' when CRC4 alignment is not found
- SSR-CRCE0 indicates one error on CRC4 for the first CEPT submultiframe / or CRC6 error in T1 mode.
- SSR-CRCE1 indicates error on CRCH for the second CEPT submultiframe.
- SSR.ECRC1/SSR.ECRC0 (CEPT) When status indication mode is enabled (via bit FCR.ACSI), these two bits include the received status indicated in Si bits of frames 13 and 15. When received Si bit 13 (or 15) is '0' then ECRC0 (or ECRC1) = 1.

2.5 CRC ERROR COUNTER 0 and 1 CEC0/CEC1 RESET = 0 @ = 20H/21H R/W

CEC0

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CEC1

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bit 0 1 2 3 4 5 6 7

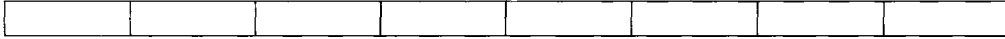
- CEC0 : 8 bits register forming the lower byte of the 16 bits CRC error counter : CEC.
- CEC1 : 8 bits register forming the upper byte of the 16 bits CRC error counter : CEC.

2.6 FRAMING BIT ERROR COUNTER 0 and 1 FEC0/FEC1 RESET = 0 @=22H/23H R/W

FEC0



FEC1

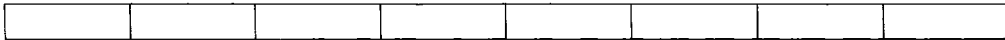


bit 0 1 2 3 4 5 6 7

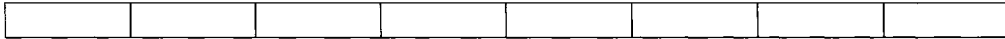
FEC0 : 8 bits register forming the lower byte of the 16 bits Framing bits error counter : FEC.
 FEC1 : 8 bits register forming the upper byte of the 16 bits Framing bit error counter : FEC.

2.7 AMI ERROR COUNTER 0 and 1 AEC0/AEC1 RESET = 0 @=24H/25H R/W

AEC0



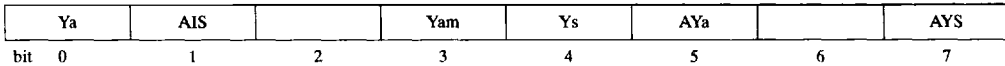
AEC1



bit 0 1 2 3 4 5 6 7

AEC0 : 8 bits register forming the lower byte of the 16 bits AMI Error Counter : AEC.
 AEC1 : 8 bits register forming the upper byte of the 16 bit AMI Error Counter : AEC.

2.8 TRANSMIT CONTROL REGISTER TCR RESET = 0 @=04H R/W



- TCR.Ya Ya=1 indicates that the transmission of a REMOTE FRAME ALARM (YELLOW ALARM) is started. In T1 mode the type of this alarm depends on bit TCR.Yam.
- TCR.AIS AIS=1 indicates that the transmission of an ALARM INDICATION SIGNAL (Framed all '1' pattern) is started.
- TCR.Yam (T1) : Yellow alarm mode. This bit is valid only for D4 and ESF. When this bit is = 0, alarm will be :
 - D4 : every bit 2 of each channel set to '0'.
 - ESF : every bit 2 of each channel set to '0'.
 When this bit is = 1, alarm will be :
 - D4 : the 12th Fs bit set to '1'
 - ESF : content of the FDL bits is a repeated ...11111110000000... (FF00 hexa) pattern.
 In 4-frames and SLC alarm is always :
 - every bit 2 of each channel set to '0'.
 In DDS mode, alarm is marked by setting bit 6 of every channel 24 to '0'.
- TCR.AYa Automatic Yellow alarm transmission. AYa = 1 will initiate transmission of a REMOTE FRAME ALARM upon a detection of a LFA (Loss of Frame Alignment).
- TCR.AYS Automatic multiframe alarm transmission. AYS=1 will initiate transmission of a REMOTE MULTIFRAME ALARM upon a detection or LMA (Loss of Multiframe Alignment).
- TCR.Ys is the bit to be transmitted in CEPT and T1/CCS frames.

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2.9 MODE REGISTER MODE RESET=0 @=05H R/W

mode	fmode0	fmode1/FAS	DL/Si	TTF/Sn	RTF/CRC	smode0	smode1
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mode : mode=1 selects CEPT line format. Mode=0 selects TS/DS1 line format.

MODE.fmode0/fmode1 (T1/DS1) : Selects the T1/DS1 or CEPT multiframe format.

	fmode1	fmode0	smode1	smode0	mode	
4FRAME	0	0	x	x	0	T1/DS1
D4	0	1	x	x	0	T1/DS1
ESF	1	0	x	x	0	T1/DS1
SLC-96	1	1	x	x	0	T1/DS1
DDS	x	x	1	1	0	T1/DS1
DOUBLE FRAME	x	0	x	x	1	CEPT
CRC4	x	1	x	x	1	CEPT

MODE.FAS (CEPT) : When this bit is '0', the FAS framing words are internally generated by the 29C96. When this bit is '1', the FAS framing words are transmitted transparently from input port XIN0...3. Received FAS words are always output at port ROUT0, ROUT3.

MODE.DL (T1/DS1) : When this bit is '1', the SERVICE F bit in 4-frames, the m bit in ESF and the D bit in SLC, DDS are latched at input port XDL (DATA LINK input) for the transmit side and output at port RDL for the receive side. When this bit is '0', these bits are taken from TDLR register (Transmit Data Link Register) for transmission and stored in RDLR register (Receive Data Link Register) for reception.

MODE.Si (CEPT) : When this bit is '1', the international spare bit in the bit 1 of time slot 0 of each frame is latched at input port XIN[0...3] for the transmit side and output at port ROUT[0...3] for the receive side. When this bit is '0', these bits are taken from TSBR register (Transmit Spare Bit Register) for transmission and stored in RSBR register (Receive Spare Bit Register) for reception.

MODE.TTF (T1/DS1) : When this bit is '0', the Ft, Fs (except in 4F) and CRC framing bits are internally generated by the 29C96. When this bit is '1', the Ft, Fs and CRC framing bits are latched at input port.

MODE.Sn (CEPT) : When this bit is '1', the national spare bits (bits 4 to 8 of time slot 0) of odd frames are latched at input port XIN[0...3], at the transmit side and output at port ROUT[0...3] at the receive side. When this bit is '0', these bits are taken from TSBR register (Transmit Spare Bit Register) for transmission and stored in RSBR register (Receive Spare Bit Register) for reception. In the IRSM format, this bit also selects the source of the data link bit. When this bit is '1', the D bit is latched at input port XDL for transmission and output at port RDL for reception. When this bit is '0', the D bits are loaded/stored in registers TSBR and RSBR (Transmit Spare Bit Register and Receive Spare Bit Register) at positions Sn0 to Sn3.

MODE.RTF (T1/DS1) : When this bit is '0', the received Ft, Fs (except in 4F) and CRCX framing bits are transparently output at port ROUT[0...3]. When this bit is '1', the Ft, Fs and CRC framing bits are set to '1'.

MODE.CRC (CEPT mode only) : When this bit is '0', the CRC-4 bits are internally computed by the 29C96. When this bit is '1' the CRC-4 bits are transparently from input port XIN[0...3]. Received CRC-4 bits are always output at port ROUT[0...3].

MODE.smode0/smode1 : signalling mode selection.

T1/DS1	smode1	smode0	CEPT	smode1	smode0
transparent	0	0	transparent	0	0
bit robbing	0	1	CAS	0	1
CCS	1	0	IRSM	1	0

Note : Upon RESET (hard or soft) the circuit configuration is as follow :
 -T1/DS1 mode -4 frame -Fs bits are transmitted and received on data link bus
 -Ft, bits are internally generated (transmit side) -Ft, bits are transparent outputs (receive side)

2.10 LOOPBACK and SIGNALLING CONTROL REGISTER LSCR RESET = 0 @=06H R/W

LLB	RLB	CLB	IDLE	CI	SIGSRC	RBS0/XBS	RBS1/TSA1
bit 0	1	2	3	4	5	6	7

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LSCR.LLB = 1 selects local loop back.

LSCR.RLB = 1 selects remote loop back.

LSCR.CLB = 1 selects channel loop back.

LSCR.IDLE : IDLE = 1 : the content of all transmit channels is replaced by the content of IDLE register.

LSCR.CI : CI=1 : the content of all transmit channels selected in register ICR0, 1, 2 and 3 (IDLE CHANNEL REGISTERS) is replaced by content of IDLE register.

LSCR.SIGSRC : selects the signalling data source. When SIGSRC = 0, signalling data is latched at input port XABCD for transmission and output at port RABCD for reception. When SIGSRC = 1, signalling data is taken from signalling registers TSR1-24/32 for transmission and stored in signalling registers RSR1-24/32 for reception.

LSCR.RBS0/LSCR.RBS1 (T/DS1) : selects the number of robbed bit states.

	RSB1	RSB0	
2 state	0	0	B, C, D signalling bits are replaces by A
4 state	0	1	C is used to carry A and D is used to carry B
16 state	1	0 (ESF only)	ABCD signalling bits are transmitted normally
unused	1	1	

LSCR.XBS (CEPT mode only) In CAS signalling mode, XBS selects the channel 16 frame 0, bits 5, 7 and 8 source (EXTRA BITS 0, 1 and 2). When XBS=0, these bits are extracted from EXTRA BITS registers XBR.XER0, 1 and 2 or stored at EXTRA BIT registers XBR.RER0, 1 and 2. When XBS=1, these bits are latched at port XDL or output at port RDL.

LSCR.TSA1 (CEPT mode only) : In CAS signalling mode, TSA1=1 forces the replacement of all signalling channels (timeslot 16) by the pattern '11111111'.

2.11 LINE CONTROL REGISTER LCR RESET = 0 @=07H R/W

REFRAME	FORCE	ALFA	ALMA	FREEZE	AMI	ZCS	B8ZC/HDB3
bit 0	1	2	3	4	5	6	7

LCR.REFRAME : When REFRAME toggles from 0 to 1, search of frame and multiframe alignment is started.

LCR.FORCE (T1/DS1) : When FORCE=1 and ALARM.FTEMPO = 1 (more than one framing candidate detected), the circuit will synchronize on the next available start bit.

LCR.ALFA : Automatic reframe on loss of frame alignment. ALFA=1 allows the 29C96 to reframe automatically when an LFA event occurs.

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LCR.ALMA : Automatic reframe on loss of multiframe alignment. ALMA=1 allows the 29C96 to reframe automatically when an LMA event occurs.

LCR.AMI : AMI=0 : line coding is in natural AMI, AMI=1 : line coding is in inverted AMI.

LCR.ZCS (T1/DS1) : ZCS=1 selects bit 7 stuffing zero suppression mode.

LCR.B8ZS (T1/DS1) : B8ZS=1 selects B8ZS zero suppression mode.

LCR.HDB3 (CEPT) : HDB3=1 selects HDB3 zero suppression mode.

2.12 FRAMER CONTROL REGISTER FCR RESET = 0 @=08H R/W

RESET	ICRC	CHM	ACSI	XSRREQ	ENACRCH	SEMA	STRANS
bit 0	1	2	3	4	5	6	7

FCR.RESET : When RESET toggles from 0 to 1, the 29C96 is reseted. Control and status registers have their reset values. Transmit formatter and receive synchronizer are stopped and counters are set to zero.

FCR.ICRC : When ICRC=1, INVERTED CRC mode is enabled.

FCR.CHM : When CHM=1 the content of all received channels indicated in registers MCR0, 1 and 2 (MASK CHANNELS REGISTERS) is replaced by the content of RECEIVE MASK register.

FCR.ACSI (CEPT) : Automatic CRC4 Status Indication. When ACSI=1 the CRC errors detected in the received submultiframe 0 and 1, (status bits ERROR.CRCE0 and CRCE1), will be indicated to the remote side by setting respectively the Si bits of frame 13 and 15 to '0' in the transmit data flow.

FCR.XSRREQ = 1 : Signalization RAM update request.

ENACRCH = 1 : (CEPT) Stop CRC4 Controlling.

FCR.STRANS = 1 : Enables transmission on XOUT/XOUT.

FCR.SEMA = 1 : Forces signalling synchro (CEPT)

2.13

MASK0	RESET=0	@=09H	R/W				
YA	FTEMPO	YS	LFA	DSYNC	LSMA	C300 BUSY	C300 INT
bit 0	1	2	3	4	5	6	7

MASK1	RESET=0	@=0AH	R/W				
AMIE	CAND	XSMU	XSMO	LSTART	CRCE	ECRC0	ECRC1
bit 0	1	2	3	4	5	6	7

MASK2	RESET=0	@=0BH	R/W				
RSBR/RDLR	TSBR/TDLR	EBRF	XRACK	SRF	AEC	CEC	FEC
bit 0	1	2	3	4	5	6	7

Each MASK bit corresponds to a status bit. When a status bit and the corresponding mask bit are activated, the INT pin is activated (low). The three status registers ALARM ERROR and MSR must be read in order to identify INT source. The pin will be

desactivated (high) when the register containing the interrupting status bit is read. The ALARM, ERROR and MSR registers are reseted as soon as they are accessed.

2.14 TRANSMIT SIGNALLING REGISTERS 1 to 24/32 TSR1..32 RESET = 0 @=40H..5FH W

A	B	C	D	E	0	0	0
bit 0	1	2	3	4	5	6	7

- TSR (A, B, C, D) Used in CEPT, CAS Mode
- TSR (A, B, C, D, E) Used in CEPT, IRSM Mode
- TSR (A, B, C) Used in T1, CCS Mode
- TSR (A, B, C, D) Used in T1, Robbed Bit Mode

2.15 RECEIVE SIGNALLING REGISTERS 1 to 24/32 RSR1..32 RESET = 0 @=40H..5FH R

A	B	C	D	E	0	0	0
bit 0	1	2	3	4	5	6	7

2

- RSR (A, B, C, D) Used in CEPT, CAS Mode
- RSR (A, B, C, D, E) Used in CEPT, IRSM Mode
- RSR (A, B, C) Used in T1, CCS Mode
- RSR (A, B, C, D) Used in T1, Robbed Bit Mode

2.16 TRANSMIT DATA LINK REGISTERS (T1-DS1) TDLR RESET=0 @=0CH R/W

DL0	DL1	DL2	DL3	DL4	DL5	0	0
bit 0	1	2	3	4	5	6	7

- TDLR.DL0 Transmit data link register, containing the data that will be inserted at SERVICE BIT position (4-frames)
- TDLR.DL1
- TDLR.DL2 m bit position (ESF) and D bit position (SLC, DDS).
- TDLR.DL3 Data will be transmitted in the following order :
- TDLR.DL4
- TDLR.DL5

- 4-frames : DL0 : Fs bit of the 2nd frame.
DL1 : Fs bit of the 4th frame.
DL2 : Fs bit of the 6th frame.
DL3 : Fs bit of the 8th frame.
DL4 : Fs bit of the 10th frame.
DL5 : Fs bit of the 12th frame.
- ESF : DL0 : m bit of the 1st, 13th frames.
DL1 : m bit of the 3th, 15th frames.
DL2 : m bit of the 5th, 17th frames.
DL3 : m bit of the 7th, 19th frames.
DL4 : m bit of the 9th, 21nd frames.
DL5 : m bit of the 11th, 23th frames.
- SLC : DL0 : D bit of the 24th, 36th, 48th, 60th frames.
DL1 : D bit of the 26th, 38th, 50th, 62nd frames.
DL2 : D bit of the 28th, 40th, 52nd, 64th frames.
DL3 : D bit of the 30nd, 42nd, 54th, 66th frames.
DL4 : D bit of the 32nd, 44th, 56th, 68th frames.
DL5 : D bit of the 34th, 46th, 58th, 70th frames.
- DDS : DL0, 5 : D bit of channel 24 over 6 successive DDS frames.

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2.17 RECEIVE DATA LINK REGISTERS (T1-DS1) RDLR RESET=0 @=0DH R/W

DL0	DL1	DL2	DL3	DL4	DL5	0	0
bit 0	1	2	3	4	5	6	7

RDLR.DL0 Receive data link register, containing the data that will be extracted from SERVICE BIT position
 RDLR.DL1
 RDLR.DL2 (4-frames), m bit position (ESF) and D bit (SLC, DDS).
 RDLR.DL3
 RDLR.DL4
 RDLR.DL5

2.18 CLEAR CHANNEL REGISTER 0,1 And 2 (T1/DS1) CCR0..CCR2

CCR0	RESET=0	@=1BH	R/W				
CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
CCR1	RESET=0	@=1CH	R/W				
CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
CCR2	RESET=0	@=1DH	R/W				
CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
bit 0	1	2	3	4	5	6	7

CCR.CH1 Each bit of these 3 registers indicates transmit channels that are not carrying signalling information
 ...
 CCR.CH24 (robbed bit mode) these channels are not affected by ZCS zero suppression scheme.

2.19 TRANSMIT SPARE BITS REGISTER (CEPT) TSBR RESET=0 @=0CH R/W

Sn0	Sn1	Sn2	Sn3	Sn4	Sn5	Si0	Si1
bit 0	1	2	3	4	5	6	7

TSBR.Sn0 Transmit Spare Bits register, containing the data that will be inserted at Sn bit position.
 TSBR.Sn1
 TSBR.Sn2
 TSBR.Sn3
 TSBR.Sn4
 TSBR.Si0 Transmit Spare Bits register, containing the data that will be inserted at Si bit position.
 TSBR.Si1

2.20 RECEIVE SPARE BITS REGISTER (CEPT) RSBR RESET=0 @=0DH R/W

Sn0	Sn1	Sn2	Sn3	Sn4	0	Si0	Si1
bit 0	1	2	3	4	5	6	7

RSBR.Sn0 Receive spare bits register, containing the data that will be extracted from Sn bit position.
 RSBR.Sn1
 RSBR.Sn2
 RSBR.Sn3
 RSBR.Sn4
 RSBR.Si0 Receive Spare Bits register, containing the data that will be extracted from Si bit position.
 RSBR.Si1

2.21 IDLE REGISTER IDLE RESET=0 @=0EH R/W

bit 0	1	2	3	4	5	6	7

IDDL 8 bit data register containing the replacement word for the selected idle channels in transmission.

2.22 IDLE CHANNELS REGISTER 0,1,2 and 3 (register 3 is used only in CEPT mode)

ICR0 RESET=0 @=0FH R/W

CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
-----	-----	-----	-----	-----	-----	-----	-----

ICR1 RESET=0 @=10H R/W

CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
-----	------	------	------	------	------	------	------

ICR2 RESET=0 @=11H R/W

CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
------	------	------	------	------	------	------	------

ICR3 RESET=0 @=12H R/W

CH25	CH26	CH27	CH28	CH29	CH30	CH31	CH32
------	------	------	------	------	------	------	------

bit 0 1 2 3 4 5 6 7

ICR0...3 Each bit of these 4 registers indicates transmit channels that will be replaced by the programmable IDLE Word.

2.23 RECEIVE MASK REGISTER RMR RESET=0 @=13H R/W

bit 0	1	2	3	4	5	6	7

RMR 8 bit register containing the replacement word for the selected masked channels in reception.

2.24 MASK CHANNELS REGISTER 0,1,2 and 3 (register 3 is used only in CEPT mode)

MCR0 RESET=0 @=14H R/W

CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
-----	-----	-----	-----	-----	-----	-----	-----

MCR1 RESET=0 @=15H R/W

CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
-----	------	------	------	------	------	------	------

MCR2 RESET=0 @=16H R/W

CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
------	------	------	------	------	------	------	------

MCR3 RESET=0 @=17H R/W

CH25	CH26	CH27	CH28	CH29	CH30	CH31	CH32
------	------	------	------	------	------	------	------

bit 0 1 2 3 4 5 6 7

MCR.CH1
MCR.CH24/32 Each bit of these 3 registers indicates received channels that will be replaced by the programmable RECEIVE MASK word.

2

2.25 CHANNEL LOOPBACK ADDRESS REGISTER CLAR RESET=0 @=18H R/W

ADD0	ADD1	ADD2	ADD3	ADD4	0	0	SIG/0
bit 0	1	2	3	4	5	6	7

CLAR.ADD0 ... CLAR.ADD4 are used to select one channel among 24/32 that will be looped back from transmit side to receive path.
 CLAR.SIG (T1/DS1) When SIG=0 the channel selected by ADD0..ADD4 is looped back in all frames. When SIG=1, loop back of channels containing signalling data is disabled.

2.27 EXTRA BITS REGISTER (CEPT) XBR RESET=0 @=19H R/W

RER0	RER1	RER2	REBRF	XER0	XER1	XER2	XEBRE
bit 0	1	2	3	4	5	6	7

XBR.XER0 ... XBR.XER2 3 bits containing the transmitted extra bits : bits 4, 6 and 7 of time slot 16. (CAS signalling mode only)
 XBR.RER0 ... XBR.RER2 3 bits containing the received extra bits : bits 4, 6 and 7 of time slot 16. (CAS signalling mode only)
 XBR.REBRF=1 When RER_i have been received ⇒ Full
 XBR.XEBRE=1 When XER_i have been transmitted ⇒ Empty

2.28 PCM MODE REGISTER PMR RESET=0 @=1AH R/W

BTYP0	BTYP1	NCHA	FRUN		PCME		
bit 0	1	2	3	4	5	6	7

PMR.BTYP0, 1 selects the number of PCM buses.
 PMR.NCHA selects the number of channels in a PCM frame. When NCHA=0 the PCM bus will include 24 (48 or 96) time slots, depending on BTYP0, 1 (T1/DS1). When NCHA=1 the PCM bus will include 32 (64 or 128) time slots (CEPT).
 PMR.PCME PCM Enable. When PCME=0, PCM bus ROUT0, 1, 2, 3 are in TRI-STATE mode. When PCME=1 data output is enabled on ROUT0, 1, 2, 3, depending on TIME SLOT SWITCH TABLE programming.
 PMR.FRUN When FRUN=1, the Frame sync will be generated by 29C96 on pin "START" (Free running mode) synchronously with PCLOCK.

2.29 TIME SLOT SWITCHING REGISTERS 1 to 24/32

TSSR1..TSR32 RESET=0 @=60H.7FH R/W

TSN0	TSN1	TSN2	TSN3	TSN4	PBN0	PBN1	SM
bit 0	1	2	3	4	5	6	7

TSSR_i.TSN0, 4 ... TSSR_i.PBN0, 1 Depending on the number of PCM buses selected by bits PMR.BTYP0, 1, these 7 bits will give the correspondance between the channel number *i* (from the line side viewpoint) and the designated channel (TSN0 → 4) of the selected PCM bus (PBN0 → 1).
 TSSR_i.SM STATUS MODE. When SM=0, the corresponding channel number *i* is inactive and its content will not be transmitted on the PCM bus. The corresponding PCM bus position selected by the TIME SLOT SWITCHING reference will be in TRI-STATE mode.

2.30 TIME SLOT SWITCHING REGISTERS 25 (T1/DS1)

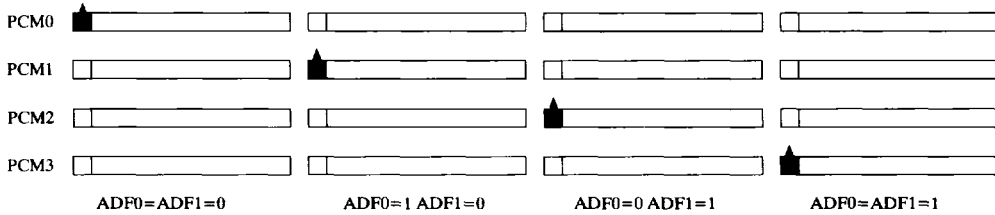
TSSR25 RESET=0 @=1EH R/W

				FBF	ADF0	ADF1	SM
bit 0	1	2	3	4	5	6	7

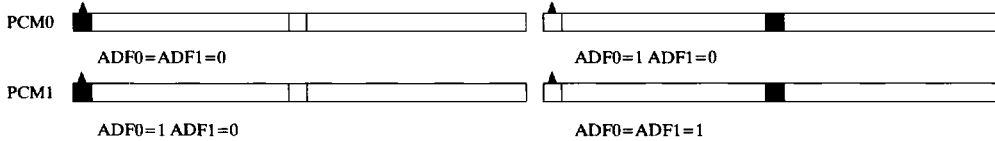
TSS25.FBF When FBF=1 it forces F bit to be send on the four Fs bit position independently of ADF [1:0] bit 5 and bit 6 of TSSR25.REG
 TSSR25.ADF[1:0] bit 5 and bit 6

■ F bit position selected ▲ START pulse

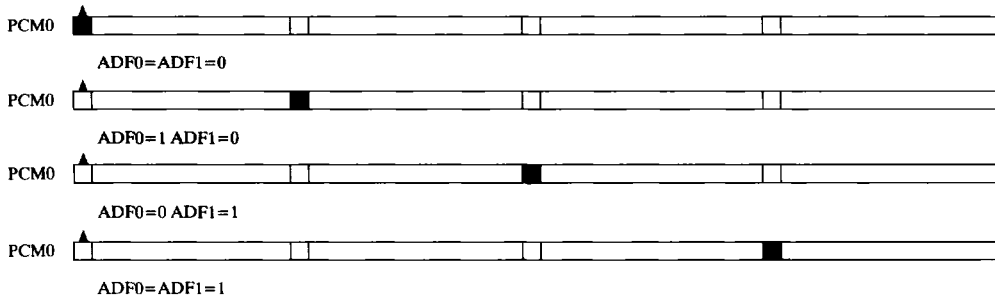
Four PCM mode



Two PCM mode



One PCM mode



TSSR25.SM Status mode. When this bit is '0', the F bit position is inactive and its content will not be transmitted on the PCM bus. The corresponding PCM bus position selected by ADF[1:0] will be in TRI_STATE mode.

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2.31 29C300 REGISTER (HOST MODE OPERATION) MXT RESET=0 @=1EH R/W

bit 0	1	2	3	4	5	6	7

In order to allow the host microprocessor to access the 29C3xx line driver via the 29C96, the MXT register is used to forward a 16-bit word through C300SDI/C300SDO, the 1st byte loaded in MXT REGISTER will be command/address byte :

R/W,	A0,	A1,	A2,	A3,	A4,	A5,	A6
	0	0	0	0	1	0	X = don't care

The MXT register is loaded with @16DEC in order to address the 29C3xx.

R/W = 1 indicates a read operation R/W = 0 indicates a write operation

The 2nd byte loaded in the MXT REGISTER will be the data byte.

D0	D1	D2	D3	D4	D5	D6	D7
LOS	DPM	EC1	EC2	EC3	REMOTE	LOCAL	TAOS

data input/output byte

LOS	DPM	EC1	EC2	EC3	REMOTE	LOCAL	TAOS
bit 0	1	2	3	4	5	6	7

bit D5 (Remote)	bit D6 (Local)	bit D7 (TAOS)	Status
0	0	0	reset has occurred or no program input
0	0	1	TAOS active
0	1	0	local loopback active
0	1	1	TAOS and local loopback active
1	0	0	remote loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed since last DPM and Clear LOS occurred

All data written into MXT at address @1EH will be transferred serially to the 29C3xx through SDI serial output. A read access at address @1EH will initiate a serial transmission from 29C3xx to the 29C96 via SDO input.

Electrical Characteristics

Absolute Maximum Ratings

VCC to GND -0.5 V to +7 V
 Input/Output Voltage -0.3 V to VCC + 0.3 V
 Storage Temperature -65 to 150°C

Operating Conditions

Voltage Range 4.5 V to 5.5 V
 Temperature Range (commercial) 0 to 70°C
 Temperature Range (industrial) -40 to 85°C

DC Electrical Characteristics

Parameter	Conditions	Min	Max	Unit
low level input voltage	VIL I = 5µA		0.8	V
high level input voltage	VIH I = 5µA	2.2		V
input leakage current	Ileak		5	µA
3 STATE output leakage current	IOL		10	µA
low level output voltage	VOL I = -6.4 mA		0.4	V
high level output voltage	VOH I = 6.4 mA	2.4		V
standby current	ICCS VCC = 5.5 V		200	µA
operating current	ICCOP VCC = 5 V, 20 MHz clock		100	mA

2

AC Timings

29C3xx Interface All outputs are connected to a 50 pF capacitor

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
tcsout	C300SCLK to C300CS out			15	ns	
tprselk	RCLOCK to C300SCLK delay			50	ns	
tdes	C300SDO to C300SCLK setup time	50			ns	
tedh	C300SCLK to C300SDO hold time	50			ns	
tch	C300SCLK high time	200			ns	
tcl	C300SCLK low time	200			ns	
tedv	C300SCLK to C300SDI valid			50	ns	
tedz	C300CS to C300SDI high Z			50	ns	10 mA pull up
tcwh	C300CS inactive time	1. × C300SCLK period			ns	

Driver Interface

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
txout	XCLOCK to XOUTP/XOUTN out			25	ns	
tsrd	RINP/RINN to RCLOCK setup time	50				
thrd	RCLOCK to RINP/RINN hold time	50			ns	

Data/Signal Link Interface

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
tdlr	DRCLOCK to RDL delay			50	ns	
tsdx	XDL to DXCLOCK setup time	50			ns	
thdx	DXCLOCK to XDL hold time	50			ns	
tsigr	SIRCLOCK to RABCD delay			50	ns	
tsrx	XABCD to SIXCLOCK setup time	50			ns	
thrx	SIXCLOCK to XABCD hold time	50			ns	

Microprocessor Interface

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
tcsmin	\overline{CS} minimum pulse width	3MCLK				
trdmin	RD minimum pulse width	3MCLK				
tadrd	address/(RD, \overline{CS}) low set up time	0			ns	
trdad	(RD + \overline{CS}) high/address hold time	0			ns	
trdyzl	RD/ \overline{WR} and \overline{CS} low to RDY low (registers)	3MCLK		6MCLK		
trdylz	RD/ \overline{WR} or \overline{CS} high to RDY high Z			35	ns	10 mA pull up load
tdryzh	RD/ \overline{WR} and \overline{CS} low to RDY high (registers)			25	ns	
trddata	RD and \overline{CS} low to data valid delay			6MCLK		
twrmin	\overline{WR} minimum pulse width	3MCLK				
tadwr	address (write, \overline{CS})/low set up time	0			ns	
twrad	(\overline{WR} + \overline{CS}) high/address hold time	0			ns	
tdatas1	Data set up time to (\overline{WR} , \overline{CS}) Low	0			ns	
tdatah1	(\overline{WR} + \overline{CS}) high/Data hold time	0			ns	

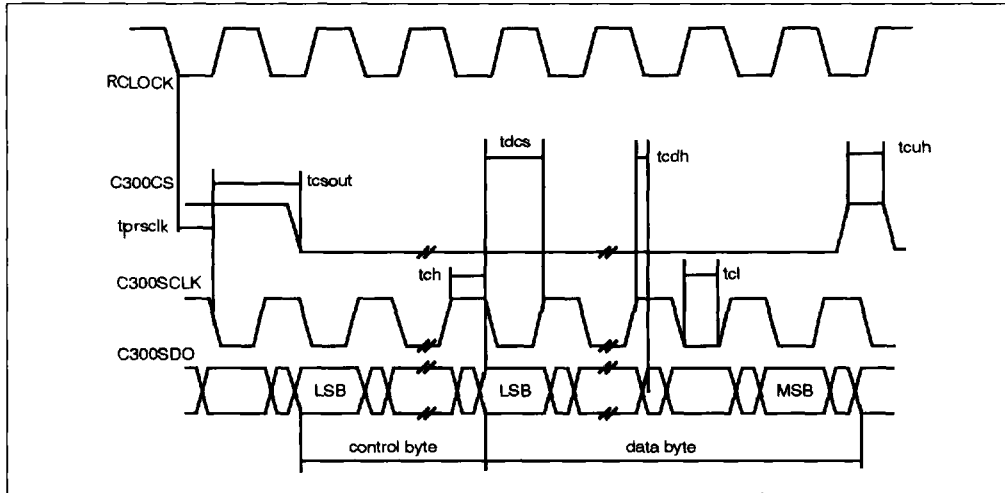
PCM Interface

Simple Clock Mode

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
tdr	START to ROUT delay			25	ns	
tstart	min START pulse width	2PCLOCK		16PCLOCK	ns	
tsxin	XIN to PCLOCK setup time	10			ns	
thxin	PCLOCK to XIN hold time	25			ns	
tdr1	PCLOCK to ROUT delay			35	ns	
tdr2	PCLOCK to ROUT high Z delay			25	ns	10 mA pull up load

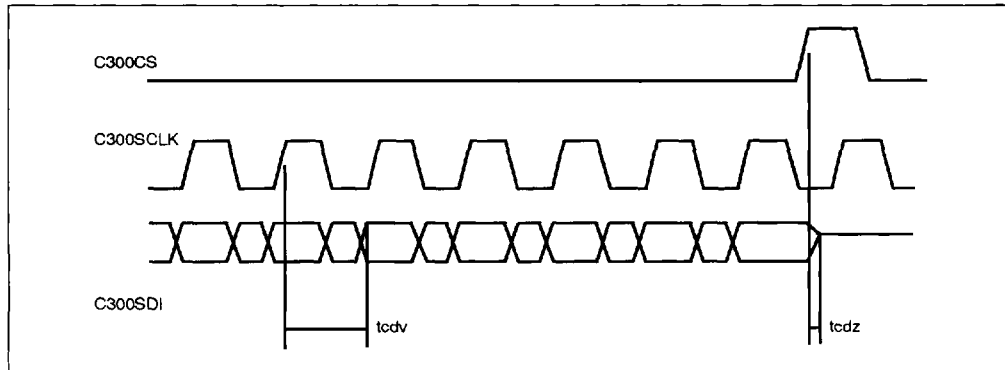
29C3XX Interface AC Timing

29C3XX Serial Data in Timing Diagram



2

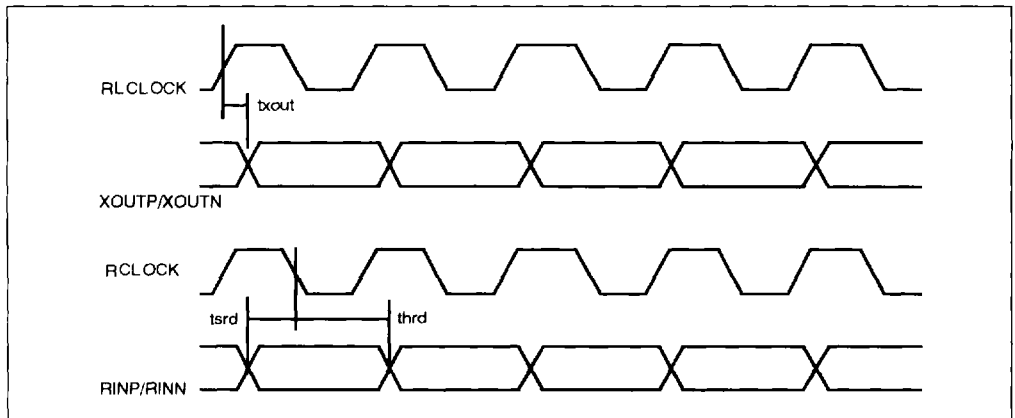
29C3XX Serial Data Output Timing Diagram



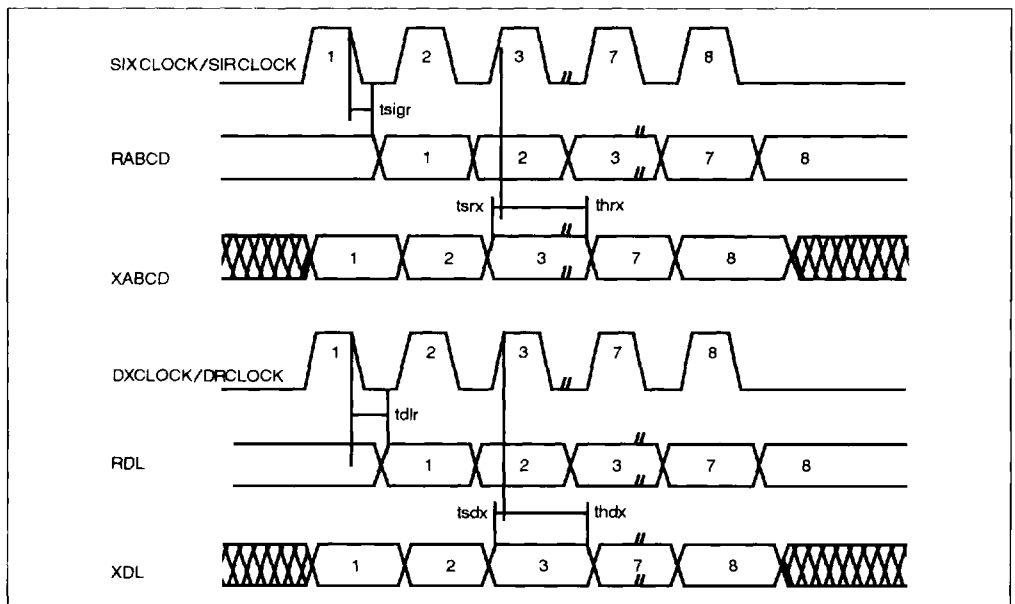
29C96

Driver Interface / Data signalling Link AC Timing

Driver Interface Timing

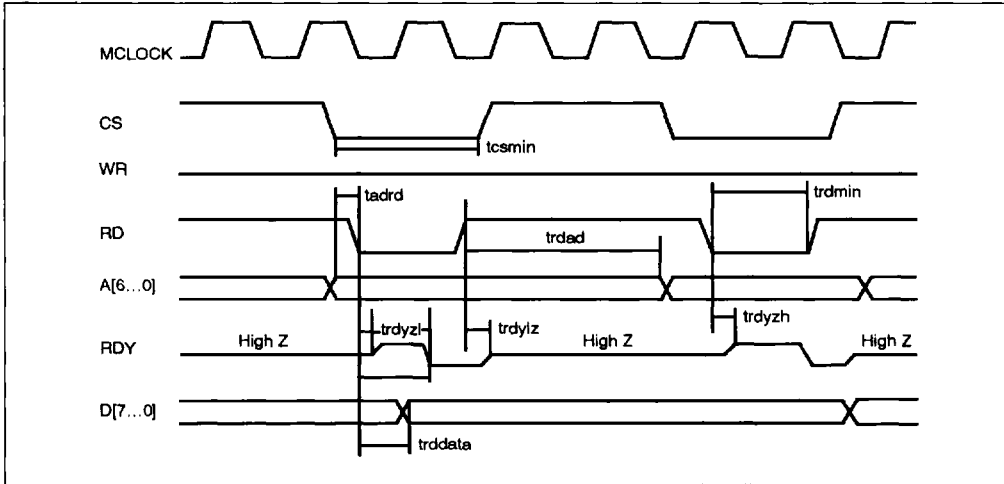


Data/signalling Timing



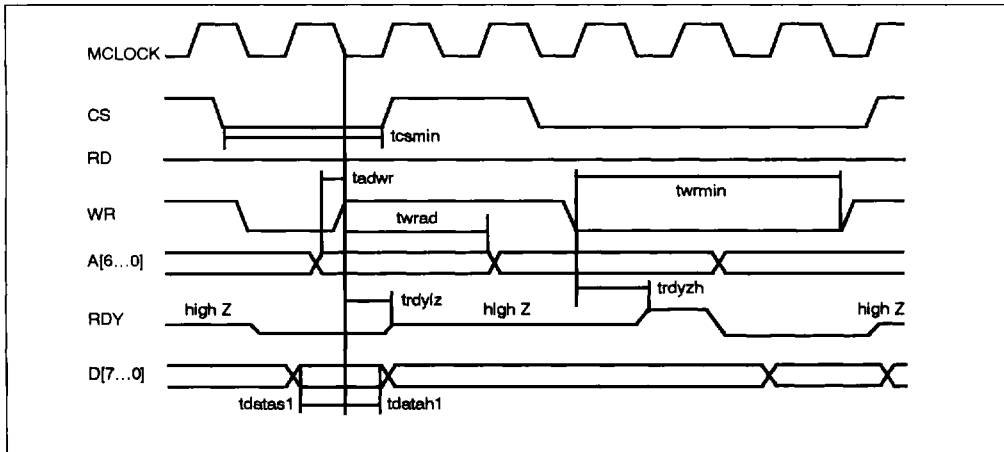
Microprocessor Interface Timing

RAM/Register Read



2

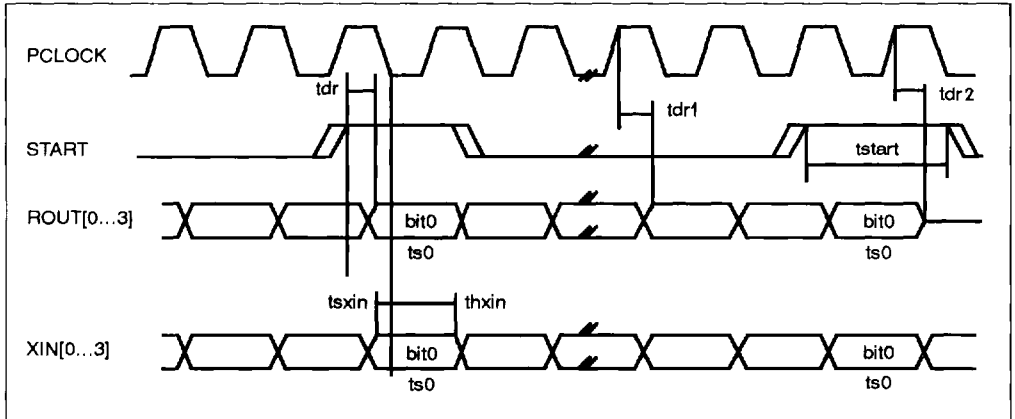
RAM/Register Write



29C96

PCM Interface Timing

Simple Clock Mode



29C96 Programming

1 Line Format

Line format (DS1 or CEPT) is selected via `MODE.mode` :

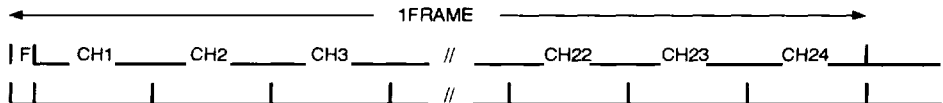
- mode=0 : DS1 mode
- mode=1 : CEPT mode

2 Frame Organization

2-1 T1/SD1 Mode.

The T1 primary rate interface is a 1.544 MHz serial link. Each frame is organized in 24×8 bits time slots transmitted at 64 kbit/s. An F bit marking the frame boundary is transmitted before the 24 time slots. The use of the F depends on the superframe organization. Superframe structure can change from 4 frames to 72 frames depending on the selected format.

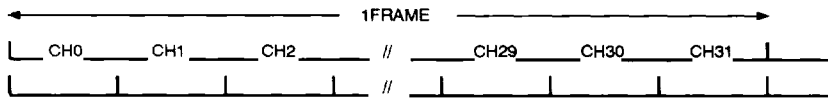
FRAME : Bit 1 = F bit, Bit 2 to 193 = 24×8 bits/64 kbit/s channels' transmitted LSB first, channel 1 first. Frequency of frame is 8 kHz.



2-2 CEPT Mode

The CEPT primary rate interface is a 2.048 MHz serial link. Each frame is organized in 32×8 bits time slots transmitted at 64 kbit/s. Superframe structure can change from 2 frames to 16 frames depending on the selected format.

FRAME : bit 1 to 256 = 32×8 bits/64 kbit/s channels' (0 to 31) transmitted LSB first, channel 0 first. Frequency of frame is 8 kHz.



3 Superframe Organization

3.1 T1/DS1 Mode

4 Frame Organization

DESCRIPTION : 4-FRAME = 4 frames at 8 kHz.

The frame alignment is provided in every Ft bit (F bit of frame 1 & 3). F bit of frames 2 & 4 is used for service bit : Fs. The alignment pattern in each frame is as follows :

Content of F bit :

	Ft	Fs
Frame 1	1	
Frame 2		service bit
Frame 3	0	
Frame 4		service bit

The 4 Frame Programming

Ft bit : If MODE.TTF = 1, Ft bits are provided directly in data flow at input port : XIN0, 3 (external Ft bit generation) in respect with 29C96 transmit clocks, and programming on the TIME SLOT SWITCH TABLE. (see PMR register). If MODE.TTF = 0, Ft bits are internally generated by the 29C96. When MODE.RTF = 0, Ft bits are directly output at port ROUT0, 3, depending of the TIME SLOT SWITCH TABLE programming. When MODE.RTF=1, Ft bits are replaced by a '1'.

Frame Bit Error

Ft bit (received data stream) is tested for alignment. When an Ft error is detected, then ERROR.FBE is set to 1 and Ft errors are counted in a 16 bits Framing Error Counter (FEC0 and FEC1 8 bits registers). Upon saturation of this counter, ERROR.FCO is set to "1". If MASK.FCO = 1, the interrupt is enabled and INT pin is activated.

Service Bit

If MODE.DL = 1 SERVICE bits are latched synchronously with FRAMER clock XDLCLOCK at DATA LINK input port XDL, (external SERVICE bits generation). The received SERVICE bits are output synchronously with clock RDLCLK at DATALINK output port RDL. When MODE.DL is = 0, the SERVICE bits are sourced from TDLR.DL0,5 register and included in the transmitted data stream. On the receive side, SERVICE bits are stored in RDLR.DL0, 5 register.

Ya Alarm

The transmission of a REMOTE FRAME ALARM or YELLOW ALARM is programmed by setting TCR.Ya to '1'. The bit 2 of each channel is set to '0'. Upon detection of a REMOTE FRAME ALARM (bit 2 of every channel being '0') in the received data stream, the bit ALARM.Ya is set to '1'. If MASK.Ya is also set to "1" the interrupt is enabled and INT pin is activated.

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D4 Multiframe Organization

DESCRIPTION : D4 MULTIFRAME = 12 frames (1 to 12) at 8 kHz.

FRAME and MULTIFRAME ALIGNMENT : The frame alignment is provided in every Ft bit (F bit of odd frames). F bits of even frames contain multiframe alignment pattern : (Fs bits).

	Ft	Fs
FRAME 1	1	
FRAME 2		0
FRAME 3	0	
FRAME 4		0
FRAME 5	1	
FRAME 6		1
FRAME 7	0	
FRAME 8		1
FRAME 9	1	
FRAME 10		1
FRAME 11	0	
FRAME 12		Ya

Ya : REMOTE FRAMING ALARM or YELLOW ALARM

The D4 Programming

FT BIT - If MODE.TTF = 1, Ft bits are provided directly in data flow at input port XIN[0...3] (external Ft bit generation) in respect with 29C96 transmit clocks, and programming of the TIME SLOT SWITCH TABLE. If MODE.TTF = '0', the Ft bits are internally generated by the framer. When MODE.RTF = 0, Ft bits are directly output at port ROUT[0...3], depending of the TIME SLOT SWITCH TABLE programming. When MODE.RTF='1', Ft bits are forced to '1'.

Fs BIT - If MODE.TTF = 1, Fs bits are provided directly in data flow at the input port XIN[0...3] (external Fs bit generation) in respect with transmit clocks and programming of the TIME SLOT SWITCH TABLE. If MODE.TTF=0, the Fs bits are internally generated by the framer. When MODE.RTF=0, Fs bits are directly output at port ROUT[0...3], depending on the TIME SLOT SWITCH TABLE programming. When MODE.RTF=1, Fs bits are forced to '1'.

Frame Bit Error

Ft and Fs bits of received data stream are tested for alignment. When an Ft or Fs error is detected, the ERROR.FBE=1 and Ft or Fs errors are counted in the 16 bits Framing Error Counter (FEC0 and FEC1 8 bits registers). Upon saturation of this counter, ERROR.FCO is set to '1'. If MASK.FCO = 1, an interrupt is enabled and INT pin is activated.

Ya Alarm

The transmission of a REMOTE FRAME ALARM or YELLOW ALARM is programmed by setting TCR.Ya to '1'. The alarm mode depends on TCR.YAM. If the YAM = 0, every bit 2 of each channel is set to '0'. When YAM=1, the 12th Fs bit is set to 1. Upon detection of a REMOTE FRAME ALARM (bit 2 of every channel being '0' or 12th Fs bit being '1') in the received data stream, ALARM.Ya is set to '1'. If MASK.Ya is = 1, then an interrupt is enabled and INT pin is activated.

ESF Multiframe Organization

DESCRIPTION : ESF MULTIFRAME : 24 frames (1 to 24) at 8 kHz.

FRAME and MULTIFRAME ALIGNMENT : The frame alignment is provided in every FAS bit (F bit of frames 4, 8, 12, 16, 20, 24). F bit of odd frames contains data link bits : (FDL).

The CRC6 of previous frame is located in F bits of frames 2, 6, 10, 14, 18, 22.

	FAS	FDL	CRC	
FRAME 1		m		A signalling
FRAME 2			CRC1	
FRAME 3		m		
FRAME 4	0			
FRAME 5		m		
FRAME 6			CRC2	
FRAME 7		m		B signalling
FRAME 8	0			
FRAME 9		m		
FRAME 10			CRC3	
FRAME 11		m		
FRAME 12	1			
FRAME 13		m		C signalling
FRAME 14			CRC4	
FRAME 15		m		
FRAME 16	0			
FRAME 17		m		
FRAME 18			CRC5	
FRAME 19		m		D signalling
FRAME 20	1			
FRAME 21		m		
FRAME 22			CRC6	
FRAME 23		m		
FRAME 24	1			

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ESF Programming

FAS bit : If MODE.TTF='1', FAS bits are provided directly in data flow at input port XIN[0...3] (external Fas bit generation) in respect with transmit clocks from the 29C96 and programming if the TIME SLOT SWITCH TABLE. If MODE.TTF = '0', the Ft bits are internally generated by the framer. When MODE.RTF=0, Fs bits are directly output a port ROUT[0...3], depending on the TIME SLOT SWITCH TABLE programming. When MODE.RTF=1, Fas bits are forced to '1'.

Frame Bit Error

Fas bits in the receive data stream are tested for alignment. When a Fas error is detected, ERROR.FBE is set to '1' and Fas errors are counted in the 16 bits Framing Error Counter (FEC0 and FEC1 8 bits registers). Upon saturation of this counter, ERROR.FCO is set to '1'. If MASK.FCO is set to '1', an interrupt is enabled and INT pin is activated.

CRC - When MODE.TTF is '0', the CRC6 check bits are internally computed and inserted in the transmitted data flow. In the received data path, CRC6 is computed with data of the current SUPERFRAME and checked with the content of the

next SUPERFRAME at the CRC bit positions. The CRC6 checking method follows the G.704 CCITT recommendation.

If MODE.TTF='1', the corresponding CRC bit positions are transmitted unchanged (external CRC generation). When the internal CRC generation is selected via bit MODE.TTF=0, FCR.ICRC=1 allows user to transmit an inverted CRC6. This can be done to monitor the CRCX error detection and CRC error counter in one of the LOOP-BACK modes. When MODE.RTF=0, CRC bits are directly output at port ROUT[0...3], depending on the TIME SLOT SWITCH TABLE programming. When MODE.RTF=1, CRC bits are forced to '1'.

CRC ERROR - CRC bits in the received data stream are tested for multiframe alignment. When a CRC error is detected, ERROR.CRCE is set to '1' and CRC errors are counted in the 16 bits. CRC Error Counter (CEC0 and CEC1 8 bits registers). Upon saturation of this counter, ERROR.CCO is set to '1', if MASK.CCO is also set 1, an interrupt is enabled and INT output is activated. CRC6 errors are externally indicated at output port CRCE. Once a CRC mismatch is detected in an ESF multiframe, the signal CRCE goes high, until the end of the current multiframe.

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FDL - When **MODE.DL=1**, FDL bits are latched at **DATA LINK** input port **XDL**, synchronously with **FRAMER** clock **XDLCLOCK**. The received FDL bits are output at **DATA LINK** output port **RDL**, synchronously with **RDLCLOCK**.

When **MODE.DL=0**, FDL bits are sourced from **TDLR.DL0,5** register and included in the transmitted data stream. On the receive side, the received FDL bits are stored in **RDLR.DL0,5** register.

Ya ALARM - The transmission of a **REMOTE FRAME ALARM** or **YELLOW ALARM** is programmed by setting **TCR.Ya** to '1'. The alarm mode depends on **TCR.YaM**. If **YaM=0**, every bit 2 of each channel is set to '0'. When **YaM=1**, the content of the FDL bits is repeatedly..1111111100000000... (FF00 hex). Upon detection of a **REMOTE FRAME**

ALARM (bit 2 of every channel being '0' or FDL is a repeated FF00) in the received data stream, **ALARM.Ya** is set to '1'. If **MASK.Ya** is also set to '1' then an interrupt is enabled and **INT** output is activated.

SLC Organization – Description :
SLC = 72 frames (1 to 72) at 8 kHz.

Frame and Multiframe Alignment :

The frame alignment is provided in every **Ft** bits (**F** bit of odd frames). **F** bit of even frames from 0 to 24 contains multiframe alignment bits : (**Fs** bits). **F** bit or even frames from 25 to 72 contain the data link message (**D** bits).

	Ft	Fs	
FRAME 1/13	1		A/C signalling
FRAME 2/14		0	
FRAME 3/15	0		
FRAME 4/16		0	
FRAME 5/17	1		
FRAME 6/18		1	
FRAME 7/19	0		
FRAME 8/20		1	
FRAME 9/21	1		
FRAME 10/22		1	
FRAME 11/23	0		
FRAME 12		0	
FRAME 24		D	
FRAME 25/37/49/61	1		A/C signalling
FRAME 26/38/50/62		D	
FRAME 27/39/51/63	0		
FRAME 28/40/52/64		D	
FRAME 29/41/53/65	1		
FRAME 30/42/54/66		D	
FRAME 31/43/55/67	0		
FRAME 32/44/56/68		D	
FRAME 33/45/57/69	1		
FRAME 34/46/58/70		D	
FRAME 35//47/59/71	0		
FRAME 36/48/60		D	
FRAME 72		0	

The SLC Programming-

FT BIT - If **MODE.TTF=‘1’**, **Ft** bits are provided directly in dataflow at input port **XIN[0...3]** (external **Ft** bit generation) in respect with transmit clocks from the 29C96, and programming of the **TIME SLOT**

SWITCH TABLE. If **MODE.TTF = ‘0’**, the **Ft** bits are internally generated by the framer. When **MODE.RTF=0**, **Ft** bits are directly output at port **ROUT[0...3]**, depending on the **TIME SLOT SWITCH TABLE** programming. When **MODE.RTF=1**, **Ft** bits are forced to '1'.

FS BIT - If **MODE.TTF**='1', **F_s** bits are provided directly in data flow at the input port **XIN[0...3]** (external **F_s** bit generation) in respect with transmit clocks from the 29C96, and programming of the **TIME SLOT SWITCH TABLE** programming. When **MODE.RTF**=1, **F_s** bits are forced to '1'.

FRAME BIT ERROR - **F_t** and **F_s** bits in the receive data stream are tested for alignment. When an **F_t** or **F_s** error is detected, **ERROR.FBE** is set to '1' and **F_t** or **F_s** errors are counted in the 16 bits Framing Error Counter (**FEC0** and **FEC1** 8 bits registers). Upon saturation of this counter, **ERROR.FCO** is set to '1'. If **MASK.FCO** = 1, then an interrupt is enabled and **INT** output is activated.

D Bits - When **MODE.DL**=1, the **D** bits are latched at **DATA LINK** input port-**XDL**, synchronously with

FRAMER clock **XDLCLOCK** (external **FDL** bit generation). The received **D** bits are output at **DATA LINK** output port **RDL**, on clock **RDLCLOCK**. When **MODE.DL**=0, the **D** bits are sourced from **TDLR.DL0,5** register and included in the transmitted data stream. In the receive side, the received **D** bits are stored in **RDLR.DL0,5** bits.

Ya ALARM - The transmission of a **REMOTE FRAME ALARM** or **YELLOW ALARM** is programmed by setting **TCR.Ya** to '1'. In that case every bit 2 of each channel is set to '0'. Upon detection of a **REMOTE FRAME ALARM** (bit 2 of every channel being '0') in the received data stream, **ALARM.Ya** is set to '1'. If **MASK.Ya** is also set to '1' then an interrupt is enabled and **INT** output is activated.

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Digital Data Service (DDS)

DESCRIPTION - **DDS MULTIFRAME** is equivalent to the **D4** format with a special use of channel 24. The channel 24 contains a framing pattern, an alarm position and a data link bit. No signalling mode is allowed in **DDS** format. The content of channel 24 is as follow :

bit	1	2	3	4	5	6	7	8
	1	0	1	1	1	Ya	D	0

Ya : Remote frame alarm (active low). D : data link bit.

THE DDS PROGRAMMING - Selection of **DDS** format is done by bits **MODE.smode0, 1**. When selected, the **DDS** format will override the use of bit **MODE.fmode0, 1** and discard any signalling mode.

Ya ALARM - The transmission of a **REMOTE FRAME ALARM** or **YELLOW ALARM** is programmed by setting **TCR.Ya** to '1'. When set, bit 6 of channel 24 is set to '0'.

D BIT - If **MODE.DL**=1, **D** bits are latched at **DATA LINK** input port **XDL**, synchronously with **FRAMER** clock **XDLCLOCK** (external **D** bits generation). The received **D** bits are output at **DATA LINK** output port **RDL**, on clock **RDLCLOCK**. When **MODE.DL** = 0, the **D** bits are sourced from **TDLR.DL0,5** register and included in the transmitted data stream. On the receive side, the **D** bits are stored in **RDLR.DL0,5** register.

3.2 CEPT Mode

Double Frame Organization : Doubleframe = 2 frames (**N** & **N+1**) at 8 kHz.

The frame alignment is provided in every channel 0 of frames **N** (**FAS** word) and **N+1** (Service bit : bit **n^o 2**) The 1st bit of frames **N** and **N+1** contains the international bit : (**Si**). The bits 4 to 8 of frames **N+1** contain the national bit : **Sn** the bit 3 of frames **N+1** contains the yellow alarm bit **Ya**. The alignment pattern in each frame is as follows :

CONTENT OF CHANNEL 0 OF FRAMES N & N+1

BIT Number	1	2	3	4	5	6	7	8
frame N alignment	Si0	0	0	1	1	0	1	1
frame N+1 alignment	Si1	1	Ya	Sn0	Sn1	Sn2	Sn3	Sn4

Si : International bit. Fixed to '1' if unused. Sn : National bits. Fixed to '1' if unused. Ya : Yellow alarm. '0' when no alarm. '1' when alarm indication.

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The Double Frame Programming

FAS - See MODE register.

Ya ALARM - see ALARM register

Sn Bits - If MODE.Sn = 1, the National Spare bits 0 to 4 are latched at input port: XIN[0...3], synchronously with FRAMER clocks (external Sn bits generation), and depending on programming of the TIME SLOT SWITCH TABLE. The received Sn bits are output on the selected output PCM ROUT[0...3], according to the TIME SLOT SWITCH TABLE. When MODE.Sn=0 the Sn bits are sourced from the internal register TSBR.Sn0, 4 (Sn bits 0 to 4 of Transmit Spare Bits Register) and included in the transmitted data stream. On the received side, the received Sn bits are stored in RSB.R.Sn0, 4 register.

Si BITS - If MODE.Si=1, the International Spare bits 0 and 1 are latched at input port: XIN0, 3, synchronously with FRAMER clocks (external Si bits generation), and depending on programming of the TIME SLOT SWITCH TABLE. The received Si bits are output at output PCM ROUT0, 3, according to the

TIME SLOT SWITCH TABLE. When MODE.Si=0, the Si bits are sourced from TSBR.Si0, 1 register and included in the transmitted data stream. On the receive side, the received Si bits are stored in the internal RSB.R.Si0, 1 register.

CRC4 Multiframe Organization

Multiframe : 16 frames (0 to 15) at 8 kHz.

Frame & Multiframe Alignment :

The frame alignment is provided in each channel 0 of even frames (FAS word) and odd frames (Service bit : bit n° 2).

CRC4 is located in 1st bit of channel 0 of even frames. Multiframe alignment signal is located in odd frames 1 to 11. The 1st bit of frames 13 and 15 carry the international bit (Si) or indication of submultiframes received with CRC error, from the remote end. The bits 4 to 8 of every odd frames contain the national bits Sn. The bit 3 of every odd frame contains the yellow alarm bit Ya.

CONTENT OF CHANNEL 0 OF FRAMES 0 to 15

	BIT NUMBER	1	2	3	4	5	6	7	8
SUBMULTIFRAME 0	FRAME 0	CRC1	0	0	1	1	0	1	1
	FRAME 1	0	1	Ya	Sn0	Sn1	Sn2	Sn3	Sn4
	FRAME 2	CRC2	0	0	1	1	0	1	1
	FRAME 3	0	1	Ya	Sn0	Sn1	Sn2	Sn3	Sn4
	FRAME 4	CRC3	0	0	1	1	0	1	1
	FRAME 5	1	1	Ya	Sn0	Sn1	Sn2	Sn3	Sn4
	FRAME 6	CRC4	0	0	1	1	0	1	1
	FRAME 7	0	1	Ya	Sn0	Sn1	Sn2	Sn3	Sn4
	FRAME 8	CRC1	0	0	1	1	0	1	1
	FRAME 9	1	1	Ya	Sn0	Sn1	Sn2	Sn3	Sn4
	FRAME 10	CRC2	0	0	1	1	0	1	1
	FRAME 11	1	1	Ya	Sn0	Sn1	Sn2	Sn3	Sn4
	FRAME 12	CRC3	0	0	1	1	0	1	1
	FRAME 13	Si	1	Ya	Sn0	Sn1	Sn2	Sn3	Sn4
	FRAME 14	CRC4	0	0	1	1	0	1	1
	FRAME 15	Si	1	Ya	Sn0	Sn1	Sn2	Sn3	Sn4

Si : International bit. Fixed to '1' if unused - Sn : National bits. Fixed to '1' if unused - Ya : Yellow alarm. '0' : no alarm. '1' : alarm, CRC : CRC4 bits.

The CRC4 Programming

In CRC4 mode, the 29C96 automatically generates the CRC4 of submultiframes 0 and 1 (bit 1 of even frames) and the multiframe alignment pattern (bit 1 of odd frames 1 to 10).

FAS - see MODE register.

Ya ALARM - see ALARM register.

Sn BITS - If MODE.Sn=1, the National Spare bits 0 to 4 are latched at input port XIN[0...3], synchronously with FRAMER clocks (external Sn bits generation), and depending on programming of the TIME SLOT SWITCH TABLE. The received Sn bits are output at output PCM ROUT[0...3] according to the TIME SLOT SWITCH TABLE. When tMODE.Sn=0, the Sn bits are sourced from TSBR.Sn0, 4 register and included in the transmitted data stream. On the receive side, the received Sn bits are stored in RSBR.Sn0, 4 register.

Si BITS - If MODE.Si=1, the International Spare bits 0 and 1 are latched at input port XIN[0...3], synchronously with FRAMER clocks (external Si bits generation), and depending on programming of the TIME SLOT SWITCH TABLE. The received Si bits are output at output PCM ROUT[0...3] according to the TIME SLOT SWITCH TABLE. When MODE.Si=0, the Si bits are sourced from TSBR.Si0, 1 register and included in the transmitted data stream. On the receive side, the received Si bits are stored in RSBR.Si0, 1 register.

CRC - When the internal CRC4 generation is selected via MODE.fmode0, FCR.ICRC=1 allows user to transmit an inverted CRC4. This can be done to monitor the CRC error detection and CRC error counter in one of the LOOPBACK modes.

CRC ERROR - CRC bits in the receive data stream are tested for multiframe alignment. When a CRC error is detected for one of the two submultiframes 0 and 1, ERROR.CRCE0 or ERROR.CRCE1 are set to '1' and CRC errors are counted in the 16 bit CRC Error Counter (CEC0 and CEC1 8 bits registers). Upon saturation of this counter, ERROR.CCO (CRC error Counter Overflow of register ERROR) is set to 1. If MASK.CRCE or MASK.CCO of the interrupt mask register is also set to 1 then an interrupt is enabled and INT output is activated. CRC4 errors are

externally indicated at output port CRCE. Once a CRC mismatch is detected in a CRC4 submultiframe, the signal CRCE goes high, until the end of the current submultiframe.

CRC STATUS - When FCR.ACSI=1, any CRC error in one of the two submultiframes 0 and 1, as indicated in the bits ERROR.CRCE0 or ERROR.CRCE1, is reported to remote end. This is done by setting Si bit of frame 13 (for submultiframe 0 CRC error) and Si bit of frame 15 (submultiframe 1 CRC error) to '0'. The reception of a '0' in Si bits of frames 13 and 15 will be reported in SSR.ECRC0 and SSR.ECRC1. This status will indicate CRC errors in the previous transmitted submultiframes 0 and 1. If MASK.ECRC of interrupt mask register is also set to 1 then an interrupt is enabled and INT output is activated.

4 Multiframe Signalling

4.1 T1/DS1 Mode

The 29C96 allows 3 signalling modes : transparent, channel 24 CCS (Common Channel Signaling) or robbed bit. The 29C96 includes also the DDS multiframe format. Selection of signalling modes or DDS format is done by bits MODE.smode0, 1 in order to prevent the use of DDS format in conjunction with one of the signalling modes. In the transparent mode, signalling is not supported by the 29C96 and the transmitted data is sent unchanged on the line. On the receive side, signalling data will be ignored. The 29C96 also includes clear channel capability, this is useful to avoid the corruption of data channels with signalling information. Signaling source can be the external input/output ports XABCD and RABCD or internal signalling RAMs. The signalling RAMs support 1 to 4 bits of signalling data in robbed bit mode and up to 8 bits in CCS mode. This data is located in registers TSR1,24 and RSR1, 24. Content of signalling registers is as follow :

bit	1	2	3	4	5	6	7	8
Signaling register	A	B	C	D	E			

Common Channel Signaling

In this signalling mode, the 8 bits of channel 24 on 24 consecutive frames (independently of multiframe structure selected) are used to carry the signalling data. When the source of signalling data is external, (XABCD input port), 8 successive bits are latched and included in the transmitted data stream and channel

24 is loaded with data received at port RABCD. When the source is the internal signalling RAM, the 8 bits of registers TSR1 to TSR24 are transmitted on the line, and the received channel 24 are stored in the registers RSR1 to RSR24.

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The content of channel 24 is as follows :

frame number	bit used channel 24							
	1	2	3	4	5	6	7	8
1	A13	A1	B1	X	X	X	1	X
2	A14	A2	B2	X	X	X	1	X
3	A15	A3	B3	X	X	X	1	X
4	A16	A4	B4	X	X	X	1	X
5	A17	A5	B5	X	X	X	1	X
6	A18	A6	B6	X	X	X	1	X
7	A19	A7	B7	X	X	X	1	X
8	A20	A8	B8	X	X	X	1	X
9	A21	A9	B9	X	X	X	1	X
10	A22	A10	B10	X	X	X	1	X
11	A23	A11	B11	X	X	X	1	X
12	1	A12	B12	X	X	X	1	X
13	A1	A13	B13	X	X	X	1	X
14	A2	A14	B14	X	X	X	1	X
15	A3	A15	B15	X	X	X	1	X
16	A4	A16	B16	X	X	X	1	X
17	A5	A17	B17	X	X	X	1	X
18	A6	A18	B18	X	X	X	1	X
19	A7	A19	B19	X	X	X	1	X
20	A8	A20	B20	X	X	X	1	X
21	A9	A21	B21	X	X	X	1	X
22	A10	A22	B22	X	X	X	1	X
23	A11	A23	B23	X	X	X	1	X
24	A12	1	1	1	0	Ys	0	1

Bit Robbing Signaling

Signaling data corresponds bit 8 of every channel of the signalling frames. Signaling scheme is not valid in 4-FRAME format. In D4 format, signalling is included in frames 6 and 12. Only 0,2 and 4 states signalling is valid for D4 format. In ESF format, signalling is inserted in frames 6, 12, 18 and 24. In SLC format signalling is sent every 6 frames, starting at frame 6 (6, 12, 18 ... 66).

The Signaling Programming

SIGNALLING MODE : The signalling mode is selected in register **MODE** by programming **MODE.smode0** and **MODE.smode1**.

SIGNALLING mode selection.

	LSCR.RSB1	LSCR.RSB0
Transparent	0	0
bit robbing	0	1
CCS	1	0
DDS	1	1

ABCD

The source and destination of signalling data is selected by LSCR.SIGSRC. When SIGSRC='1', ABCD data are latched at input port XABCD for the transmit side and output at port RABCD for receive side. When SIGSRC='0', ABCD data are loaded/stored from/in the signalling RAM, (XSR1 to XSR24 for transmission and RSR1 to RSR24 for reception).

Each of the transmit signalling registers (XSR1 to XSR24) and receive signalling registers (RSR1 to RSR24) are 8 bits registers, directly addressable by the host microprocessor. After transmission or reception of a complete signalling RAM, the bits MSR.SRE and MSR.SRF are set to 1. If MASK.SRE or MASK.SRF=1, an interrupt is enabled and INT output is activated.

ROBBED BITS STATES - The number of robbed bit states is selected by LSCR.RBS0 and LSCR.RB1 according to the following table :

Robbed bit states selection.

	LSCR.RSB1	LSCR.RSB0
2 STATE	0	0
4 STATE	0	1
16 STATE	1	0
unused	1	1

In case of a 2-state mode, the bit B, C and D are replaced by the A bits. In the 4-states mode, the C bit carry a A information and D bit, a B information. In the 16-states mode, ABCD data configuration is as indicated previously.

CLEAR Channel

Clear channel operation is possible in the 29C96 by simply programming the individual channels that does

not carry signalling information or ZCS zero suppression method. This is done by setting to '1' the bit corresponding to the selected channel in one of the CLEAR CHANNEL registers : CCR0, CCR1, CCR2.

CCS : In common channel signalling mode, the A to H data are taken from registers XSR1 to XSR24, or latched at port XABCD depending of the bit LSCR.SIGSRC. The 8 bits of the signalling registers 1 to 24 (or 8 consecutive bits of external data) are placed in the time slot 24 of 24 consecutive frames, starting with register XSR1 in frame 1.

Transmission of a complete signalling RAM is made within 2 multiframes in D4 format and 1 multiframe in ESF. In SLC format, signalling RAM can be sent 3 times within 2 multiframes. Similarly, data received in the channel 24 will be stored in the receive signalling RAM (RSR1 to RSR24) or output at port RABCD depending on the value of bit LSCR.SIGSRC. Storage of the 8 bits data in the receive registers is done in the same manner as in the transmit direction.

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4.2 CEPT Mode

The 29C96 allows 3 signalling modes : transparent, channel 16 CAS (Channel Associated signalling) and IRSM (Remote Switching Module) Selection of the signalling mode is done with MODE.smode0, 1/. In the transparent mode, no signalling is supported by the 29C96 and the transmitted data are sent unchanged on the line. On the receive side, signalling data will be ignored. Signaling source can be the external input/output ports XABCD and RABCD or the microprocessor addressable internal signalling RAMs. These RAMs include the 4 (CAS) or 5 (IRSM) signalling bits for each channel in the transmit and receive data flow. They are located in TSR1,32 registers or RSR1,32 registers.

Channel Associated Signaling

In this signalling mode, the 8 bits of channel 16 are used to carry the signalling data. When the source of signalling data is the external input port XABCD, 8 successive bits are latched and included in the transmitted data stream and the received data on channel 16 are output at port RABCD. When the source is the internal signalling RAM, the 8 bits of registers TSR1 to TSR32 are transmitted on the line, and the received channel 16 are stored in the registers RSR1 to RSR32 are transmitted on the line, and the received channel 16 are stored in the registers RSR1 to RSR32.

CAS signalling time slot 16 organization.

Ys : Signaling multiframe alarm, active high. XB1, 2, 3 : Extra bits. Signaling data.

bit number	1	2	3	4	5	6	7	8
FRAME 0	0	0	0	0	XB0	Ys	XB1	XB2
FRAME 1	A1	B1	C1	D1	A17	B17	C17	D17
FRAME 2	A2	B2	C2	D2	A18	B18	C18	D18
FRAME 3	A3	B3	C3	D3	A19	B19	C19	D19
FRAME 4	A4	B4	C4	D4	A20	B20	C20	D20
FRAME 5	A5	B5	C5	D5	A21	B21	C21	D21
FRAME 6	A6	B6	C6	D6	A22	B22	C22	D22
FRAME 7	A7	B7	C7	D7	A23	B23	C23	D23
FRAME 8	A8	B8	C8	D8	A24	B24	C24	D24
FRAME 9	A9	B9	C9	D9	A25	B25	C25	D25
FRAME 10	A10	B10	C10	D10	A26	B26	C26	D26
FRAME 11	A11	B11	C11	D11	A27	B27	C27	D27
FRAME 12	A12	B12	C12	D12	A28	B28	C28	D28
FRAME 13	A13	B13	C13	D13	A29	B29	C29	D29
FRAME 14	A14	B14	C14	D14	A30	B30	C30	D30
FRAME 15	A15	B15	C15	D15	A31	B31	C31	D31

Content of signalling registers is as follow :

BIT	1	2	3	4	5	6	7	8
	A	B	C	D	E	0	0	0

Content of signalling registers XSR1 to XSR32 and RSR1 to RSR32 with signalling data occupies the 8 bits of channel 16 in frames 0 to 15. The first byte, transmitted in frame 0, contains a multiframe alignment pattern, a multiframe alignment alarm Ys and a 3 bits extra data XB1,3. Frames 1 to 15 include two 4 bits signalling words A, B, C, D related to one of the data channels 1 to 15 and 17 to 31.

Remote Switching Module (IRSM) :

The IRSM signalling mode uses the same specification as CAS signalling mode for the content of time slot 16. But the IRSM mode uses the four national spare bits Sn1,4 to carry extra signalling bit (E) and Sn0 spare bit for a data link. This information is placed in time slot 0.

SIGNALLING MODE - The signalling mode is selected in MODE register by programming the bits MODE.smode0 and MODE.smode1.

	MODE.smode1	MODE.smode0
Transparent	0	0
CAS	0	1
IRSM	1	0
unused	1	1

ABCD - The source and destination of signalling data is selected by LSCR.SIGRC. When SIGSRS=0, the ABCD data is latched as input port XABCD for the transmit side and output at port RABCD for receive side. When SIGSRC=0, the ABCD data is loaded/stored from/in the signalling RAM (XSR1 to XSR32 for transmit and RSR1 to RSR32 for receive). Each of the transmit signalling registers (XSR1 to XSR32) and receive signaling registers (RSR1 to RSR32) are 8 bit registers, directly addressable by the host microprocessor.

CONTENT OF CHANNEL 0 OF FRAMES 0 to 15

IRSM signalling time slot 0 organization

Si : International bit. Fixed to '1' if unused.

Sn : National bits. Fixed to '1' if unused.

Ya : Yellow alarm. '0' : no alarm. '1' : alarm

CRC : CRC4 bits.

bit number	1	2	3	4	5	6	7	8
FRAME 0	CRC1	0	0	1	1	0	1	1
FRAME 1	0	1	Ya	D	E0	E1	E16	E17
FRAME 2	CRC2	0	0	1	1	0	1	1
FRAME 3	0	1	Ya	D	E2	E3	E18	E19
FRAME 4	CRC3	0	0	1	1	0	1	1
FRAME 5	1	1	Ya	D	E4	E5	E20	E21
FRAME 6	CRC4	0	0	1	1	0	1	1
FRAME 7	0	1	Ya	D	E6	E7	E22	E23
FRAME 8	CRC1	0	0	1	1	0	1	1
FRAME 9	1	1	Ya	D	E8	E9	E24	E25
FRAME 10	CRC2	0	0	1	1	0	1	1
FRAME 11	1	1	Ya	D	E10	E11	E26	E27
FRAME 12	CRC3	0	0	1	1	0	1	1
FRAME 13	Si	1	Ya	D	E12	E13	E28	E29
FRAME 14	CRC4	0	0	1	1	0	1	1
FRAME 15	Si	1	Ya	D	E14	E15	E30	E31

2

IRSM signalling time slot 16 organization.

Ys : Signaling multiframe alarm, active high.

XB1, 2, 3 : Extra bits.

ABCD : Signaling data.

bit number	1	2	3	4	5	6	7	8
FRAME 0	0	0	0	0	XB1	Ys	XB2	XB3
FRAME 1	A1	B1	C1	D1	A17	B17	C17	D17
FRAME 2	A2	B2	C2	D2	A18	B18	C18	D18
FRAME 3	A3	B3	C3	D3	A19	B19	C19	D19
FRAME 4	A4	B4	C4	D4	A20	B20	C20	D20
FRAME 5	A5	B5	C5	D5	A21	B21	C21	D21
FRAME 6	A6	B6	C6	D6	A22	B22	C22	D22
FRAME 7	A7	B7	C7	D7	A23	B23	C23	D23
FRAME 8	A8	B8	C8	D8	A24	B24	C24	D24
FRAME 9	A9	B9	C9	D9	A25	B25	C25	D25
FRAME 10	A10	B10	C10	D10	A26	B26	C26	D26
FRAME 11	A11	B11	C11	D11	A27	B27	C27	D27
FRAME 12	A12	B12	C12	D12	A28	B28	C28	D28
FRAME 13	A13	B13	C13	D13	A29	B29	C29	D29
FRAME 14	A14	B14	C14	D14	A30	B30	C30	D30
FRAME 15	A15	B15	C15	D15	A31	B31	C31	D31

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After transmission or reception of a complete signalling RAM, MSR.XRACK and MSR.SRF are set to '1'. If the bit MASK.SRE or MASK.SRF of the interrupt mask register is also set to 1, an interrupt is enabled and INT output is activated.

Multiframe Pattern

In CAS signalling mode, the channel 16 of frame 0 includes the MULTIFRAME pattern (bit 1 to 4 as indicated in IRSM signalling time slot 16 organization). When this mode is selected, multiframe pattern is internally generated.

Loss Of Signaling Multiframe

When the CAS multiframe pattern is detected with error in two consecutive multiframe, or the content of channel 16 of all frames in a multiframe is '0', the 29C96 will indicate a loss of signalling multiframe alignment and the bit ALARM.LSMA will be set to '1'.

Multiframe Alarm

This multiframe alarm YS is activated by setting the bit TCR.Ys=1. In such case, the bit Ys (bit 6 of time slot 16 of frame 0) is set to '1' in the transmitted data. When the alarm is detected in the received data, the bit ALARM.Ys of ALARM register is set to '1'. If the bit MASK.Ys of the interrupt mask register is also set to 1 then an interrupt is enabled and INT output is activated.

Extra Bits

The bits 5, 6 and 8 of timeslot 16 of frame 0 carry the 3 extra bits. When LSCR.XBS=0, these bits are sourced from register EBR.XER0, 1 and 2 at transmission and stored in positions EBR.RER0, 1 and 2 at reception. When LSCR.XBS is set to '1', the extra bits are latched at input port XDL for transmission or output at port RDL for reception.

Signaling Idle

Signaling channels can be replaced in transmission by an all '1' pattern by programming LSCR.TSAI = 1.

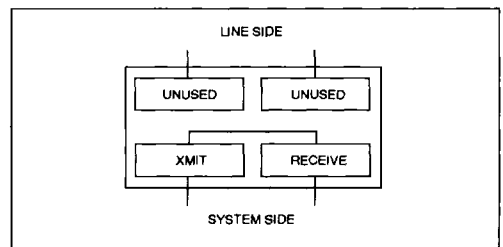
Data Link-

When the bit MODE.Sn=1, the D bit is latched at input port XDL at transmission and output at port RDL at reception. When this bit is '0', the D is taken in TSBR register at position Sn0 to Sn3 for transmission and stored in register RSBR at position Sn0 to Sn3.

5 Loop Back

LOCAL LOOP BACK is programmed by setting to '1' the bit LLB in LSCR register.

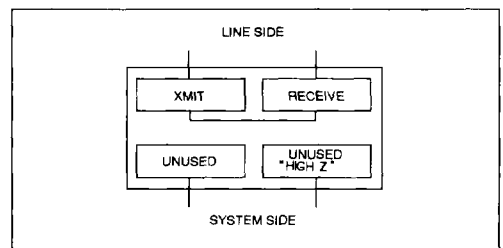
This loop back mode internally routes the output data and clock signals on the carrier side (data assembled by the 29C96 transmitter) to the data and clock input signals (synchronizer and receiver inputs). The data from the carrier PORTS are ignored and the transmit data on carrier PORTS are set IDLE or AIS. IDLE code is a 8 bits programmable code, AIS is an 'all 1' pattern.



REMOTE LOOP BACK is programmed by setting to '1' the bit RLB in LSCR register.

This loop back mode internally routes the data and clock input signals on the carrier side (data extracted from the synchronizer and receiver) to the data and clock output signals (data assembled by the transmitter).

The data from the system PORTS are ignored and the transmitted data on system PORTS are set IDLE or transparently output. IDLE code is an 8 bits programmable code.



CHANNEL LOOP BACK is selected by setting to '1' the bit CLB in LSCR register.

T1/DS1 Mode

In the channel loop back mode, a specified channel (among 24) is looped from the 29C96 transmitter to the receiver inputs.

The content of the designated channel remains unchanged or can be set to IDLE in the same manner as local loop back mode. The loop back of a channel from a signalling frame can be disabled.

CEPT Mode

This loop back mode is selected by setting to '1' the bit LSCR.CL (bit Channel Loop Back in Loopback and Signaling Control Register). When this mode is selected, the associated register CHANNEL LOOPBACK REGISTER, designates the address of one of the 32 channels which is looped back (CLR.ADD0 to CLR.ADD4). Disabling of loop back containing signalling information is done by programming bit CLR.SIG to '1'.

6 IDLE Mode

When the bit LSCR.IDLE is set to 1, the content of all channels in the transmit direction is replaced by the content of register IDLE.

IDLE Channels

When LSCR.IC is set to '1', the content of the designated channels in the transmit direction is replaced by the content of register IDLE. Channels to set idle are programmed in the IDLE CHANNELS REGISTERS 0 to 3.

7 Receive Mask

When FCR.CHM is set to '1', the content of the designated channels in the receive direction is replaced by the content of register RMR (Receive Mask Register). Channels to disable and mask are programmed in the MASK CHANNELS REGISTERS 0 to 3.

8 AIS

TCR.AIS=1 will force to replace the content of all transmit channels by a 'framed all '1' pattern'. When an all '1' pattern (2 or less zero in a multiframe) is detected in the received stream, the bit ALARM.AIS of the ALARM register is set to '1'. If the bit MASK.AIS of the interrupt mask register is also set to '1', an interrupt is enabled and INT output is activated.

9 AMI Coding/Programming

AMI - Inputs and outputs of framer are AMI coded, (Alternate Mark Inversion). The '1's are coded

alternatively as pulses of positive and negative polarity. '0' are coded as no pulse. If a protocol providing a '0' density instead of a '1' density is used, data flow can be inverted before AMI coding.

When LCR.AMI=0, data in the transmit or receive flow is directly transcoded from non-return-to-zero to AMI (DIRECT AMI). When this bit is set to '1', the NRZ data is inverted before AMI coding or after AMI decoding (INVERT AMI).

AMI Errors

AMI errors are counted in registers AEC0 and AEC1 (AMI Error Counter 0 and 1). AEC0 is the lowest byte of the 16 bits AMI error counter and AEC1 is the upper byte. Upon detection of AMI error in the received data, ERROR.AMIE is set to '1'. When the AMI error counter reaches the maximum error count, ERROR.ACO is set to '1'. If MASK.ACO is also set to 1 then an interrupt is enabled and INT output is activated. When the synchronizer detects an AMI error, AMIE output will go high for one RCLOCK period, indicating the error to the external environment.

T/DS1 Mode

ZCS - Zero code stuffing. This zero code replacement mechanism works on a channel basis. When an all '0' channel is detected, one bit (bit 7) is replaced with a '1'. It can be disabled on a channel basis to form a CLEAR CHANNEL.

This zero suppression method can be programmed by setting LCR.ZCS to '1'.

B8ZS - The B8ZS coding is used to avoid a great '0' density. Each block of $8 \times "0"$ is replaced by a violation pattern '000vb0vb' where b is the insertion of a '1' with no violation of alternating law and v is the insertion of a '1' with violation of alternating law. In the receive side, any violation pattern found in data flow is replaced by the code '00000000'. Violations can be reported in a violation counter that stores the number of violations or non-B8ZS violations depending on selected mode. An interrupt or status bit can be set when the counter overflows. The counter can be preset in order to monitor the line. This zero suppression method can be programmed by setting LCR.B8ZS to '1' the bit LCR.B8ZS. On the receive side, the detection of B8ZS type violations is reported by ERROR.B8ZS.

CEPT Mode

HDB3 - The HDB3 coding is used to avoid a great '0' density. The conversion is made in transmit side before AMI coding on the data flow independently of the channel boundaries. In order to avoid long sequences of "0", AMI code is modified, when the

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number of "1" in the data stream is even this pattern is b00v, when the number of "1" in the data stream is odd this pattern is "000V", b is the insertion of a '1' with no violation of alternating law and v is the insertion of a '1' with violation of alternating law. In the receive side, any non-alternate mark and the 3 preceding data corresponding to an HDB3 code are replaced by the code '0000'. Violations can be reported in a violation counter that store the number of violations or non-HDB3 violations depending on the mode selected. An interrupt or status bit is set when the counter overflows. The counter can be preset in order to monitor the line.

10 Synchronization

T1/DS1 Mode

Frame Alignment

4-FRAME - Frame alignment is assumed to be lost when 2 Ft bits out of 4 have been received with error status. In that case ALARM.LFA is set to '1'. Frame alignment is assumed to be recovered when only 1 Ft framing pattern is found. In case of multiple framing

possibilities, alignment on the first available start of multiframe can be forced by programming LCR.FORCE to '1'. Resync of the receiver can be automatically initiated upon loss of alignment when autoresync mode is enabled (LCR.ALFA=1), or forced by programming LCR.REFRAME to "1".

D4 - Frame alignment is assumed to be lost when 2 Ft bits out of 4 have been received with error status. In that case ALARM.LFA is set to '1'. Multiframe alignment is assumed to be lost when 2 Fs bits out of 4 have been received with error status and LARM.DSYNC is set to '1'. The loss of frame alignment or multiframe alignment leads to asynchronous state. Frame alignment is assumed to be recovered when only 1 Ft framing pattern is found. Multiframe alignment is searched when frame alignment is met, it is assumed when 2 consecutive multiframe patterns (Fs bits) are found correct. In case of multiple framing possibilities, alignment on the first available start of frame can be forced by programming LCR.FORCE to '1'. Resync of receiver can be automatically initiated upon loss of alignment when auto-mode is enabled (LCR.ALFA=1 or LCR.ALMA=1), or forced by programming LCR.REFRAME to '1'.

	Ft	Fs	
FRAME 1	1		A signalling channel
FRAME 2		0	
FRAME 3	0		
FRAME 4		0	
FRAME 5	1		
FRAME 6		1	
FRAME 7	0		
FRAME 8		1	
FRAME 9	1		
FRAME 10		1	
FRAME 11	0		
FRAME 12		Ya	B signalling channel

ESF - Frame alignment is assumed to be lost when 2 FAS bits out of 4 have been received with error status. In that case ALARM.LFA is set to '1'. Multiframe alignment based on CRC6 checking is not mandatory, it can be used if several framing candidates are detected. In that case, alignment is assumed when FAS pattern and CRC code match together. Errors in CRC does not lead to a loss of frame or multiframe alignment.

Frame alignment is assumed to be recovered when only 1 FAS framing pattern is found. In case of multiple framing possibilities, CRC6 checking is used to perform multiframe alignment. When more than one candidate subsists after a 100 ms checking period, alignment can be done on the first available candidate by programming LCR.FORCE to '1'.

	FAS	FDL	CRC	
FRAME 1		m		A signalling frame
FRAME 2			CRC1	
FRAME 3		m		
FRAME 4	0			
FRAME 5		m		
FRAME 6			CRC2	
FRAME 7		m		B signalling frame
FRAME 8	0			
FRAME 9		m		
FRAME 10			CRC3	
FRAME 11		m		
FRAME 12	1			
FRAME 13		m		C signalling frame
FRAME 14			CRC4	
FRAME 15		m		
FRAME 16	0			
FRAME 17		m		
FRAME 18			CRC5	
FRAME 19		m		D signalling frame
FRAME 20	1			
FRAME 21		m		
FRAME 22			CRC6	
FRAME 23		m		
FRAME 24	1			

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SLC 72-FRAME - Same as D4 Alignment.

	FAS	FDL	
FRAME 1/13	1		A/C signalling frame
FRAME 2/14		0	
FRAME 3/15	0		
FRAME 4/16		0	
FRAME 5/17	1		
FRAME 6/18		1	
FRAME 7/19	0		
FRAME 8/20		1	
FRAME 9/21	1		
FRAME 10/22		1	
FRAME 11/23	0		
FRAME 12		0	
FRAME 24		D	D signalling frame
FRAME 25/37/49/61	1		A/C signalling frame
FRAME 26/38/50/62		D	
FRAME 27/39/51/63	0		
FRAME 28/40/52/64		D	
FRAME 29/41/53/65	1		
FRAME 30/42/54/66		D	
FRAME 31/43/55/67	0		
FRAME 32/44/56/68		D	
FRAME 33/45/57/69	1		
FRAME 34/46/58/70		D	
FRAME 35/47/59/71	0		
FRAME 36/48/60		D	
FRAME 72		0	D signalling frame

Resynchronisation of the receiver can be automatically initiated upon loss of alignment when autoresynchronisation mode is enabled (LCR.ALFA=1), or forced by programming LCR.REFRAME to '1'.

DDS - DDS multiframing format uses the same framing method as D4 format. In addition the content of channel 24 is used to perform the multiframing alignment. Criteria of Loss of Frame Alignment and Loss of Multiframing Alignment are those described in

D4 chapter. Multiframing alignment will also be lost when $4 \times$ DDS alignment patterns are detected with error status in 12 consecutive frames. In that case ALARM.DSYNC is set to '1' and the receiver will switch to asynchronous state. When frame alignment is found, based on Ft pattern, the synchronizer will search for Fs multiframing pattern and start checking the content of channel 24 for a correct DDS pattern. Alignment will be considered correct after 6 consecutive frames without error.

Frame/Multiframe Alignment Programming

REFRAME - When LCR.REFRAME toggles from '0' to '1' the 29C96 synchronizer is reseted, then it starts searching a valid framing candidate corresponding to the various criterias described earlier. During the reframe period, the CRC, AMI, Frame bit error counters are stoped. Upon a new frame or multiframe alignment, the internal CRC, AMI, Frame bit error counters are cleared.

FORCE REFRAME - During the resynchronization period, the framer tests every bit position, that is the number of bits between two consecutive framing bits (386 in 4-FRAME/D4/SLC, 772 in ESF). The synchronization algorithm eliminate all but one candidate before establishing a multiframe alignment. The framer first tests the frame alignment (Ft bits and then looks for a multiframe alignment pattern (Fs bits). If no multiframe synchronization is found after 4 multiframe periods the candidate is eliminated and the next available candidate will be tested for multiframe alignment until all framing criterias are met. If all candidates are eliminated during the reframe period, the resynchronizer is reseted and starts a new reframe period. If more than one candidate is found during the synchronization periods, ALARM.FTEMPO will be set to 1. If MASK.FTEMPO=1, an interrupt is enabled and INT output is activated. If LCR.FORCE is set to 1 at this time or as soon as this bit will be set to 1, the synchronizer will force multiframe alignment on the first available candidate.

START OF MULTIFRAME - Synchronization with the 29C96 framer is made easy with signals marking start of transmit and receive multiframe. The output signal XMFSYNC is multiframe clock whose rising edge is synchronous with first bit of a multiframe and falling edge is synchronous with the first bit of the second frame.

LOSS OF FRAME ALIGNMENT - Error in F bits framing pattern leads to a loss of frame alignment

(Ft error in 4-FRAME/D4/ESF/SLC). This is indicated in ALARM register by setting ALARM.LFA to 1. If MASK.LFA is also set to 1, an interrupt is enabled and INT output is activated.

AUTOMATIC REFRAME ON LFA - If LCR.ALFA is programmed to '1', the 29C96 framer will automatically reframe upon detection of a loss of frame alignment. This event will be indicated by setting SSR.VERR to '1'.

AUTOMATIC YA TRANSMIT - If TCR.AYa is programmed to '1', the 29C96 framer will automatically send Ya signal after a loss of frame or

multiframe alignment. The alarm depends on MODE.YaM.

LOSS OF MULTIFRAME ALIGNMENT - Error in F bits multiframe pattern leads to a loss of frame alignment (Fs error in D4/SLC). This is indicated in ALARM register by setting ALARM.DSYNC to 1. If MASK.DSYNC is also set to 1, an interrupt is enabled and INT output is activated. This event will be indicated by setting SSR.CMFA to 1.

AUTOMATIC REFRAME ON DSYNC - If LCR.ALMA is programmed to '1', the 29C96 framer will automatically reframe upon detection of a loss of multiframe alignment.

2

CEPT Mode

Frame Alignment

Frame alignment is assumed to be lost when 3 consecutive FAS words have been received with error status, or when 3 consecutive service bits (non FAS word) have been receive with error status. In that case ALARM.LFA is set to '1'. Frame alignment is assumed to be recovered when :

- a correct FAS word is detected in a frame.
- a correct service bit (non FAS word) is detected in the second frame.
- a correct FAS word is detected in a third frame.

Resynchronisation of the receiver can be automatically initiated upon loss of alignment when autoresynchronisation mode is enabled (LCR.ALFA=1), or forced by programming LCR.REFRAME to 1.

Multiframe Alignment

CRC MULTIFRAME - The CRC alignment is performed after the FRAME alignment is declared, it is achieved by matching CRC code in every even frame of a multiframe, and multiframe alignment signal in the odd frames. The CRC multiframe alignment is delcared if 2 CRC4 and multiframe alignment signals are found valid in the 4 multiframes following the frame alignment. Multiframe alignment is lost when more than 915 CRC4 errors are detected within 1 second or when the 6 bit multiframe alignment pattern has been received with error status during two consecutive multiframes. The loss of frame alignment or multiframe alignment lead to asynchronous state and ALARM.DSYNC is set to '1'. Resynchronisation of the receiver can be automatically initiated upon loss of alignment depending autoresync mode is enabled (LCR.ALMA=1), or forced by programming LCR.REFRAME to 1.

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CAS MULTIFRAME - CAS alignment is declared when the 4 lowest bits of channel 16 in frame 0 are set to '0' and at least a '1' state is present at any bit position of any other frames (channel 16 of frames 1 to 15). CAS alignment is declared lost, when all bits in a channel 16 in any frame is '0' (eight '0' (eight '0' bit in a channel 16) or CAS multiframe pattern error is detected during two consecutive multiframes.

Frame/Multiframe Alignment Programming

REFRAME - When LCR.REFRAME toggles from '0' to '1' the 29C96 synchronizer is reseted and start searching for a valid framing candidate corresponding to the various criterias described earlier. During the reframe period, the CRC, AMI, Frame bit error counters are stopped. Upon a new frame or multiframe alignment, the internal CRC, AMI, Frame bit error counters are cleared.

START OF MULTIFRAME - Synchronization with the 29C96 framer is made easy with the XMFSYNC. This signal is multiframe clock whose rising edge is synchronous with first bit of a multiframe and falling edge is synchronous with the first bit of the second frame. RMFSYNC is synchronous with first bit of multiframe computed inside 29C96 by the synchronisation function.

LOSS OF FRAME ALIGNMENT - Errors in FAS words framing pattern lead to a loss of frame alignment. This is indicated by setting ALARM.LFA to 1. If MASK.LFA is also set to 1, an interrupt is enabled and the INT output is activated.

AUTOMATIC REFRAME ON LFA - If LCR.ALFA is programmed to '1', the 29C96 framer will

automatically reframe upon detection of a loss of frame alignment. The 29C96 will start searching a valid frame alignment at the position following the preceding start bit. When a new alignment is met, this will be indicated by setting SSR.VERR to 1.

AUTOMATIC Ya TRANSMIT - If TCR.AYa is programmed to '1', the 29C96 framer will automatically send Ya signal after a loss of frame alignment.

LOSS OF MULTIFRAME ALIGNMENT - Error in CRC4 multiframing pattern leads to a loss of frame alignment (LMA). This is indicated by setting ALARM.DSYNC to 1. MASK.DSYNC is also set to 1, an interrupt is enabled.

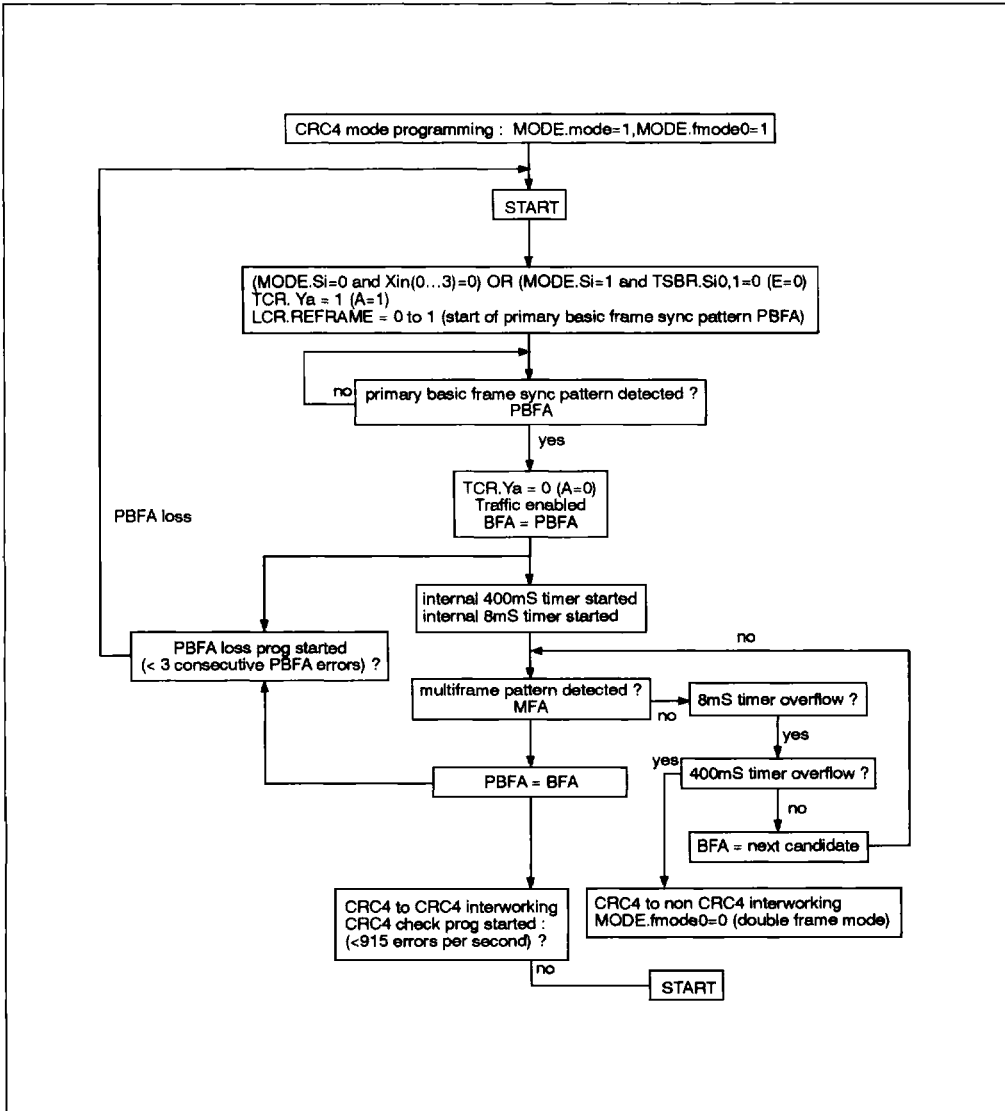
AUTOMATIC REFRAME ON DSYNC - If LCR.ALMA is programmed to '1', the 29C96 will start searching a valid multiframe alignment at the position following the preceding start bit. When a new alignment is met, this will be indicated by setting SSR.BFA to '1'.

LOSS OF CAS MULTIFRAME ALIGNMENT - Error in the CAS multiframing pattern leads to a Loss of Signaling Multiframe Alignment (LSMA). This is indicated by setting ALARM.LSMA to 1. If MASK.LSMA is also set to 1, an interrupt is enabled and INT output is activated.

AUTOMATIC YS TRANSMIT - If TCR.AYs is programmed to '1', the 29C96 framer will automatically send Ys signal after a loss of multiframe alignment (LMA) or a loss of CAS signalling multiframe alignment (LSMA). This is valid only in CAS signalling mode.

INTERWORKING BETWEEN CRC4 AND NON CRC4 EQUIPMENTS IN CEPT MODE (appendix B of G706) (Timers, time out handling and error counters are internal and not accessible for user)

2



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11 Interrupts

12 Slip Memory

FUNCTIONAL DESCRIPTION - The FRAMERS data clock is generally jittered compared to system clock. In order to eliminate this jitter the FRAMER uses a slip memory. This memory is a FIFO, read on the receive side by the carrier data clock, and written on the system side at the system clock rate. This memory forms a circular FIFO with a two frames capacity. The FIFO is written starting at position zero. When the memory is half full (write at position 193/256) reading can start at position zero. The read and write pointers are incremented at their own frequency. When the read pointer exceeds the write pointer an underflow condition is detected, MSR.XSMU is set to 1. When the write pointer exceeds the read pointer an overflow condition is detected, MSR.XSMO is set to 1. If the corresponding interrupt enable bits are activated and INT output is activated.

SLIP MEMORY PROGRAMMING :

- TRANSMIT SLIP MEMORY : 1 FIFO memory with a 48x8/64x8 bits capacity.
- RECEIVE SLIP MEMORY : 1 FIFO memory with a 48x8/64x8 bits capacity.
- TRANSMIT SLIP MEMORY UNDERFLOW : Error is reported in bit MSR.XSMU.
- TRANSMIT SLIP MEMORY OVERFLOW : Error is reported in bit MSR.XSMO.
- ON MSR.XSMO or MSR.XSMU SLIP MEMORY are resetted automatically.

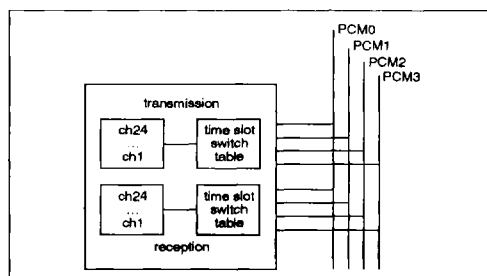
13 PCM Interface

FUNCTIONAL DESCRIPTION - The 29C96 can interface from 1 to 4 PCM buses or 1 to 128 time slots. This selection is made by PMR.NCHA and PMR.BTYP0,1. The control of data on the 4 PCM buses ROUT0, 1, 2, 3 is made by PMR.PCME, PCME=1 enables data output on the bus, PCME=0 forces all bus to TRI-STATE.

PMR.NCHA allows to select the configuration of PCM buses to be a multiple of 24 channels (PMR.NCHA=0) or a multiple of 32 channels (PMR.NCHA=1).

These two bits select the number of buses. The total number of time slots is always 128, but the maximum number of time slots per bus (or the DATA rate on this bus) depends on the number of addressable buses.

It may change from 32 (24) to 128 (96) time slots on a bus. After selection of bus number (or time slots) interfacing the 29C96, TSSR1 to 24/32 registers (TIME SLOT SWITCHING TABLE) allow user to define a unique correspondance between any individual T1/CEPT LINE channels and the 128/96 possible PCM channels.



PMR.BTYP0, 1 select the number of PCM buses that the 29C96 will interface with, according to the following table.

	PMR.BTYP1	PMR.BTYP0
0 PCM NO SYSTEM BUS	0	0
1 PCM bus : PCM0 at 8 192 (6 176) kHz/128 (96) time slots	0	1
2 PCM bus : PCM0, 1 at 4 096 (3 088) kHz/64 (48) time slots	1	0
4 PCM bus : PCM0, 1, 2, 3 at 2 048 (1 544) kHz/32 (24) time slots	1	1

The correspondance between T1/CEPT channel and PCM channel is shown in the following tables :

BTYP0	BTYP1
1	0

REGISTER TSSR_i

TSN0	TSN1	TSN2	TSN3	TSN4	TSN5	TSN6	SM
------	------	------	------	------	------	------	----

Index i ranges from 1 to 24/32 and corresponds to the actual transmitted or received T1 channel.

TSN0,6 These 7 bits select the time slot of PCM0 that is affected to the T1/CEPT channel number i in the transmit as well as in the receive side.

SM When this bit is '0', the corresponding time slot of ROUT0 is TRI-STATE, the T1/CEPT channel number i does not carry any data.

2

BTYP0	BTYP1
0	1

REGISTER TSSR_i

TSN0	TSN1	TSN2	TSN3	TSN4	TSN5	TSN6	SM
------	------	------	------	------	------	------	----

Index i ranges from 1 to 24/32 and corresponds to actual transmitted or received T1/CEPT channel.

PBN0 Selects the bus [PCM0 (PNB0=0) or PCM1 (PNB0=1)] that will correspond to the T1 channel number i.

TSN0,5 These 6 bits select the time slot of the selected PCM that is affected to the T1/CEPT channel number i in the transmit as well as in the receive side.

SM When this bit is '0', the corresponding time slot of PCM is TRI-STATE, the T1/CEPT channel number i does not carry any data.

BTYP0	BTYP1
1	1

REGISTER TSSR_i

TSN0	TSN1	TSN2	TSN3	TSN4	PBN0	PBN1	SM
------	------	------	------	------	------	------	----

Index i ranges from 1 to 24/32 and corresponds to the actual transmitted or received T1/CEPT channel.

PBN0,1 Select the bus that will correspond to the T1/CEPT channel number i :

- PCM0 (PNB0=0, PNB1=0)
- PCM1 (PNB0=1, PNB1=0)
- PCM2 (PNB0=0, PNB1=1)
- PCM3 (PNB0=1, PNB1=1)

TSN0,4 These 5 bits select the time slot of the selected PCM that is affected to the T1/CEPT channel number i in the transmit as well as in the receive side.

SM When this bit is '0', the corresponding time slot of PCM is TRI-STATE, the T1/CEPT channel number i does not carry any data.

29C96

Ordering Information

\emptyset — 	S — 	29C96 —
TEMPERATURE RANGE \emptyset COMMERCIAL 0 TO 70 °C I INDUSTRIAL -40 TO 85 °C	PACKAGE : S = PLCC	Part number 29C96

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