OVERVIEW

The SED1278 is a dedicated character display controller/driver which, when used with the SED1181F or the SED1681 segment drivres, is able to display up to 80 characters under 4- or 8-bit MPU control.

The internal character generator (CG) ROM has an extended 240, 5×10 pixel, character set, plus CGRAM space for an additional eight user definable 5×8 pixel characters. These memory features combined with the rich set of control instructions offer the potential for a highly flexible character display system.

The SED1278 features a guaranteed minimum LCD drive voltage of 3 V making it suitable for use with low voltage LCD panels.

FEATURES

- Interface for 4- and 8-bit MPUs
- Display RAM – 80 bytes (80 characters)
- Character generator ROM – 240 characters
  - 5×8 pixel font
- Character genrator RAM – 64 bytes
  - 5×8 pixel font, 8 characters.
  - 5×10 pixel font, 4 characters.
- Number of characters used

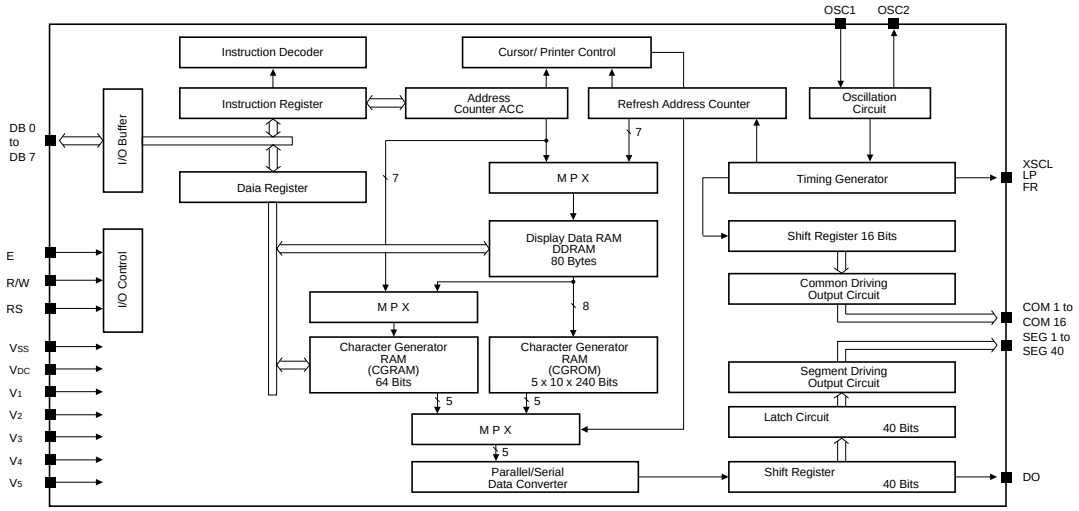
	Duty	SED1278F	SED1181F$_{LA}$	No. of characters used
One-line display	1/8, 1/11	1	0	8 columns × 1 line
			6	80 columns × 1 line
Two-line display	1/16	1	0	8 columns × 2 lines
			3	40 columns × 2 lines

- Powerful display control instructions
- LCD driver outputs
  - 40 segment driver outputs
  - 16 common driver outputs
- Low LCD drive voltage – 3 V minimum (V_{DD}–V_5)
- Dual-frame AC drive
- On-chip power-on reset
- On-chip RC oscillator
- Single 5 V operation
- Chip (SED1278D) and 80-pin QFP (SED1278F) packages

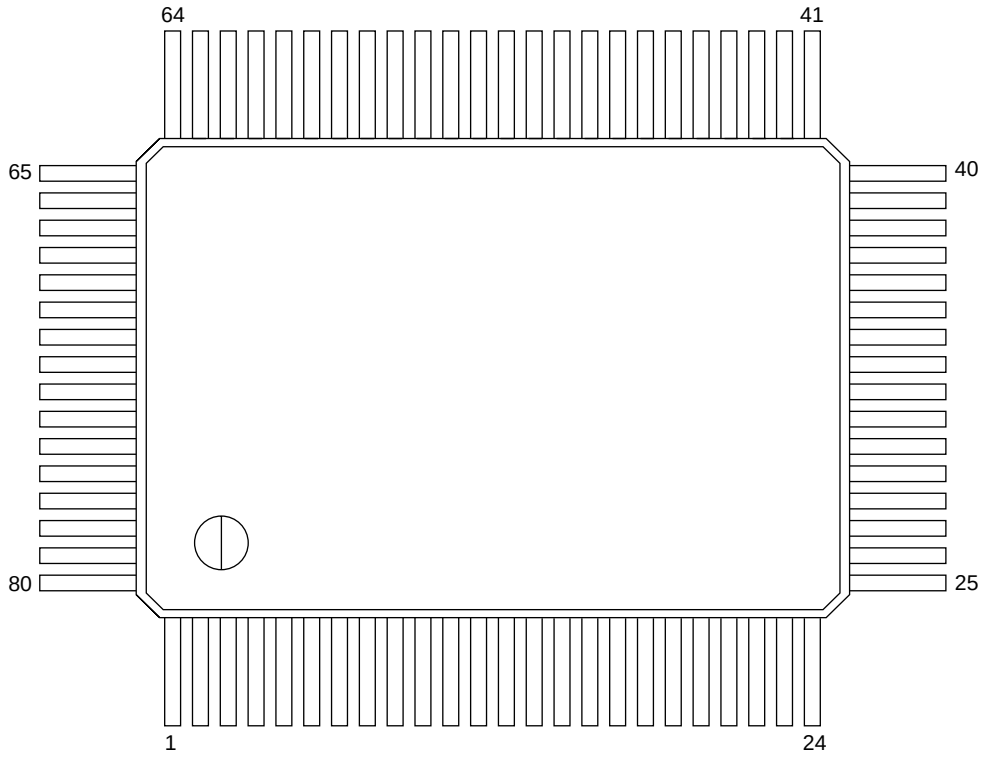
(Compatible with HD 44780 and HD 66780 by Hitachi Limited)

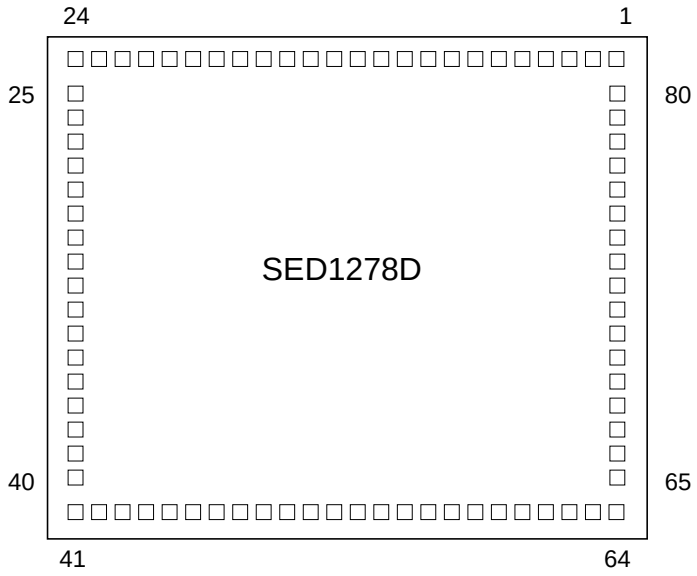
The SED1278 is equivalent to the HD 44780 and HD 66780 by Hitachi Limited. Before use, make sure that there is no problem for practical use. It should be noted that this is not intended to guarantee enforcement of industrial property and other rights, or to grant license for the use of this product.

BLOCK DIAGRAM



PACKAGE OUTLINE





PINOUT

Pin		Pin		Pin		Pin	
Number	**Name**	**Number**	**Name**	**Number**	**Name**	**Number**	**Name**
1	SEG22	21	SEG2	41	DB2	61	COM15
2	SEG21	22	SEG1	42	DB3	62	COM16
3	SEG20	23	GND	43	DB4	63	SEG40
4	SEG19	24	OSC1	44	DB5	64	SEG39
5	SEG18	25	OSC2	45	DB6	65	SEG38
6	SEG17	26	V_1	46	DB7	66	SEG37
7	SEG16	27	V_2	47	COM1	67	SEG36
8	SEG15	28	V_3	48	COM2	68	SEG35
9	SEG14	29	V_4	49	COM3	69	SEG34
10	SEG13	30	V_5	50	COM4	70	SEG33
11	SEG12	31	LP	51	COM5	71	SEG32
12	SEG11	32	XSCL	52	COM6	72	SEG31
13	SEG10	33	V_{DD}	53	COM7	73	SEG30
14	SEG9	34	FR	54	COM8	74	SEG29
15	SEG8	35	DO	55	COM9	75	SEG28
16	SEG7	36	RS	56	COM10	76	SEG27
17	SEG6	37	R/W	57	COM11	77	SEG26
18	SEG5	38	E	58	COM12	78	SEG25
19	SEG4	39	DB0	59	COM13	79	SEG24
20	SEG3	40	DB1	60	COM14	80	SEG23

PIN DESCRIPTION

MPU Interface

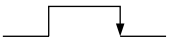
RS Register select signal input. Selects between the data and instruction registers during CPU access.
RS = 0: Instruction register access cycle
RS = 1: Data register access cycle

R/W This input selects between SED1278 register read and write cycles.
R/W = 0: Register write cycle
R/W = 1: Register read cycle

E Read/write execute signal input.

DB0 to DB7 TTL level data input/output lines, for connection to the system MPU data bus.

TABLE 1 The Function of the E Signal

RS	R/W	E	Operation
0	0		Instruction write cycle
0	1	1	Busy flag read cycle Address counter read cycle
1	0		DDRAM or CGRAM data write cycle
1	1	1	DDRAM or CGRAM data read cycle

LCD Panel Interface

COM1 to COM16 Common driver outputs to the LCD panel.

SEG1 to SEG40 Segment driver outputs to the LCD panel.

OSC1 If the internal RC oscillator is used to generate the LCD drive signals, the feedback resistor, R_f, is connected to this pin. If an external clock source is used, the clock is connected to this pin.

OSC2 If the internal RC oscillator is used to generate the LCD drive signals, the feedback resistor, R_f, is connected to this pin. If an external clock source is used, this pin is left open.

External Segment Driver Interface

LP Data latch pulse output for an external X-driver.

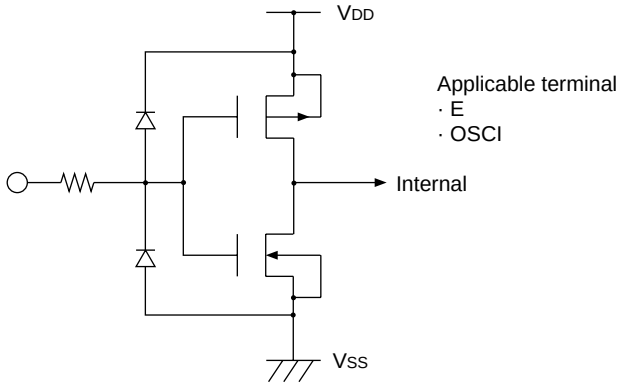
XSCL Data shift clock output for an external X-driver.

FR LCD AC-drive waveform for an external X-driver.

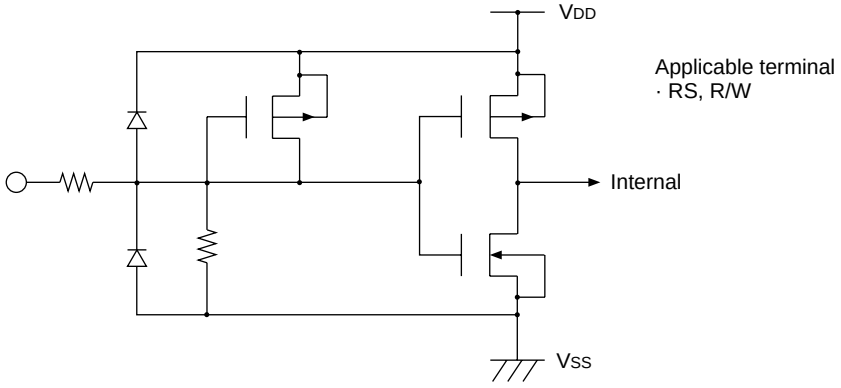
DO Display data output for an external X-driver.

TERMINAL CONFIGURATION

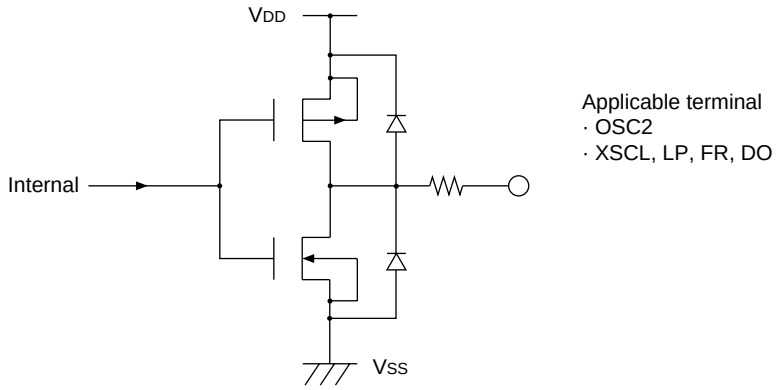
1. Input terminal configuration (1)



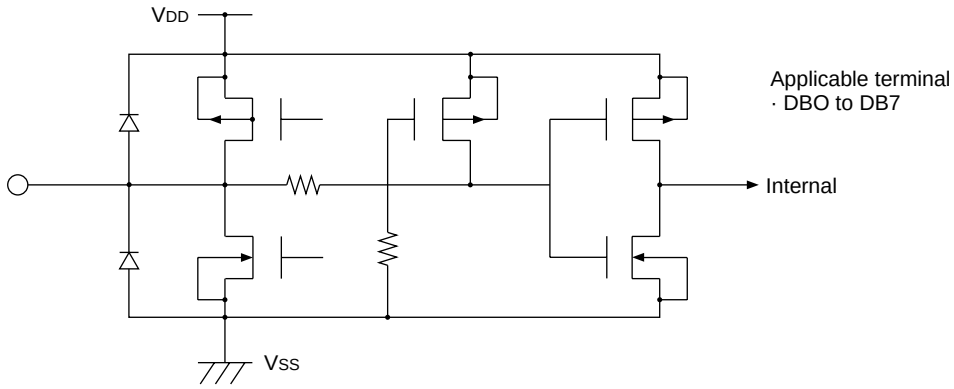
2. Input terminal configuration (2)
   With pull-up MOS resistor



3. Output terminal configuration



4. Input/Output terminal configuration



INSTRUCTION DESCRIPTION

Instruction Summary

Instruction	Code										Description	Cycle Time (max.)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display data and sets DDRAM address 0 in the address counter.	410 clocks
Return Home	0	0	0	0	0	0	0	0	1	*	Set DDRAM address 0 in the address counter. Also returns any shifted data to home. The contents of DDRAM remain unchanged.	410 clocks
Entry Mode Set	0	0	0	0	0	0	0	1	I/$\overline{D}$	S	Specifies the direction in which the cursor moves and whether the display is to be shifted or not, when data is writen to or read from memory	10 clocks
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Sets all display on/off (D) cursor on/off (C), and character blinking in the cursor position (B).	10 clocks
Cursor or Display Shift	0	0	0	0	0	1	S/$\overline{C}$	R/$\overline{L}$	*	*	Moves the cursor and shifts the display without changing the contents of DDRAM.	10 clocks
System Set	0	0	0	0	1	IF	N	F	*	*	Sets the interface data length (IF), number of characters to be displayed (N), and character font (F).	10 clocks
Set CGRAM Address	0	0	0	1	ACG						Set CGRAM addresses, followed by transfer of CGRAM data.	10 clocks
Set DDRAM Address	0	0	1	ADD							Sets DDRAM address, followed by transfer of DDRAM data.	10 clocks
Read Busy Flag and Address	0	1	BF	ACC							Reads the busy flag (BF) which indicates internal operation and the contents of the address counter.	0
Write Data to CG or DDRAM	1	0	Write Data								Writes data to DDRAM or CGRAM.	10 clocks
Read Data from CG or DDRAM	1	1	Read Data								Reads data from DDRAM or CGRAM.	10 clocks

* Don't care

Write Only Instructions

Clear Display

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	01H

RS = 0

This instruction
1. loads all locations in the display data (DD) RAM with 20H.
2. clears the contents of the address counter to 0H.
3. sets the display for zero character shift.
4. sets the address counter to point to the DDRAM.
5. , if the cursor is displayed, moves the cursor to the left most character in the display or, if a two line display is used, moves the cursor to the leftmost character in the top line (line 1).
6. sets the address counter to increment on each access of DDRAM or CGRAM.

Cursor Home

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	1	*	02H, 03H

RS = 0

This instruction
1. clears the contents of the address counter to 0H.
2. sets the address counter to point to the DDRAM.
3. sets the display for zero character shift.
4. , if the cursor is displayed, moves the cursor to the left most character in the display or, if a two line display is used, the left most character in the top line (line 1).

Entry Mode Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	I/$\overline{D}$	S	04H to 07H

RS = 0

- The I/$\overline{D}$ bit selects the way in which the contents of the address counter are modified after every access to DDRAM or CGRAM.
  - I/$\overline{D}$ = 1: The address counter is incremented.
  - I/$\overline{D}$ = 0: The address counter is decremented.
- The S bit enables display shift, instead of cursor shift, after each write or read to the DDRAM.
  - S = 1: Display shift enabled.
  - S = 0: Cursor shift enabled.

  The direction in which the display is shifted is opposite in sense to that of the cursor. For example if S = 0 and I/$\overline{D}$ = 1 the cursor would shift one character to the right after an MPU write to DDRAM. However if S = 1 and I/$\overline{D}$ = 1, the display would shift one character to the left and the cursor would maintain its position on the panel.

  The cursor will already be shifted in the direction selected by I/$\overline{D}$ during reads of the DDRAM, irrespective of the value of S. Similarly reading and writing the CGRAM always shifts the cursor. Note that if a two line display is used both lines will be shifted simultaneously.

Display ON/OFF

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	D	C	B	08H to 0FH

RS = 0

This instruction controls various features of the display.
- The D bit turns the entire display on or off.
  - D = 1: Display on
  - D = 0: Display off
- The C bit turns the cursor on or off.
  - C = 1: Cursor on
  - C = 0: Cursor off
- The B bit enables blinking of the character the cursor coincides with.
  - B = 1: Blinking on
  - B = 0: Blinking off

  Blinking is achieved by alternating between a normal and all dark display of a character. The blinking period is set at 204800 fOSC. For example if fOSC = 250 kHz the cursor will blink with a period of 0.8192 seconds, or about 1.2 Hz.

Cursor/Display Shift

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	S/$\overline{C}$	R/$\overline{L}$	*	*	10H to 1FH

RS = 0

This instruction shifts the display and/or moves the cursor, on character to the left or right, regardless of a DDRAM ready/write.
- The S/$\overline{C}$ bit selects movement of the cursor or movement of both the cursor and the display.
  - S/$\overline{C}$ = 1: Shift both cursor and display
  - S/$\overline{C}$ = 0: Shift cursor only
- The R/$\overline{L}$ bit selects leftward or rightward movement of the display and/or cursor.
  - R/$\overline{L}$ = 1: Shift one character right
  - R/$\overline{L}$ = 0: Shift one character left

System Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	IF	N	F	*	*	20H to 3FH

RS = 0

This instruction initializes the system, and must be the first instruction executed after power-on.
- The IF bit selects between an 8-bit or a 4-bit MPU interface.
  - IF = 1: 8-bit MPU interface using DB7 to DB0.
  - IF = 0: 4-bit MPU interface using DB7 to DB4.
- The N and F bits select the number of display lines and the corresponding duty cycle, as listed in table 2.

TABLE 2 Combinations of Display Lines and Duty Cycle

N	F	Number of Line	Duty Ratio	Common Output Signal	Non-Selected Common Output Signal
0	0	1 line	1/8	COM1 to COM8	COM9 to COM16
0	1	1 line	1/11	COM1 to COM11	COM12 to COM16
1	*	2 lines	1/16	COM1 to COM16	—

Set CGRAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	ACR						40H to 7FH

RS = 0

This instruction
1. loads a new 6-bit address into the address counter.
2. sets the address counter to address CGRAM.

Once "Set CGRAM Address" has been executed, the contents of the address counter will be automatically modified after every access of CGRAM, as determined by the "Entry Mode Set" instruction.

If the "Set CGRAM Address" instruction is issued by the system MPU while the display is enabled, and if either the cursor is on or blink is on, pseudo-cursor or pseudo-blink appears. To prevent this, turn both the cursor and display blink off before loading a new CGRAM address.

The active width of the address counter, when it is addressing CGRAM, is 6-bits so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CGRAM.

Set DDRAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	ADD						

RS = 0

80H to CFH … 1 line
80H to A7H line 1 … 2 line
C0H to E7H line 2 … 2 line

This instruction
1. loads a new 7-bit address into the address counter.
2. sets the address counter to point to the DDRAM.

Once the "Set DDRAM Address" instruction has been executed, the contents of the address counter will be automatically modified after each access of DDRAM, as selected by the "Entry Mode Set" instruction.

The SED1278 has only 80 DDRAM locations. The valid address spaces for various display configurations are listed in table 3.

TABLE 3 Valid CGRAM Address Ranges

Number of Lines		Characters	ADR
1-line		80	00H to 4FH
2-line	1st line	40	00H to 27H
	2nd line	40	40H to 67H

Write Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DATA							

RS = 1

This instruction writes the data in DB7 to DB0 into either the CGRAM or the DDRAM. The RAM space (CG or DD), and the address in that space, that is accessed depends on whether a "Set CGRAM Address" or a "Set DDRAM Address" instruction was last executed, and on the parameters of that instruction.

The contents of the address counter will be automatically modified after each "Write Data", as determined by "Entry Mode Set". When data is written to the CGRAM, the DB7, DB6 and DB5 bits are not displayed directly as characters.

Read Only Instructions

Read Busy Flag/Address Counter

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BF	ACC						

RS = 1

Reading the instruction register yields the current value of the address counter and the busy flag. This instruction must be executed prior to any other instructions.

- ACC, the address counter value, will point to a location in either CGRAM or DDRAM, depending on the type of "Set RAM Address" instruction last sent.
  In "Busy Flag Check" immediately after executing "RAM Address Set" instruction, a valid address counter value can be read 5 clock cycles after the busy flag (BF) goes low.
  In "Busy Flag Check" immediately after executing "Write Data" instruction, a valid address counter value can be ready as soon as BF goes low.
- The BF bit shows the status of the busy flag.
  - BF = 1: SED1278 busy.
  - BF = 0: SED1278 ready for next instruction.

Read Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DATA							

RS = 1

This instruction reads data from either CGRAM or DDRAM, depending on the type of "Set RAM Address" instructions last sent. The address in that space depends on the "Set RAM Address" instructions parameters. Immediately before executing "Read Data", "Set CGRAM Address" or "Set DDRAM Address" must be executed.

The contents of the address counter are modified after each "Read Data", as determined by "Entry Mode Set". Display shift is not executed, independently of "Entry Mode Set".

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–3 to +7.0	V
Supply voltage (2)*	V_1 to V_5	–0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature × time**	T_{sol}	260, 10	°C, s
Power dissipation	P_D	300	mW

Notes: 1. $V_{DD} > V_1 > V_2 > V_3 > V_4 > V_5 > V_{SS}$
2. A flat package product can become less resistant to moisture if exposed to extreme temperatures. When mounting this package on a printed circuit board, use a soldering technique which avoids excessive thermal loading of the package resin.
3. All voltages assume V_{SS} = 0 V.

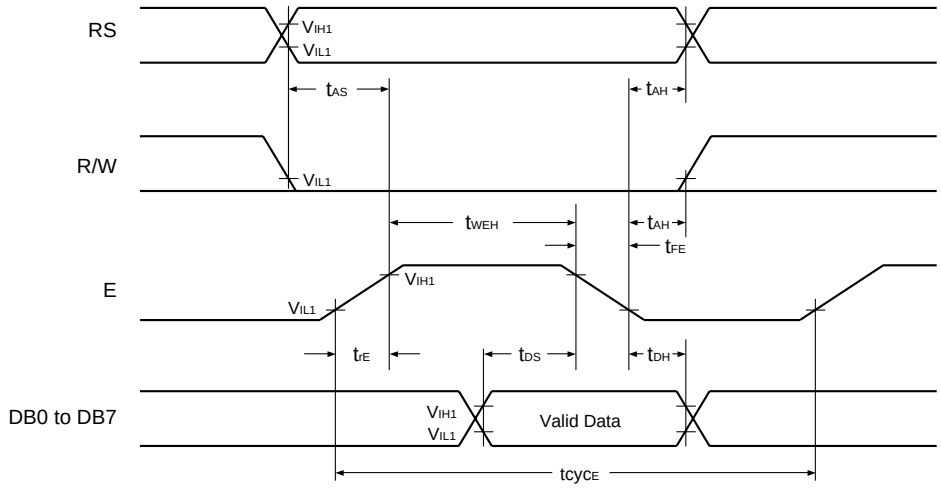
DC Characteristics

(V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Rating			Unit	Applicable Pins
			min	typ	max		
"H" level input voltage (1) (TTL)	V_{IH1}		2.0	—	V_{DD}	V	DB0 to DB7, RS, R/$\overline{W}$, E
"L" level input voltage (1) (TTL)	V_{IL1}		V_{SS}	—	0.8	V	
"H" level input voltage (2) (CMOS)	V_{IH2}		V_{DD}–1.0	—	V_{DD}	V	OSC1
"L" level input voltage (2) (CMOS)	V_{IL2}		V_{SS}	—	1.0	V	
"H" level output voltage (1) (TTL)	V_{OH1}	$-I_{OH}$ = 0.205 mA	2.4	—	—	V	DB0 to DB7
"L" level output voltage (1) (TTL)	V_{OL1}	I_{OL} = 1.6 mA	—	—	0.4	V	
"H" level output voltage (2) (CMOS)	V_{OH2}	$-I_{OH}$ = 0.04 mA	0.9V_{DD}	—	—	V	XSCL, LP, DO
"L" level output voltage (2) (CMOS)	V_{OL2}	I_{OL} = 0.04 mA	—	—	0.1V_{DD}	V	
Driver-on resistor (COM)	R_{COM}	| V_{COM}–V_n | = 0.5 V	—	2	10	kΩ	COM1 to COM16
Driver-on resistor (SEG)	R_{SEG}	| V_{SEG}–V_n | = 0.5 V	—	2.5	10	kΩ	SEG1 to SEG40
I/O leakage current	I_{IL}	V_{IN} = 0 to V_{DD}	—	—	1	µA	
Pull-up MOS current	–IP	V_{DD} = 5 V	50	125	250	µA	DB0 to CB7, RS, R/$\overline{W}$
Supply current	I_{OP}	Rf oscillation, from external clock V_{DD} = 5 V, f_{OSC} = f_{CP} = 270 kHz	—	0.5	0.8	mA	V_{DD}

AC Characteristics

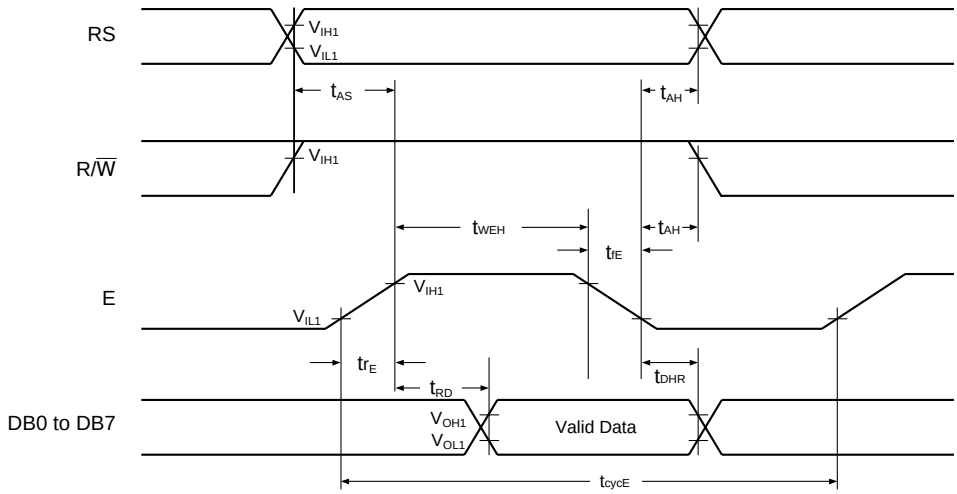
- MPU write cycle timing (write to SED1278)



(V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = –20 to 70°C)

Parameter	Symbol	Condition	Rating		Unit
			min	max	
Enable cycle time	t_{cycE}		500	—	ns
Enable "H" level pulsewidth	t_{WEH}		220	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	25	ns
RS, R/$\overline{W}$ setup time	t_{AS}		40	—	ns
RS, R/$\overline{W}$ address hold time	t_{AH}		10	—	ns
Data setup time	t_{DS}		60	—	ns
Write data hold time	t_{DH}		10	—	ns

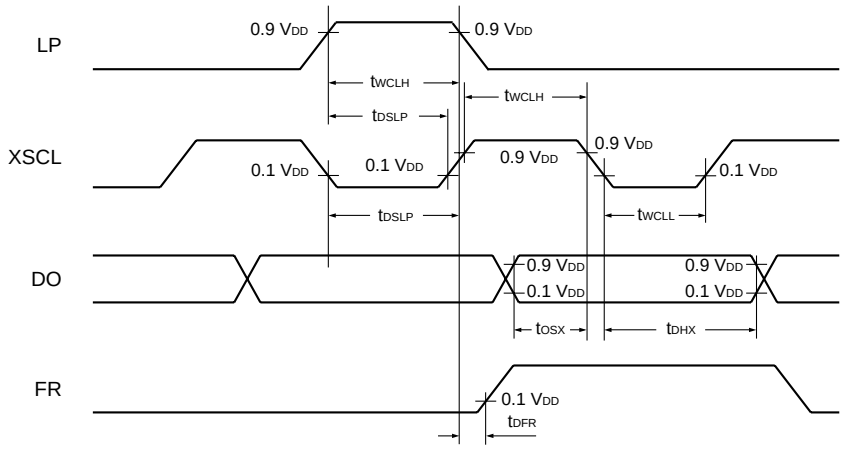
- MPU read cycle timing (read from SED1278)



(V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = –20 to 75°C)

Parameter	Symbol	Condition	Rating		Unit
			min	max	
Enable cycle time	t_{cycE}		500	—	ns
Enable "H" level pulsewidth	t_{WEH}		220	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	25	ns
RS, R/$\overline{W}$ setup time	t_{AS}		40	—	ns
RS, R/$\overline{W}$ address hold time	t_{AH}		10	—	ns
Read data setup time	t_{RD}	C_L = 100 pF	—	120	ns
Read data hold time	t_{DHR}		20	—	ns

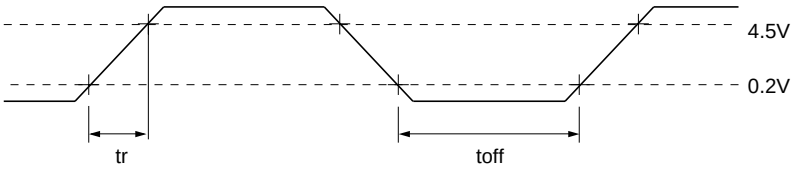
• External segment driver signal timing



(V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = –20 to 70°C)

Parameter	Symbol	Condition	Rating		Unit
			min	max	
Clock pulsewidth: High level	t_{WCLH}		0.8/2f_{OSC}	—	ns
Clock pulsewidth: Low level	t_{WCLL}		0.8/2f_{OSC}	—	ns
Latch pulse setup time	t_{DSLP}		0.7/2f_{OSC}	—	ns
Data setup time	t_{OSX}		0.7/2f_{OSC}	—	ns
Data hold time	t_{DHX}		0.7/2f_{OSC}	—	ns
FR delay	t_{DFR}		–1000	1000	ns

- Power-on reset timing



0.1ms ≤ tr ≤ 10ms

toff ≥ 1ms

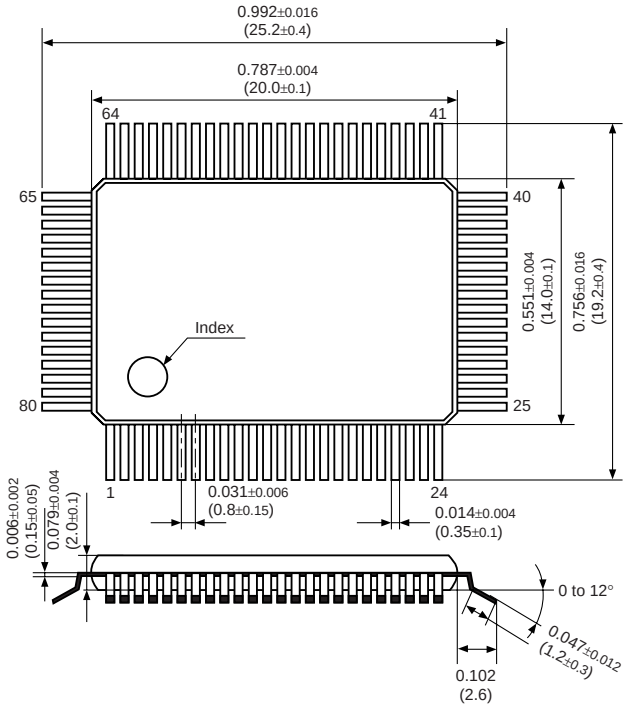
(Ta = –20 to 75 deg. C)

LCD Drive Voltages

Pin	Duty 1/8 or 1/11	Duty 1/16
V_1	3/4 (V_{DD} – V_5)	4/5 (V_{DD} – V_5)
V_2	2/4 (V_{DD} – V_5)	3/5 (V_{DD} – V_5)
V_3	2/4 (V_{DD} – V_5)	2/5 (V_{DD} – V_5)
V_4	1/4 (V_{DD} – V_5)	1/5 (V_{DD} – V_5)
V_5	V_5	V_5

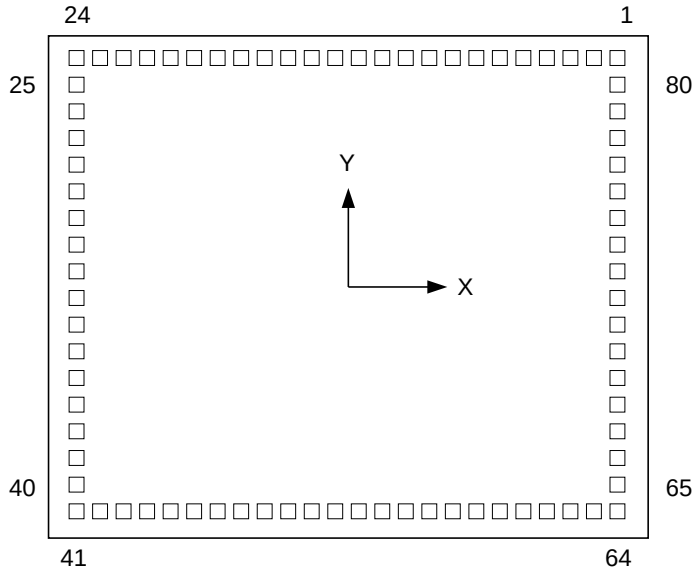
Mechanical Specifications

SED1278F Package Dimensions



SED1278D Package Dimensions

Chip size: 4.50 mm × 3.67 mm
Chip thickness: 400 µm
Pad size: 109 µm × 109 µm
Pad pitch: 182 µm



Pad		X (μm)	Y (μm)
Number	Name		
1	SEG22	2087	1671
2	SEG21	1905	1671
3	SEG20	1723	1671
4	SEG19	1541	1671
5	SEG18	1359	1671
6	SEG17	1177	1671
7	SEG16	995	1671
8	SEG15	814	1671
9	SEG14	633	1671
10	SEG13	452	1671
11	SEG12	272	1671
12	SEG11	91	1671
13	SEG10	–91	1671
14	SEG9	–272	1671
15	SEG8	–452	1671
16	SEG7	–633	1671
17	SEG6	–814	1671
18	SEG5	–995	1671
19	SEG4	–1177	1671
20	SEG3	–1359	1671
21	SEG2	–1541	1671
22	SEG1	–1723	1671
23	GND	–1905	1671
24	OSC1	–2087	1671
25	OSC2	–2087	1365
26	V_1	–2087	1183
27	V_2	–2087	1001
28	V_3	–2087	819
29	V_4	–2087	637
30	V_5	–2087	455
31	LP	–2087	273
32	XSCL	–2087	91
33	V_{DD}	–2087	–91
34	FR	–2087	–273
35	DO	–2087	–455
36	RS	–2087	–637
37	R/$\overline{W}$	–2087	–819
38	E	–2087	–1001
39	DB0	–2087	–1183
40	DB1	–2087	–1365

Pad		X (μm)	Y (μm)
Number	Name		
41	DB2	–2087	–1671
42	DB3	–1905	–1671
43	DB4	–1723	–1671
44	DB5	–1541	–1671
45	DB6	–1359	–1671
46	DB7	–1177	–1671
47	COM1	–995	–1671
48	COM2	–814	–1671
49	COM3	–633	–1671
50	COM4	–452	–1671
51	COM5	–272	–1671
52	COM6	–91	–1671
53	COM7	91	–1671
54	COM8	272	–1671
55	COM9	452	–1671
56	COM10	633	–1671
57	COM11	814	–1671
58	COM12	995	–1671
59	COM13	1177	–1671
60	COM14	1359	–1671
61	COM15	1541	–1671
62	COM16	1723	–1671
63	SEG40	1905	–1671
64	SEG39	2087	–1671
65	SEG38	2087	–1365
66	SEG37	2087	–1183
67	SEG36	2087	–1001
68	SEG35	2087	–819
69	SEG34	2087	–637
70	SEG33	2087	–455
71	SEG32	2087	–273
72	SEG31	2087	–91
73	SEG30	2087	91
74	SEG29	2087	273
75	SEG28	2087	455
76	SEG27	2087	637
77	SEG26	2087	819
78	SEG25	2087	1001
79	SEG24	2087	1183
80	SEG23	2087	1365

OPERATION

The Busy Flag

The SED1278 takes between 10 and 410 clock cycles to execute instructions. During that period additional instructions should not be issued. The device is provided with a busy flag to let the user check the internal state of the chip. BF should be 0 before another instruction is issued.
If the busy flag is not checked between instructions the user must arrange for a guaranteed delay of more than the instruction execution time, before issuing the next instruction.

4-Bit MPU Interface

If a "System Set" instruction is issued with bit 4 set to 0, then the SED1278 will operate with a 4-bit MPU data bus interface.
If a 4-bit interface is used, the 8-bit instructions are written nibble by nibble; the high-order nibble being written first, followed by the low-order nibble. It is not necessary to check the busy flag between writing separate nibbles of individual instructions.
Reading the Busy Flag/Address Counter yields the high-order nibble first, followed by the low-order nibble.

System Initialization

Power-on reset

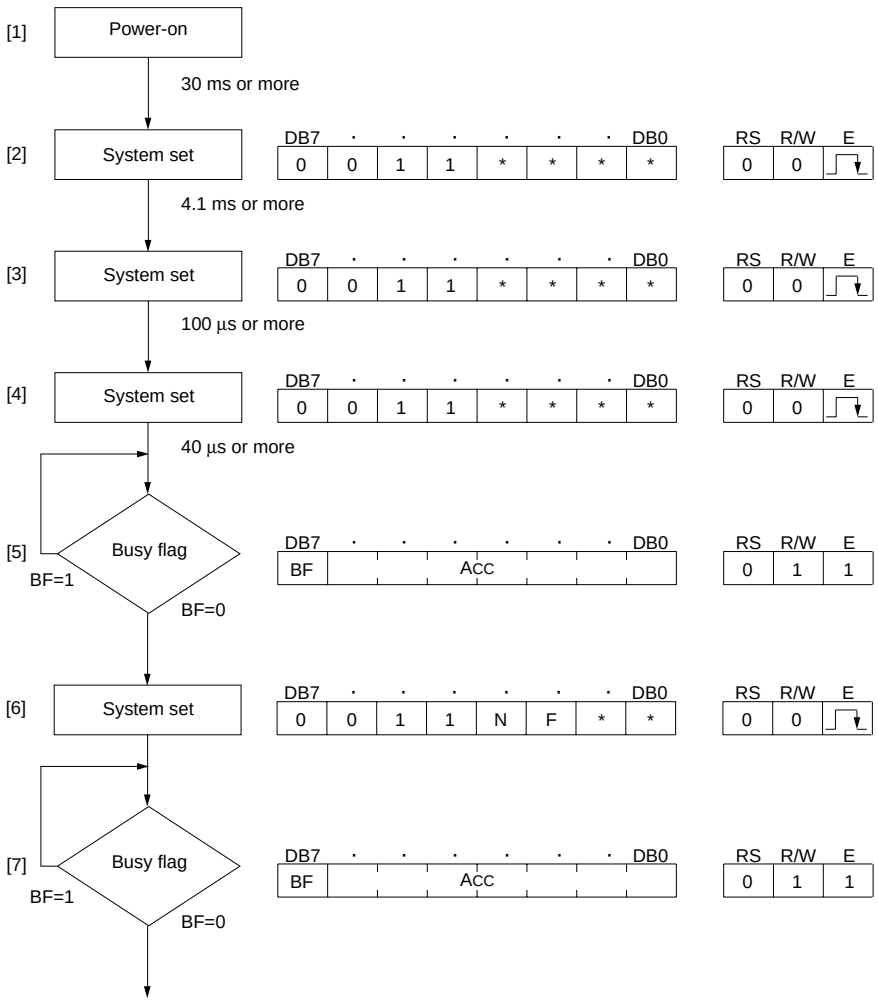
Although the SED1278 has no external reset input, it will automatically reset on system power-on. The sequence starts once $V_{DD} < 4.5$ V.
While the SED1278 is resetting the busy flag is set to 1. The reset takes about 3,750 clock cycles. For example if $f_{OSC} = 250$ kHz, the reset sequence takes about 30 ms.
Reset places the SED1278 in a state where

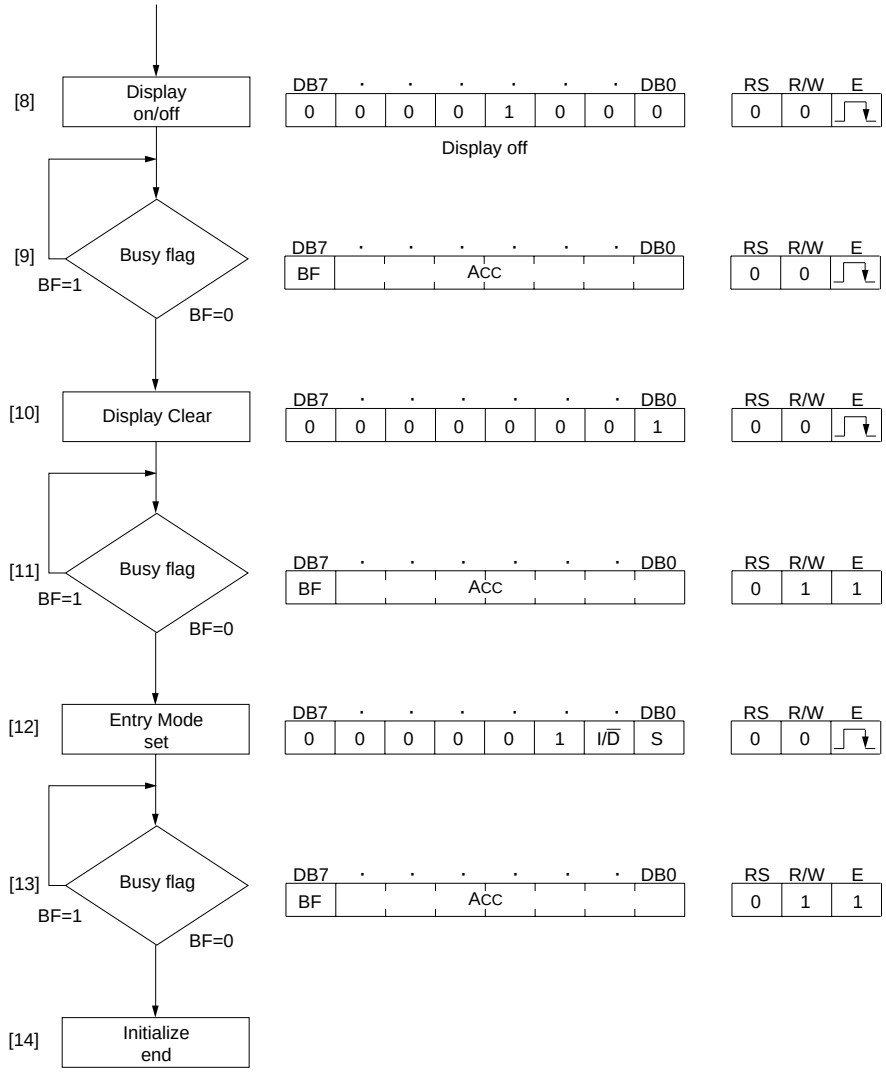
- the display is clear.
- the system configuration corresponds to
  - IF = 1: 8-bit MPU interface
  - N = 0: 1-line display
  - F = 0: 1/8 duty cycle
- the display configuration corresponds to
  - D = 0: Display off
  - C = 0: Cursor off
  - B = 0: Blink off
- the entry mode is set to
  - I/$\overline{D}$ = 1: Increment
  - S = 1: No display shift

Software initialization

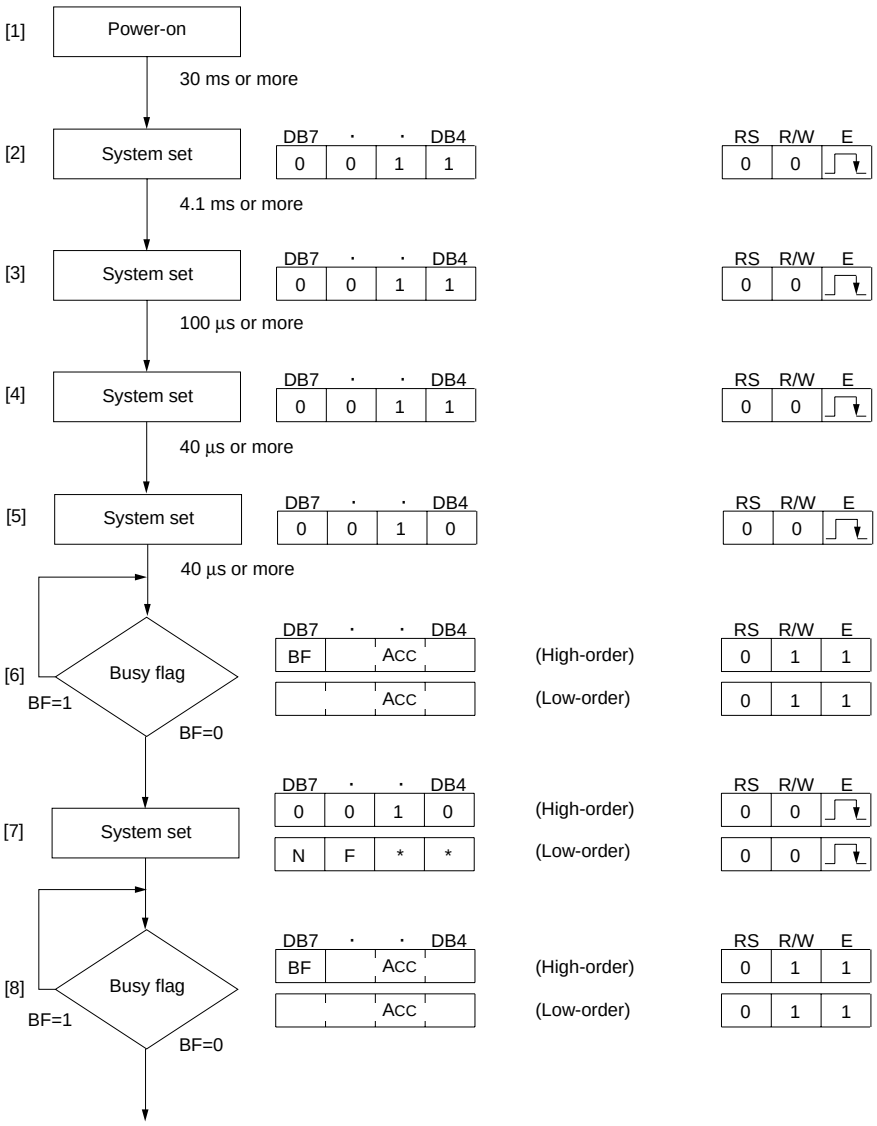
Initialization during power-on reset involves several unstable factors related to power-supply output fluctuations. For this reason it is strongly recommended that a software initialization sequence is followed.

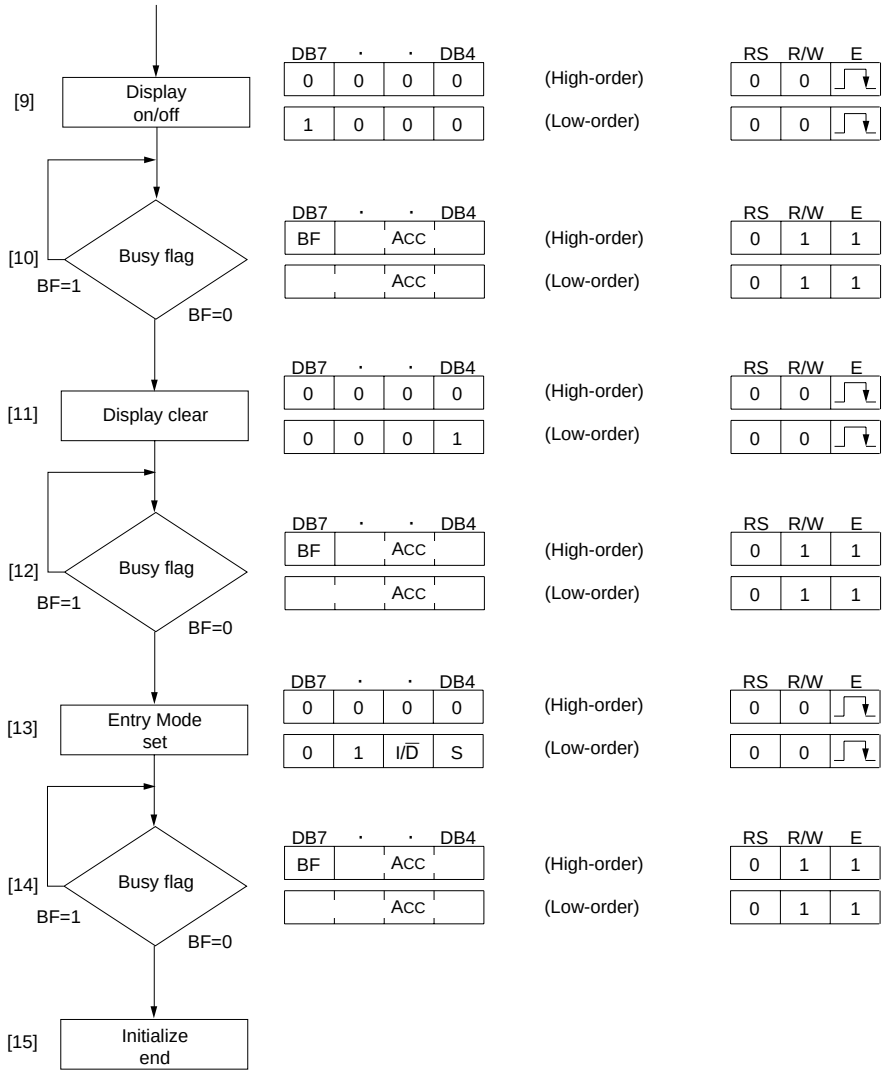
- Software Initialization (8-bit MPU bus, f_{OSC} = 250 kHz)




[8]
Display on/off
DB7 · · · · · · DB0
0 0 0 0 1 0 0 0
RS R/W E
0 0
Display off
[9]
Busy flag
BF=1
BF=0
DB7 · · · · · · DB0
BF ACC
RS R/W E
0 0
[10]
Display Clear
DB7 · · · · · · DB0
0 0 0 0 0 0 0 1
RS R/W E
0 0
[11]
Busy flag
BF=1
BF=0
DB7 · · · · · · DB0
BF ACC
RS R/W E
0 1 1
[12]
Entry Mode set
DB7 · · · · · · DB0
0 0 0 0 0 1 I/D S
RS R/W E
0 0
[13]
Busy flag
BF=1
BF=0
DB7 · · · · · · DB0
BF ACC
RS R/W E
0 1 1
[14]
Initialize end

- Software Initialization (4-bit MPU bus, f_{OSC} = 250 kHz)




[9]
Display on/off
DB7 · · DB4
0 0 0 0 (High-order)
1 0 0 0 (Low-order)
RS R/W E
0 0 (High-order)
0 0 (Low-order)
[10]
Busy flag
BF=1
BF=0
DB7 · · DB4
BF ACC (High-order)
ACC (Low-order)
RS R/W E
0 1 1 (High-order)
0 1 1 (Low-order)
[11]
Display clear
DB7 · · DB4
0 0 0 0 (High-order)
0 0 0 1 (Low-order)
RS R/W E
0 0 (High-order)
0 0 (Low-order)
[12]
Busy flag
BF=1
BF=0
DB7 · · DB4
BF ACC (High-order)
ACC (Low-order)
RS R/W E
0 1 1 (High-order)
0 1 1 (Low-order)
[13]
Entry Mode set
DB7 · · DB4
0 0 0 0 (High-order)
0 1 I/D S (Low-order)
RS R/W E
0 0 (High-order)
0 0 (Low-order)
[14]
Busy flag
BF=1
BF=0
DB7 · · DB4
BF ACC (High-order)
ACC (Low-order)
RS R/W E
0 1 1 (High-order)
0 1 1 (Low-order)
[15]
Initialize end

THE CHARACTER GENERATOR

Character Generator ROM (CGROM)

The SED1278 contains a 240 character, masked CGROM. Each character is 5×10 pixels, for 1/11 duty cycle compatibility. Refer to Appendix A for available codes and their corresponding fonts.
Because the CGROM is masked, customers may arrange to have their own CGROM masks made.
A custom mask allows the user to have

- their own character set.
- a character set of up to 256 characters.

Please contact the SEIKO EPSON Marketing Department for further information.
If a custom CGROM is used, two things should be noted.

1. The "Clear Display" instruction relies on the character whose code is 20H being a blank.
2. If more than 240 ROMed characters are specified, then the number of CGRAM characters available is correspondingly reduced. The physical RAM space is still available, and is available for use as memory, however it will no longer have an associated character code.
3. The character ROM implemented in a particular chip is indicated by a two character suffix attached to the device number, for example SED1278F0A.

Character Generator RAM (CGRAM)

The SED1278 has 64 bytes of CGRAM, allowing the user to program up to 8 characters.

5×8 pixel font (1/8 or 1/16 duty cycle)

The maximum character height is 8 pixels, however if a cursor is used row 7 should be all zeros. 8 such characters are available to the user.
The CGRAM address is made up of the following components.

- The least significant three bits, a_2 to a_0, specify the row number of the character data.
- Bits a_5 to a_3 are made up of the least significant three bits of the character code.
- The most significant bit, a_7, is ignored.
  Figure 1 shows an example 5×8 pixel font.

CGRAM address						CGRAM data (Character pattern)							
A5	·	·	·	·	A0	DB7	·	·	·	·	·	·	DB0
0	0	0	0	0	0	*	*	*	0	0	0	0	[1]
0	0	0	0	0	1	*	*	*	0	0	0	0	[1]
0	0	0	0	1	0	*	*	*	0	[1]	0	0	[1]
0	0	0	0	1	1	*	*	*	[1]	[1]	[1]	[1]	[1]
0	0	0	1	0	0	*	*	*	0	[1]	0	0	0
0	0	0	1	0	1	*	*	*	0	0	0	0	0
0	0	0	1	1	0	*	*	*	0	0	0	0	0
0	0	0	1	1	1	*	*	*	0	0	0	0	0

Figure 1 A 5×8 Pixel Font

5×11 pixel font (1/11 duty cycle)

The maximum character height is 11 pixels, however if a cursor is used row 10 must be left blank.
The SED1278 requires that, although the maximum character height is 11 rows, each character is allocated 16 rows (bytes) of address space. The last five bytes are ignored.
The CGRAM address is made up of the following components.

- The least significant 4 bits, a_3 to a_0, specify the row number of the character data.
- Bits a_5 and a_4 correspond to bits 2 and 3, respectively, of the character code.
- The most significant bit, a_7, is ignored.

Figure 2 shows an example 5×11 pixel font.

CGRAM address						CGRAM data							
A5	·	·	·	·	A0	DB7	·	·	·	·	·	·	DB0
0	0	0	0	0	0	*	*	*	0	0	0	0	1
0	0	0	0	0	1	*	*	*	0	0	0	0	1
0	0	0	0	1	0	*	*	*	0	0	0	0	1
0	0	0	0	1	1	*	*	*	0	0	1	0	1
0	0	0	1	0	0	*	*	*	0	1	0	0	1
0	0	0	1	0	1	*	*	*	1	1	1	1	1
0	0	0	1	1	0	*	*	*	0	1	0	0	0
0	0	0	1	1	1	*	*	*	0	0	1	0	0
0	0	1	0	0	0	*	*	*	0	0	0	0	0
0	0	1	0	0	1	*	*	*	0	0	0	0	0
0	0	1	0	1	0	*	*	*	0	0	0	0	0
0	0	1	0	1	1	*	*	*	*	*	*	*	*
0	0	1	1	0	0	*	*	*	*	*	*	*	*
0	0	1	1	0	1	*	*	*	*	*	*	*	*
0	0	1	1	1	0	*	*	*	*	*	*	*	*
0	0	1	1	1	1	*	*	*	*	*	*	*	*

Figure 2 A 5×11 Pixel Font

LCD INTERFACE

LCD Drive Voltages

The SED1278 generates segment and common drive signals using the voltages supplied to pins V_1, V_2, V_3, V_4 and V_5. The voltage levels at these pins depend on the duty cycle of the display. The specifications of these voltages.

The simplest way of producing these voltages is to use a resistive dividing network.

Figures 3 and 4 show examples of networks for 1/8, or 1/11, and 1/16 duty cycles respectively.

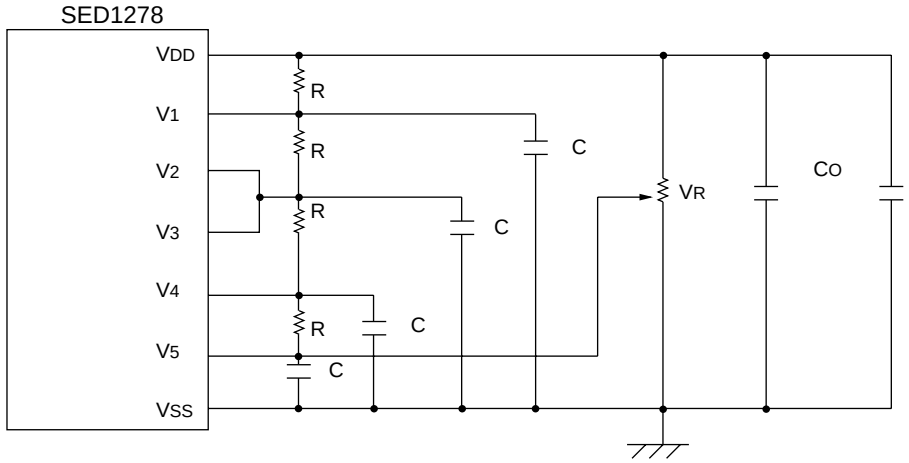


Figure 3 LCD Drive Voltage Network – 1/8 or 1/11 Duty Cycle

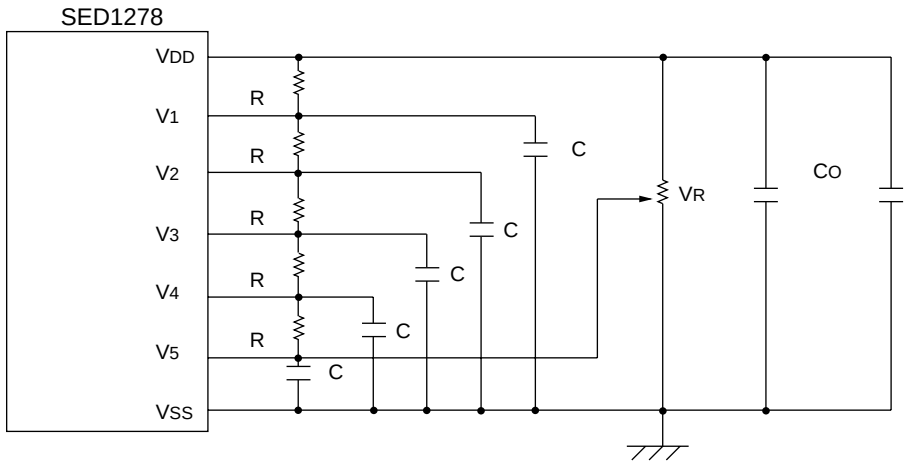


Figure 4 LCD Drive Voltage Network – 1/16 Duty Cycle

Notes: 1. V_5 is set using a potentiometer and (V_{DD}–V_{SS}).
2. The power supply to the SED1278 should be bypassed with a capacitor, C_O, of at least 0.1 µF placed as close to the chip as possible.

LCD Drive Signal Waveforms

The segment and common drive waveforms generated by the SED1278, for various duty cycle ratios, are shown in figures 5, 6 and 7.

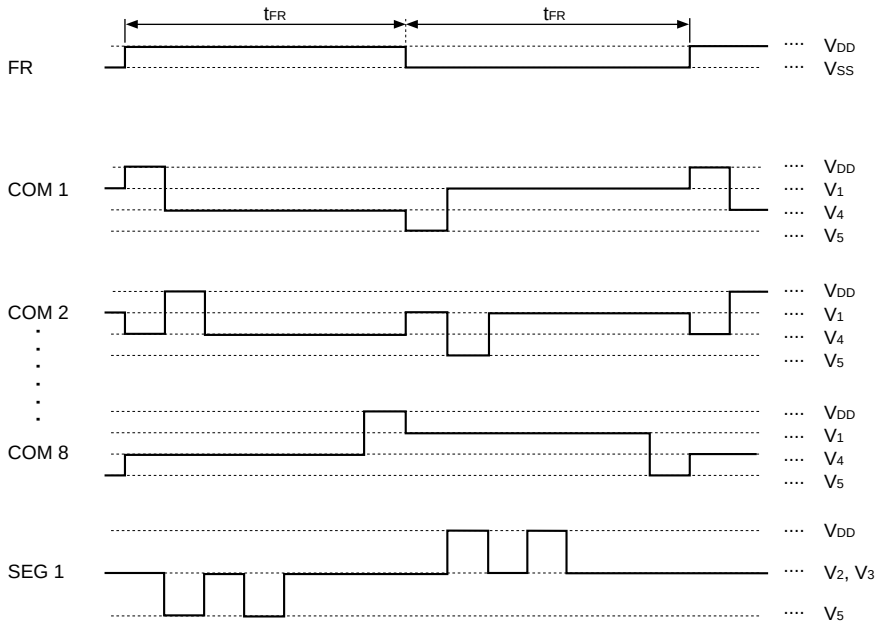


Figure 5 1/8 Duty Cycle Drive Waveforms

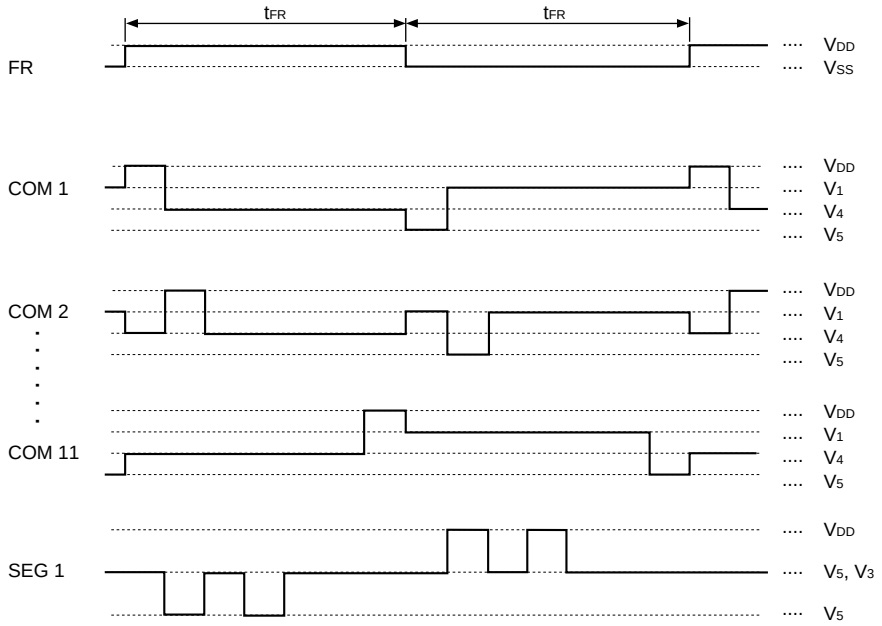


Figure 6 1/11 Duty Cycle Drive Waveforms

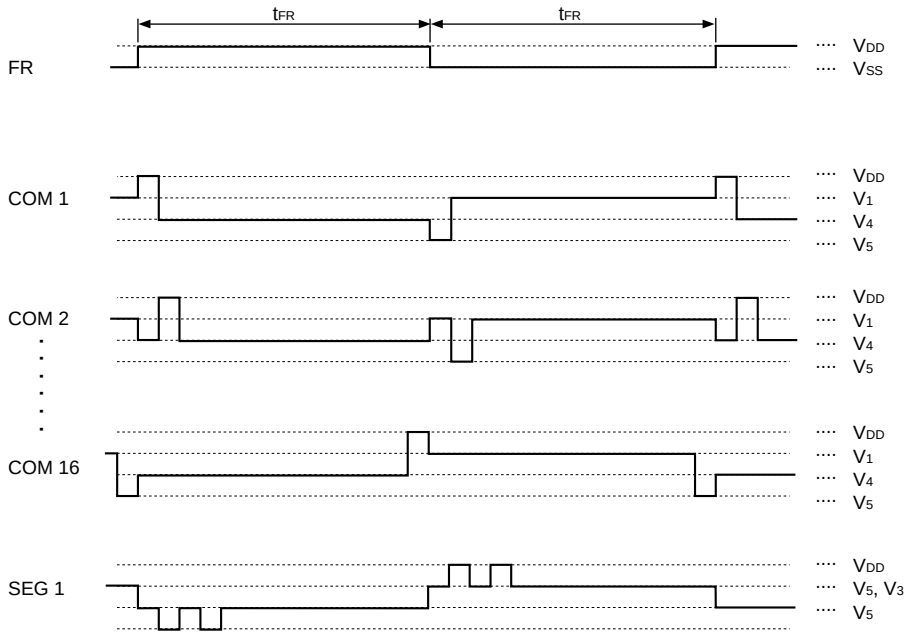
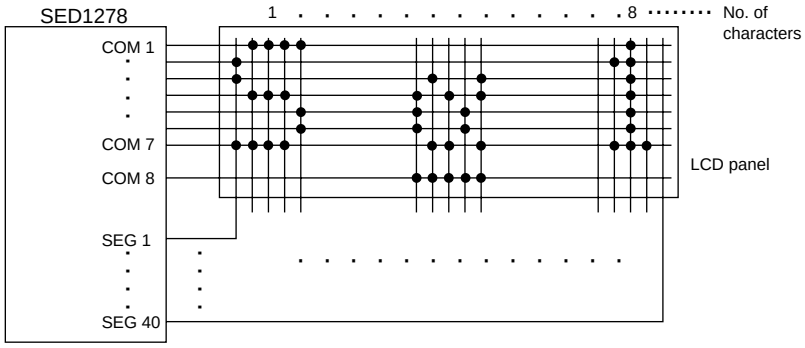


Figure 7 1/16 Duty Cycle Drive Waveforms

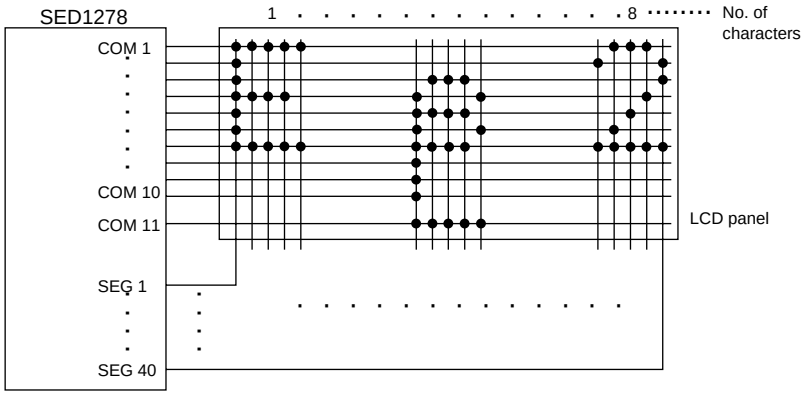
LCD Interface Configurations

The SED1278 has 16 common and 40 segment drive outputs, enabling the chip to drive up to 16 characters by itself. The drive capability can be expanded to 80 characters, by using SED1181FLA external segment drivers.

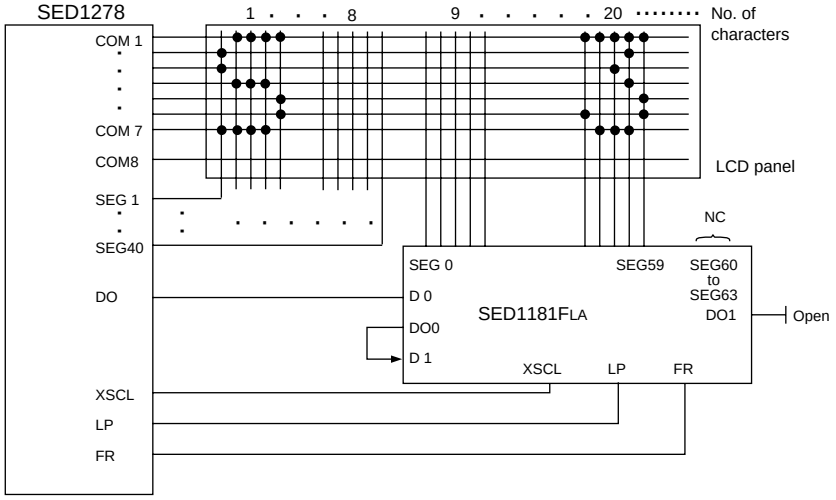
- 1 line
- 8 characters
- 5×7 pixels + cursor
- 1/8 duty cycle
- System set: N = 0, F = 0



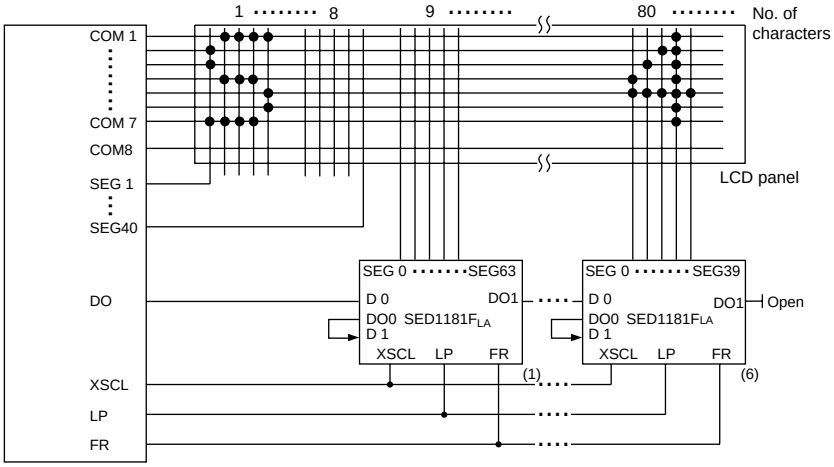
- 1 line
- 8 characters
- 5×10 pixels + cursor
- 1/11 duty cycle
- System set: N = 0, F = 1



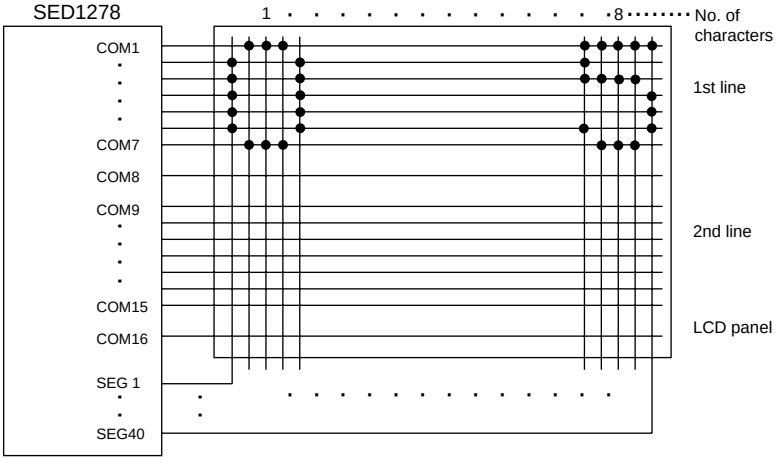
- 1 line
- 20 characters
- 5×7 pixels + cursor
- 1/8 duty cycle
- System set: N = 0, F = 0



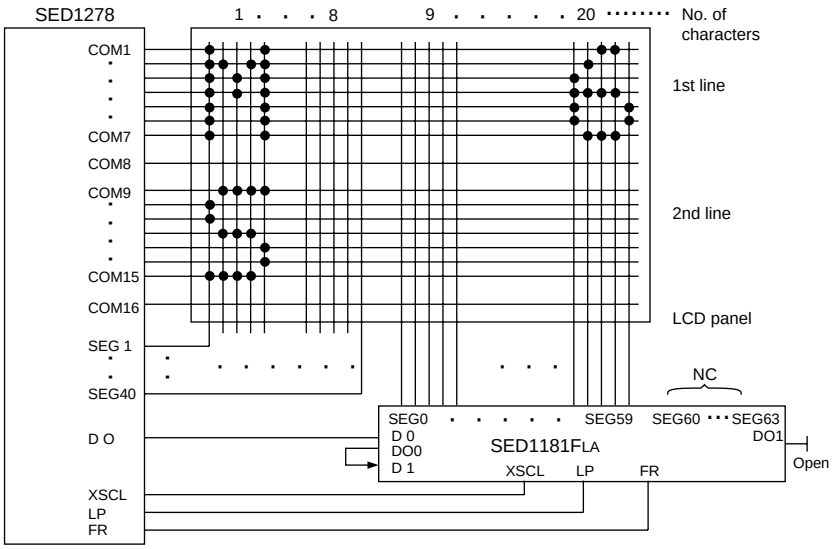
- 1 line
- 80 characters
- 5×7 pixels + cursor
- 1/8 duty cycle
- System set: N = 0, F = 0



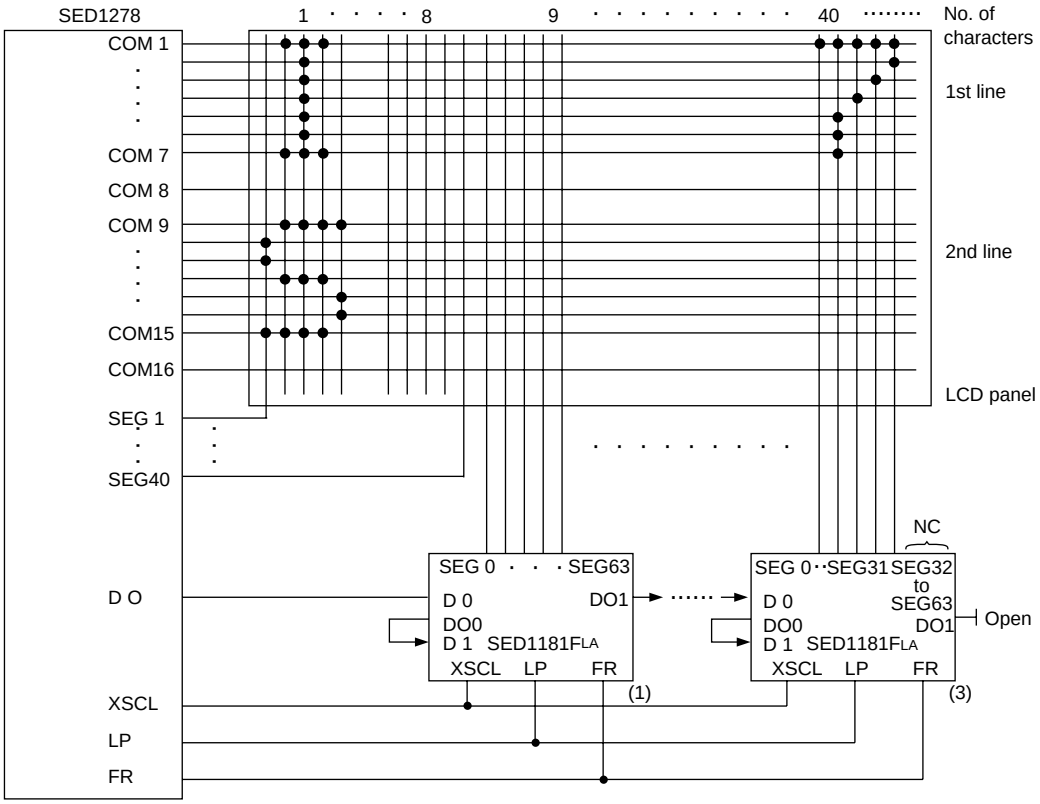
- 2 line
- 8 characters
- 5×7 pixels + cursor
- 1/16 duty cycle
- System set: N = 1, F = don't care



- 2 line
- 20 characters
- 5×7 pixels + cursor
- 1/16 duty cycle
- System set: N = 1, F = don't care



- 2 line
- 40 characters
- 5×7 pixels + cursor
- 16 duty cycle
- System set: N = 1, F = don‘t care



MPU INTERFACE

The SED1278 has selectable 8- or 4-bit MPU interface. An example of a typical 8-bit MPU interface is shown figure 8.

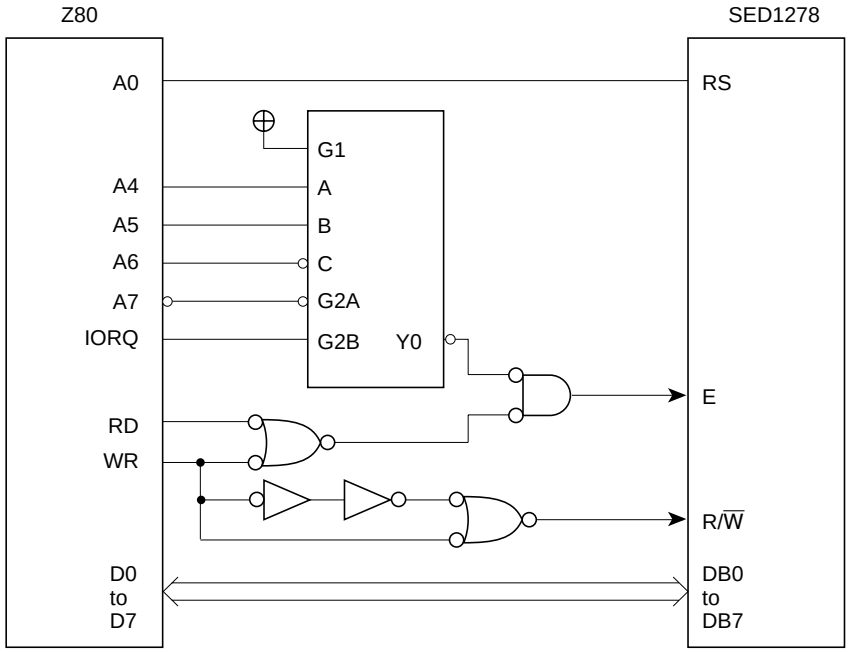


Figure 8 Interfacing the SED1278 to the Zilog Z80®

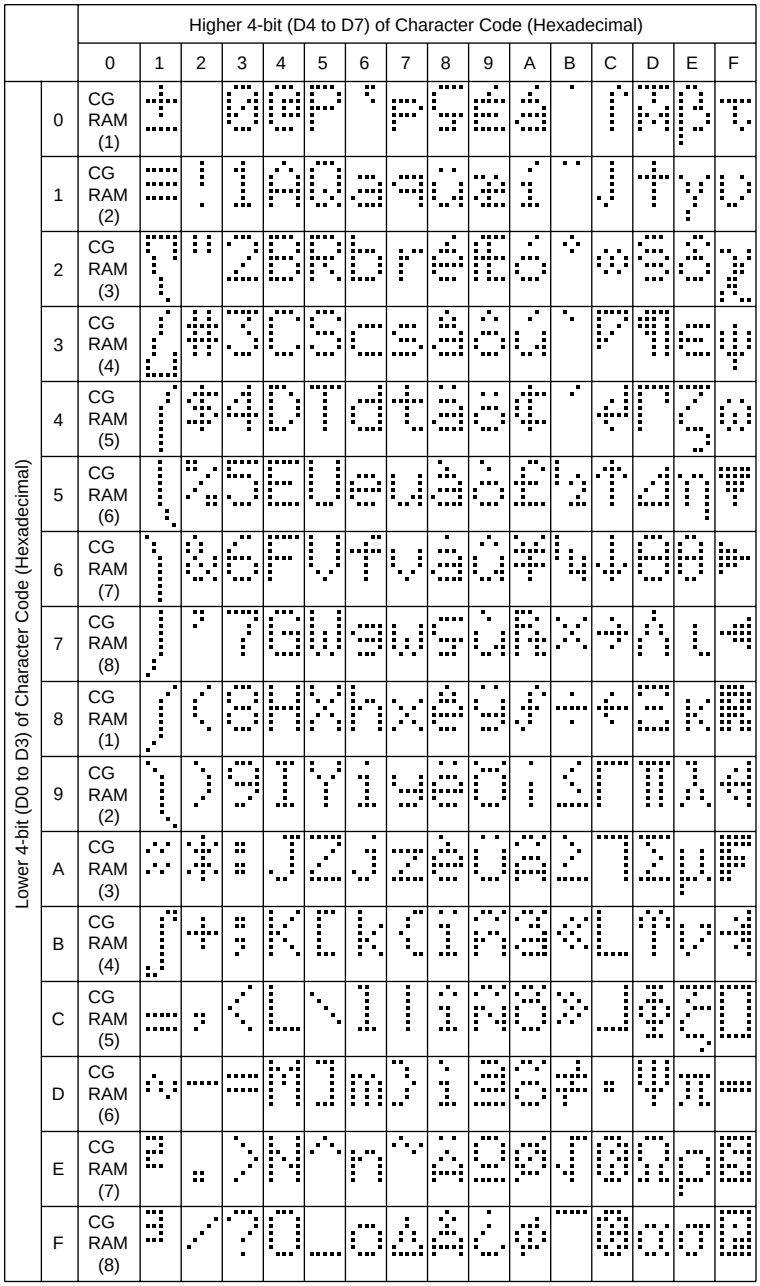
COMPARISON WITH HD44780 BY HITACHI

Item	HD44780 (Hitachi)	SED1278
Data display RAM	80 bytes	←
Character generator ROM Character font	192 types 5 × 7: 160 types 5 × 10: 32 types	240 types 5 × 10: 240 types
Character generator RAM	64 bytes	←
LCD drive output	16 common driver outputs 40 segment drive outputs	←
Character font (with cursor)	5 × 8 dots (1/8 and 1/16 duty) 5 × 11 dots (1/1 duty)	←
Conversion to duty	1/8, 1/11, 1/16	←
LCD drive voltage (V_{DD}–V_5)	Max. 13.5 V Min. 4.6 V	Max. 1 V_{DD} Min. 3 V
LCD drive waveform	Waveform A (Single frame AC drive)	Waveform D (Dual frame AC drive)
E pulse width	450 nsec	220 nsec
Timing to change the address counter subsequent to CGRAM and DDRAM data writing and reading	The contents of address counter are determined 1.5 clock after release of busy state (6 microseconds at f_{OSC} = 250 kHz).	The contents of address counter are determined immediately after release of busy state.
No. of instructions	11	←
Reset terminal	Not provided	←
Chip selector terminal	Not provided	←
Power-on reset terminal	Provided	←
Extension segment driver	Hitachi HD44100: 40 outputs SED1181F$_{LA}$: 64 outputs	←
Package	80-pin plastic flat package	←
Pin layout		Pin compatible

APPENDIX A: CHARACTER CODES AND FONTS

SED1278F0A/SED1278D0A

SED1278F0B/SED1278D0B



SED1278F0C/SED1278D0C

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	CG RAM (1)															
	1	CG RAM (2)															
	2	CG RAM (3)															
	3	CG RAM (4)															
	4	CG RAM (5)															
	5	CG RAM (6)															
	6	CG RAM (7)															
	7	CG RAM (8)															
	8	CG RAM (1)															
	9	CG RAM (2)															
	A	CG RAM (3)															
	B	CG RAM (4)															
	C	CG RAM (5)															
	D	CG RAM (6)															
	E	CG RAM (7)															
	F	CG RAM (8)															

SED1278F0E/SED1278D0E

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	CG RAM (1)															
	1	CG RAM (2)															
	2	CG RAM (3)															
	3	CG RAM (4)															
	4	CG RAM (5)															
	5	CG RAM (6)															
	6	CG RAM (7)															
	7	CG RAM (8)															
	8	CG RAM (1)															
	9	CG RAM (2)															
	A	CG RAM (3)															
	B	CG RAM (4)															
	C	CG RAM (5)															
	D	CG RAM (6)															
	E	CG RAM (7)															
	F	CG RAM (8)															

SED1278F0G/SED1278D0G

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	CG RAM (1)															
	1	CG RAM (2)															
	2	CG RAM (3)															
	3	CG RAM (4)															
	4	CG RAM (5)															
	5	CG RAM (6)															
	6	CG RAM (7)															
	7	CG RAM (8)															
	8	CG RAM (1)															
	9	CG RAM (2)															
	A	CG RAM (3)															
	B	CG RAM (4)															
	C	CG RAM (5)															
	D	CG RAM (6)															
	E	CG RAM (7)															
	F	CG RAM (8)															

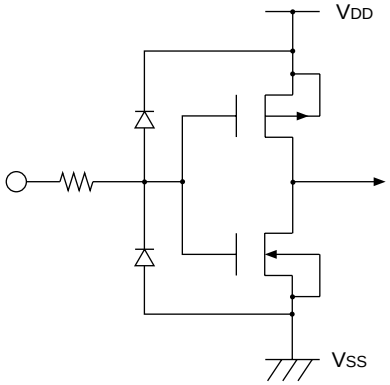
SED1278F0H/SED1278D0H

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	CG RAM (1)															
	1	CG RAM (2)															
	2	CG RAM (3)															
	3	CG RAM (4)															
	4	CG RAM (5)															
	5	CG RAM (6)															
	6	CG RAM (7)															
	7	CG RAM (8)															
	8	CG RAM (1)															
	9	CG RAM (2)															
	A	CG RAM (3)															
	B	CG RAM (4)															
	C	CG RAM (5)															
	D	CG RAM (6)															
	E	CG RAM (7)															
	F	CG RAM (8)															

APPENDIX B: PIN CONSTRUCTION

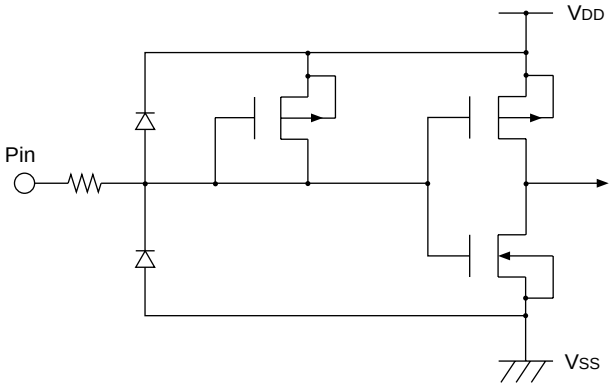
Input Pin Type 1

- E
- OSC1



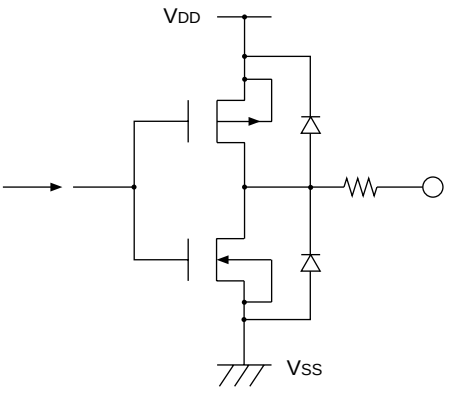
Input Pin Type 2

- RS
- R/$\overline{W}$



Output Pin

- OSC2
- XSCL, LP, FR, DO



I/O Pin

- DB0 to DB7