S1D13781

S1D13781 WQVGA LCD Controller

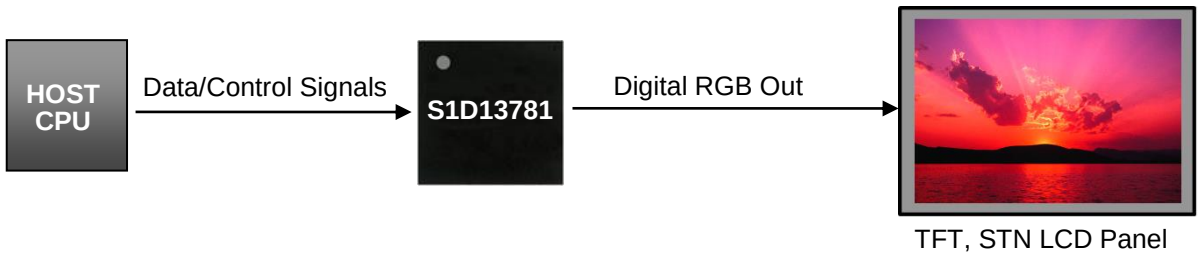
The S1D13781 is a multi-purpose graphics LCD controller with 384 KB embedded SRAM display buffer which supports both RGB interface TFT and CSTN panels. The S1D13781 supports most popular CPU interfaces in both 8/16-bit and direct/indirect variations. The embedded display buffer allows WQVGA up to 480x272 at 24 bpp or 800x480 8 bpp for single layer display, or 480x272 at 16 bpp (main layer) and 480x272 at 8 bpp (PIP layer) for two layer display.

The S1D13781's combination of multiple CPU interfaces and display interface types offers a versatile, yet easy to develop display system. Additionally, it offers multiple window support, transparency and alpha blending functions, as well as 2D BitBLT functions. It is a flexible, low cost, low power, single chip solution designed to meet the demands of embedded markets, such as office automation, factory automation, and building equipment, where total system cost and battery life are major concerns. It's impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

FEATURES

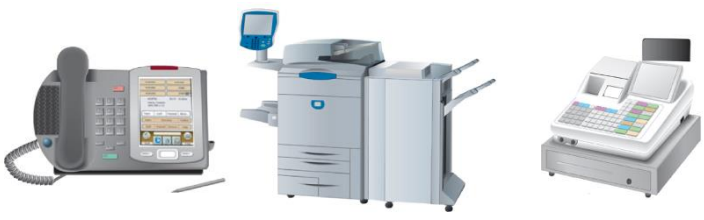
- Embedded 384 KB display buffer
- Direct and indirect CPU interfaces
- 8/16-bit data bus width
- SPI CPU interface
- Support for single panel implementation:
  - RGB interface TFT panel
  - Color and monochrome STN
- Programmable resolutions up to 800x480 @ 8 bpp
- Programmable color depth up to 24 bpp
- Multiple window support for Main and PIP
- SwivelView™ 90°, 180°, 270° rotation
- General purpose input/output pins
- LUT 256x24bitx3pcs for both main and PIP layer
- Alpha blending, transparency, flashing
- 2D BitBLT Engine
- Software initiated power save mode
- H/PIOVDD: 3.3 or 1.8V CORE/PLLVDD: 1.5V
- Clocks can be selected from embedded PLL or digital clock inputs
- Temperature range: -40° ~ 85°C
- Package: QFP 100-pin, 0.5mm pin pitch

SYSTEM BLOCK DIAGRAM



S1D13781 Features

- 384 KB SRAM
- 2D BitBLT Engine
- 2 layer support
- Alpha blending and transparency
- PIP layer flashing



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DESCRIPTION

CPU Interface

- Support for most popular CPU interfaces
- Direct and indirect addressing
- 8/16-bit interface support
- SPI

Display Support

- Single panel implementation can be:
  - RGB Interface TFT panel
  - Color and monochrome STN
- 16/18/24-bit color TFT
- Programmable resolutions up to 800x480 @ 8 bpp
- Programmable color depths up to 24 bpp

Display Features

- Multiple window support for Main and PIP windows
- Alpha blending and transparency
- PIP flashing
- LUT 256x24bitx3pcs for both Main and PIP layer
- SwivelView™ 90°, 180°, 270° display image rotation

Display Memory

- 384 KB of embedded SRAM
- Maximum resolution for WQVGA:
  - 1 layer: 480x272 @ 24 bpp
    or 800x480 @ 8 bpp
  - 2 layer: Main 480x272 @ 16 bpp
    and PIP 480x272 @ 8 bpp

Miscellaneous

- 2D BitBLT Engine
- Internal system clock: 66MHz
- Software initiated power save mode
- Multiple general purpose input/output pins
- Flexible clock structure:
- Embedded PLL
- Digital clock inputs
- Operating temperature range: -40°~ 85°C
- PLL/COREVDD 1.5 volts
  IO/HIOVDD 3.3 or1.8 volts
- Package: QFP 100-pin, 0.5mm pin pitch

For more information on the S1D13781 and other Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html