CR timer

BU2302/BU2302F/BU2305/BU2305F

The BU2302/F and BU2305/F are general-purpose ICs used in timers. The timer off time is based on the oscillation frequency that is determined by the external CR connected to the internal oscillator circuit.
The BU2302/F is an ideal timer IC for applications in which the output of a device such as a battery charger is turned on for a given period of time. When the timer set pin (SET) is LOW, the IC is reset to its initial state. When the SET pin is HIGH, oscillation begins and the timer is activated. Oscillation stops when the end of the set time period is reached.
The BU2305/F is ideal for applications such as sleep timers in radios and radio cassette players. When the timer set pin (SETB) is LOW, oscillation begins. The timer is set through the chatter prevention circuit, and the output is turned on and off repeatedly.

●Applications
Timers

●Features
1) Low power consumption because of CMOS process.
2) Wide operating voltage range of 1.8 to 6.0V.
3) Output is Nch open drain.
4) Oscillation frequency (time) can be set freely, using external CR.

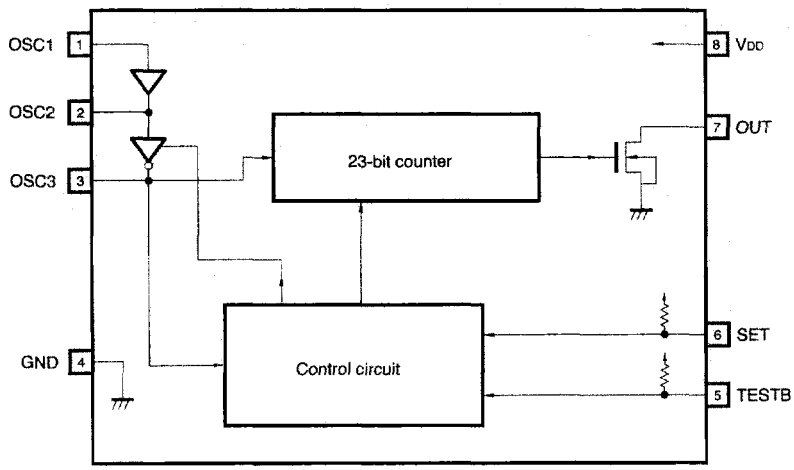
●Absolute maximum ratings

Prameter	Symbol	Limits	Unit
Output voltage	V_{DD}	−0.3~7.5	V
Power supply voltage	V_{OUT}	−0.3~7.5	V
Power dissipation	Pd	500 (DIP8 - T8) *1	mW
		350 (SOP8) *2	
Operating temperature	Topr	−20~75	℃
Storage temperature	Tstg	−50~150	℃

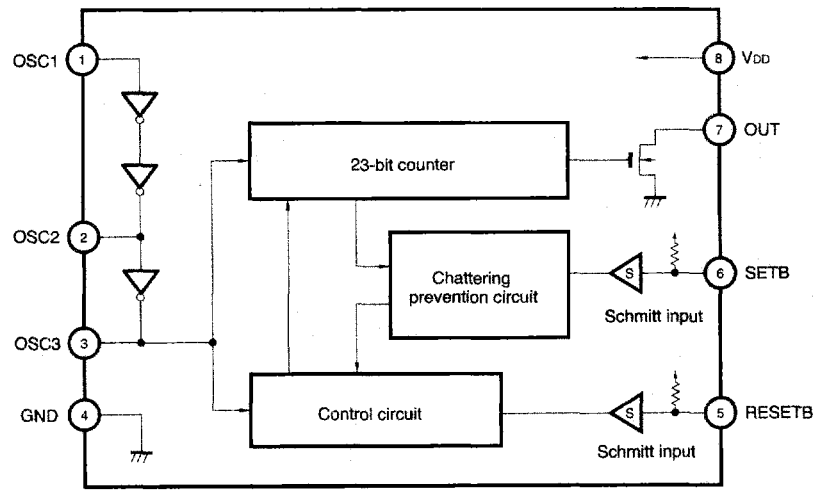
*1 Reduce power by 4.0 mW for each 1°C that the temperature rises.
*2 Reduce power by 2.8 mW for each 1°C that the temperature rises.

●Block diagram

BU2302 / F



BU2305 / F



●Pin descriptions

BU2302/F

Pin No.	Pin Name	Function
1 2 3	OSC1 OSC2 OSC3	CR connection pins for oscillation; one or two oscillators can be used.
4	GND	Power supply pin (GND)
5	TESTB	LOW state is the test mode. In normal operation, this pin should be set to HIGH. This pin contains a pull-up resistance.
6	SET	Reset when LOW. When HIGH, oscillation begins, output is turned on, the timer is activated, output is turned off, and oscillation stops. This pin contains a pull-up resistance.
7	OUT	Nch open drain output
8	V_{DD}	Power supply pin (V_{DD})

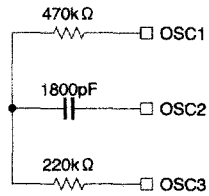
BU2305/F

Pin No.	Pin Name	Function
1 2 3	OSC1 OSC2 OSC3	CR connection pins for oscillation; one or two oscillators can be used.
4	GND	Power supply pin (GND)
5 6	RESETB SETB	See table below
7	OUT	Nch open drain output
8	V_{DD}	Power supply pin (V_{DD})

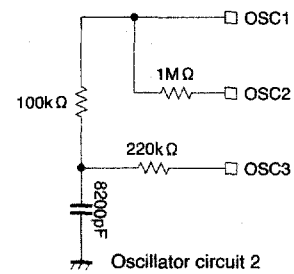
RESETB	SETB	Operating state
L	L	* Test mode The IC is not reset. Output is uncertain.
L	H	* Initial reset The IC is reset internally. This must always be done when the power supply is turned on.
H	L	* Set and reset operation Set and reset operations are repeated each time the SETB pin goes LOW. If the SETB pin is held LOW with the output on, the output remains on after the timer is activated, and oscillation does not stop.
H	H	* Operating and standby states The timer is activated, the output is turned off, and oscillation stops.

* The RESETB and SETB pins are equipped with a pull-up resistance.

●CR oscillator circuits



Oscillator circuit 1



Oscillator circuit 2

●Electrical characteristics

BU2302/F (Unless otherwise noted, Ta=25℃, V_{CC}=3.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating power supply voltage	V_{DD}	1.8	3.0	6.0	V	
Quiescent current consumption	I_{QD}	—	—	0.5	μA	OSC is stopped
Operating current consumption	I_{DD}	—	—	0.2	mA	When circuit 2 is used
SET pin rise time (Pin 6)	t_{SR}	—	—	50	ms	
Output pin rise time (Pin 7)	t_{or}	1.0	—	2.4	μs	R_O=10kΩ, C_O=50pF
LOW output current (Pin 7)	I_{OL}	5.0	—	—	mA	V_{OL}=3.0V
LOW output current (Pin 7)	I_{OL}	3.2	—	—	mA	V_{OL}=0.4V
Output leakage current	I_L	—	—	±0.1	μA	V_O=0~3.0V
LOW output current (Pins 2, 3)	I_{OL}	0.3	—	—	mA	V_{OL}=0.4V
HIGH output current (Pins 2, 3)	I_{OH}	—	—	−0.1	mA	V_{OH}=2.6V
LOW output current (Pins 1 ~ 3)	I_{IL}	—	—	±0.1	μA	
HIGH output current (Pins 1 ~ 3)	I_{IH}	—	—	±0.1	μA	
LOW output current (Pins 5, 6)	I_{IL}	—	—	20	μA	V_{IL}=0V
HIGH output current (Pins 5, 6)	I_{IH}	—	—	±0.1	μA	V_{IH}=3V
LOW input voltage (Pins 1 ~ 3, 5, 6)	V_{IL}	0.0	—	0.6	V	
HIGH input voltage (Pins 1 ~ 3, 5, 6)	V_{IH}	2.4	—	3.0	V	
Oscillation frequency	f_{OFC}	—	1.17	—	kHz	Circuit 2, V_{DD}=2V
Oscillation frequency characteristic	$\triangle f_{OFC}$	—	10	—	%	V_{DD}=2V, Ta=−10~60℃

* The value for the oscillation frequency characteristic is the value for the IC as a stand-alone unit, using oscillator circuit 2.

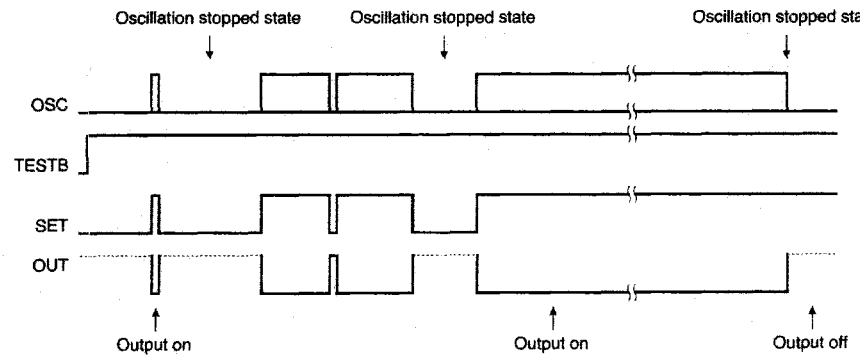
BU2305/F (Unless otherwise noted, Ta=25℃, V_{DD}=3.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating power supply voltage	V_{DD}	1.8	3.0	6.0	V	
Quiescent current consumption	I_{QD}	—	—	0.5	μA	OSC is stopped
Operating current consumption	I_{DD}	—	—	0.2	mA	When oseillation circuit 2 is used
Output pin rise time (Pin 7)	t_{or}	1.0	—	2.4	μSec	R_O=10kΩ, C_O=50pF
Output current (Pin 7)	I_{OL}	3.2	—	—	mA	V_{OL}=0.4V
Output leakage current	I_L	—	—	±0.1	μA	V_O=0~3.0V
Output current (Pins 2, 3)	I_{OL}	0.3	—	—	mA	V_{OL}=0.4V
Output current (Pins 2, 3)	I_{OH}	—	—	−0.1	mA	V_{OH}=+2.6V
LOW input current (Pins 1 ~ 3)	I_{IL}	—	—	±0.1	μA	
HIGH input current (Pins 1 ~ 3)	I_{IH}	—	—	±0.1	μA	
LOW input current (Pins 5, 6)	I_{IL}	—	—	20	μA	V_{IL}=0V
HIGH input current (Pins 5, 6)	I_{IH}	—	—	±0.1	μA	V_{IH}=3V
LOW input voltage (Pins 1 ~ 3, 5, 6)	V_{IL}	0.0	—	−0.6	V	
HIGH input voltage (Pins 1 ~ 3, 5, 6)	V_{IH}	2.4	—	3.0	V	
Oscillation frequency	fosc	—	1.08	—	kHz	Circuit 2, V_{DD}=2V
Oscillation frequency characteristic	△fosc	—	10	—	%	V_{DD}=2V, Ta=−10~60℃

* The value for the oscillation frequency characteristic is the value for the IC as a stand-alone unit, using oscillator circuit 2.

●Timing charts

BU2302 / F



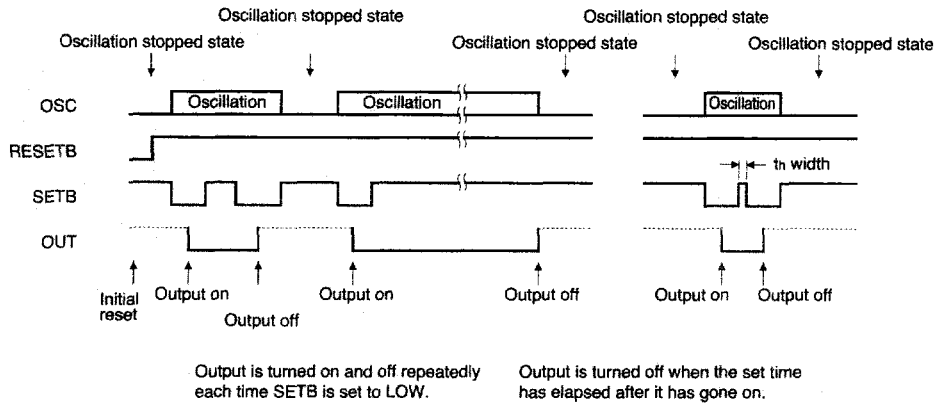
*1 A reset is carried out whenever the IC internal counter and OUT pin are set to the LOW level.

*2 The output is set to OFF about 4,190,000 clock pulses (OSC3 pin) from when it goes on (the SET pin goes HIGH).

*3 The relationship between the timer set time (t) and the oscillation frequency [fosc (Hz)] is as follows:

$$T=\frac{1}{60\times fosc}\times 2^{22}\fallingdotseq\frac{69905}{fosc}\ (min.)$$

BU2305/F



*1 When the LOW level has been on for period tS after the SETB falling edge is detected, OUT changes. (tS: See "Precautions regarding use".)

*2 The timer set time is equal to about 4,190,000 lock pulses from the oscillation circuit. The relationship between the timer set time [T (min)] and the oscillation frequency [fosc (Hz)] is shown below.

$$T = \frac{1}{60 \times fosc} \times 2^{22} \fallingdotseq \frac{69905}{fosc} \text{ (min.)}$$

*3 Initial reset: Always make sure an initial reset is carried out after the power supply is turned on. Please be aware that the initial reset does not engage when RESETB and SETB are both LOW.

*4 th width: About 20 pulses of the oscillation frequency can be removed as chattering, but if the th width exceeds 20 pulses, it cannot be removed as chattering, and the output will be changed.

●Circuit operation

CR oscillator circuit

1. Operation principle

The BU2302/05 use a stable multivibrator CR oscillation circuit. The three stages of the oscillation circuit are composed of a circuit structure which includes a negative feedback loop after a positive feedback loop, as shown in Figure 1.

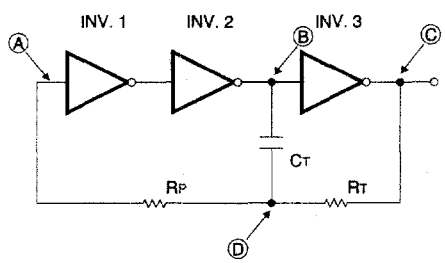


Fig.1

Immediately after the power supply is turned on, the electrical charge on capacitor C is 0. Consequently, the potential at Ⓓ is V_{SS}, and the potential at Ⓐ, Ⓑ, and Ⓒ is V_{SS}, V_{SS}, and V_{DD}, respectively. The third gate charges the capacitor C through the resistance R, and as this happens, the potential at point Ⓓ increases. When the threshold voltage of the first gate is exceeded, all of the gates are inverted.

Thus, the potential at Ⓓ is $V_{TH} + V_{SS}$, and the potential at Ⓒ is V_{SS}. Consequently, the electrical charge on capacitor C is discharged through the resistance R. When the potential at Ⓓ exceeds the threshold voltage of the first gate, each gate is inverted again. As a result, the potential at Ⓓ is $V_{TH} - V_{DD}$, and at Ⓒ is V_{DD}. Capacitor C begins to recharge. Oscillation is maintained by repeating the above operation.

1-1. How the input protection resistor (R_P) works

In the oscillator a voltage exceeding the rated value is applied to the first input. The CMOS IC may be damaged by the input current flowing as a result of this excessive voltage. To avoid excessive current, an input protection resistor (R_P) must be used.

However, if the value of the input protection resistor is too large, noise may appear in the resistor, causing chattering during the output inversion.

Conversely, if the value of the resistor is too small, it will not protect the input from excessive current flow.

Note also that the current flowing into the IC input protection circuit may change the oscillation frequency if the IC is switched.

An appropriate value for the input protection resistance is 10k ~ 500kΩ.

1-2. Design guidelines

The following formula shows how to determine the oscillation period T for the third oscillator.

(However, this formula assumes that when $R_P \geqq 2R_T$, the current flowing to R_P can be ignored.)

$$T = -CR_T \left[\ell n \left(\frac{V_{TH}}{V_{DD} + V_{TH}}\right) + \ell n \left(\frac{V_{DD} - V_{TH}}{2V_{DD} - V_{TH}}\right)\right] \quad \cdots (1)$$

Here, if $V_{TH} = 1/2\ V_{DD}$, the oscillation period T will be as shown in equation (2). Consequently, the oscillation frequency f_{OSC} will be expressed as the inverse of the oscillation period T.

$$t = 2.2\ CR_T = 1/f_{OSC},\ f_{OSC} = 1/2.2\ CR_T \quad \cdots (2)$$

However, if R_T is made too small, the CMOS output current is saturated and the oscillation frequency is less than the calculated value. It is better to use a larger resistance.

An appropriate value would be $RT \geqq 200k\Omega$.

This IC includes a CR oscillator and a 23-bit counter. The counter is composed of a binary counter which uses 22 bits.

The relation between the timer set period and the oscillation frequency is as follows :

$$\text{Set time (min) } T = \frac{1}{60 \times f_{OSC}} \times 2^{22}$$

$$= \frac{2^{22}}{4 \times 15 \times f_{OSC}} = \frac{2^{20}}{15 \times f_{OSC}}$$

Equations (1) and (2) are calculated based on a number of assumptions, and the frequency changes depending on the actual IC and the CR constant, so the value should be determined based on experimentation. Also, when determining the precision, adjust R_T using a semi-fixed resistance.

As an example, the oscillation circuit constant for a T = 60 minute timer would be as follows :

$$f_{OSC} = \frac{2^{20}}{15 \times T} = \frac{1048576}{900} = 1.165\ (kHz)$$

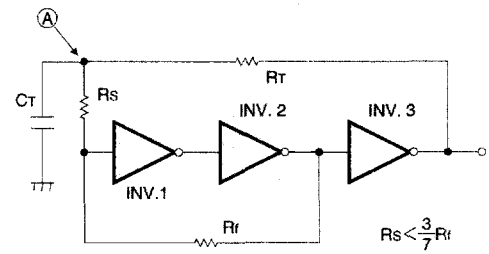
$$C_T = \frac{1}{2.2 \times f_{OSC} \times R_T} \quad (RT \text{ is set to } 220k\Omega)$$

$$= 1773\ (pF) \fallingdotseq 1800\ (pF)$$

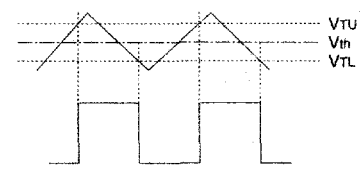
Thus, T = 60 minutes, R_T = 220 (kΩ), and C_T = 1800 (pF).

1-3. Oscillator circuit 2

In the oscillation circuit described in 1-1, the maximum amplitude of the oscillation level at point D is 2 V_{DD}, which may result in noise being induced in other circuits in the system. In such cases, the oscillation circuit can be changed to a Schmitt trigger type.



(A)



(B)

Fig.2

The Schmitt trigger circuit is composed of the INV. 1, INV. 2, and the resistors R_f and R_S shown in Figure 2. As shown in Figure 2 (B), the high level circuit threshold voltage V_{TU} and the low level circuit threshold voltage V_{TL} cause inversion and result in the rise of the output voltage V of INV. 2. As a result, the output voltage V_{OUT} is raised at point A and operation is stabilized through the feedback resistance R_f.

The circuit threshold voltages V_{TU} and V_{TL} of the Schmitt trigger circuit are given by the following equations :

$$V_{TU} = \left[\frac{R_S + R_f}{R_f}\right] V_{th} \cdots\cdots (2\cdot1)$$

$$V_{TL} = V_{DD} - \frac{R_S + R_f}{R_f} [V_{DD} - V_{th}]$$

$$= \left[\frac{R_S + R_f}{R_f}\right] \left[V_{th} - \frac{R_S}{R_S + R_f} V_{DD}\right] \cdots (2\cdot2)$$

The relationship between the Schmitt trigger circuit input voltage and the circuit threshold value voltage is as follows :

$$V_{DD} > V_{TU},\ V_{DD} > \left[\frac{R_S + R_f}{R_f}\right] V_{th} \cdots\cdots (2\cdot3)$$

$$0 < V_{th},\ 0 < \left[\frac{R_S + R_f}{R_S}\right] \left[V_{th} - \frac{R_S}{R_S + R_f} V_{DD}\right] \cdots (2\cdot4)$$

The circuit threshold value voltage V_{th} at its maximum is $V_{th} = 0.7\ V_{DD}$. When this value is substituted in the equation for VDD (equation 2·3), the following is obtained :

$$V_{DD} > \left[\frac{R_S + R_f}{R_f}\right] \times 0.7V_{DD} \quad ※V_{th} = 0.3 \sim 0.7V_{DD}$$

and it follows that $\therefore R_S < 3/7R_f \cdots\cdots (2\cdot5)$

In other words, the input resistance R_S must be less than 3 / 7 of the feedback resistance R_f. When this equation is not fulfilled, the dispersion of the CMOS inverter INV. 1 circuit threshold voltage V_{th} may result in the circuit not operating.

The equation for obtaining the oscillation frequency f_{OSC} of the CR oscillation circuit which uses the Schmitt trigger hysteresis characteristics is given by the following.

$$f_{OSC} = \frac{1}{-C_T R_T \left[\ell n \left(\frac{V_{TL}}{V_{TU}}\right) + \ell n \left(\frac{V_{DD} - V_{TU}}{V_{DD} - V_{TL}}\right)\right]}$$

The circuit threshold voltage V_{th} is 1 / 2 V_{DD} for standard values, but the actual distribution is 40 to 60% V_{DD}. In CMOS logic, in general, the dispersion is in the range of 30 to 70%.

Comparing oscillation circuits 1 and 2, the oscillation frequency equations clearly show that oscillation circuit 1 has a low dependency on the power supply voltage. However, please be aware that the hysteresis characteristics change as the power supply voltage changes, and this directly changes the oscillation frequency of oscillation circuit 2.

1-4. Oscillating elements

The capacitor C_T, which determines the oscillation frequency, can be an inexpensive ceramic capacitor if absolute precision of the timer is not required. However, use of a semiconductor capacitor with good temperature characteristics is recommended. If ceramic capacitors are not used, a film capacitor with a negative temperature coefficient such as a styrole capacitor can be used.

1-5. Preventing abnormal oscillation

To prevent abnormal oscillation, be careful to avoid applications in which Pins 1 and 3 are connected in a capacitive connection.

●Circuit operation

2. Timer output circuit

The timer output is through the N channel open drain, as shown in Figure 3. A PNP transistor with a small input-to-output voltage differential is used as the power supply switching element. The current drawn from the Pin 7 output is the sum of the base current I_B and the current which flows to R_2. The output leakage current I_L of this IC is very low, at ±0.1 (μA). Thus, the range of R_2 values can be calculated from $R_2 < V_{BE} / I_L$. During actual use, however, the value should always be less than 100 (kΩ). (When considering I_B, in consideration of the h_{FE} dispersion and temperature characteristics, assume that I_B is 2 to 3 times larger than it actually is.) R_1 is determined by V_{DD} and V_{BE}, and is set as follows :

$$R_1 \leqq (V_{DD} - V_{BE}) \cdot \frac{h_{FE}}{I_{CC}} \quad \cdots\cdots (1-1)$$

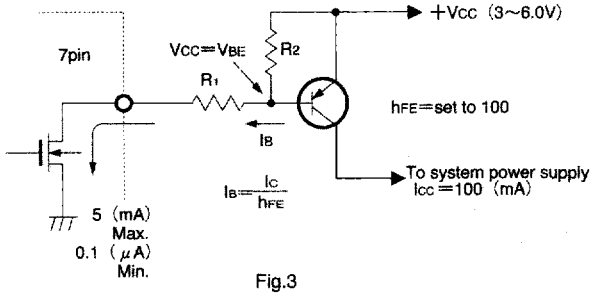


Fig.3

As an example, assume that V_{CC} = 3.0 (V), h_{FE} of the transistor = 100, I_{CC} = 100 (mA), V_{BE} = 0.5 (V), and R_2 = 22 (kΩ).

$$R_1 \leqq (V_{DD} - V_{BE}) \times \frac{h_{FE}}{I_{CC}}$$

$$= 2.5 \times \frac{100}{100 \times 10^{-3}}$$

$$= 2.5 \text{ (k}\Omega\text{) max.}$$

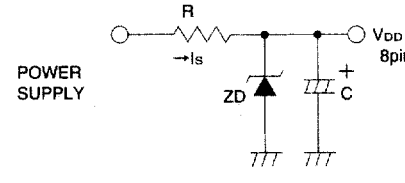
In practice, use a 2.2 (kΩ) transistor to assure that there is plenty of margin.

3. Chattering prevention circuit (BU2305)

The mechanical connections to a switch (lock or momentary type) that is used to start the timer create a short period of spurious output after it goes from off to on. This is referred to as chattering at the junction. Inputting such signals as a digital signal results in many pulses where only one should exist. Thus, a circuit to prevent chattering is necessary. Although there are a number of methods, this IC takes 32 periods from the oscillation frequency counter circuit as a clock pulse. Using this period, which is longer than the chattering period, chattering is eliminated by using a D flip-flop shift register. For switches used in a set, either a lock or a momentary switch may be used.

4. Operating voltage

When using this IC near its maximum power supply voltage, the voltage must be prevented from exceeding the maximum rated voltage when the power supply is turned on or off, or when power supply ripples or noise are present. A preventative Zener diode can be added to the power supply line as a way to circumvent this problem.



The circuit in Figure 4 is called a Zener shunt circuit. The current control R must follow the power supply current and be kept at a value higher than the allowable dissipation for the Zener diode. The value of the electrolytic capacitor for the shunt must be selected with consideration of the power supply current peak value and the pulse width.

The following may be used as a guideline :

R : in the range of 100 to several kΩ

C : in the range of 10 to 100 (μF)

●Operation notes

BU2302/F

・Initial reset

An initial reset must always be carried out when the power supply is turned on. The initial reset is done by setting TESTB to HIGH and SET to LOW.

・Set pin (SET)

When the power supply is turned on, make sure SET is in LOW state, so that an initial reset will be carried out. Then set the pin to HIGH before turning on the output.

BU2305/F

・Initial reset

An initial reset must always be carried out when the power supply is turned on. The initial reset is done by setting RESETB to LOW and SETB to LOW.

・Set pin (SETB)

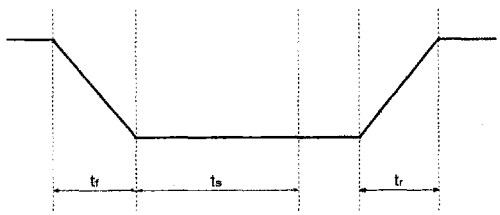
The chattering prevention circuit connected to the set pin (SETB) consists of a differential circuit (D-FF). To synchronize the OSC Pin 3 oscillation clock with the timed period, the restrictions shown below must be observed.

* Set pin (SETB) operating waveform

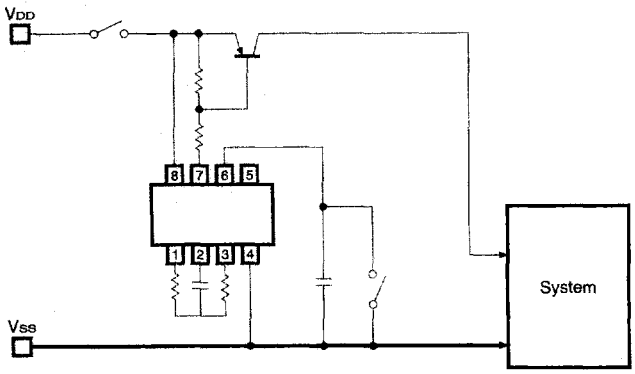
$t_f \leqq \frac{20}{fosc}$ (S)

$t_s \geqq \frac{40}{fosc}$ (S)

$t_r \geqq \frac{20}{fosc}$ (S)



●Application example



●Measurement data

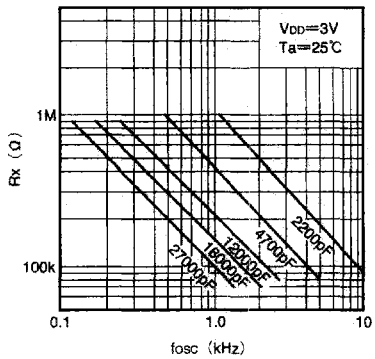


Fig. 5 Rx vs. oscillation frequency characteristic (oscillator circuit 1)

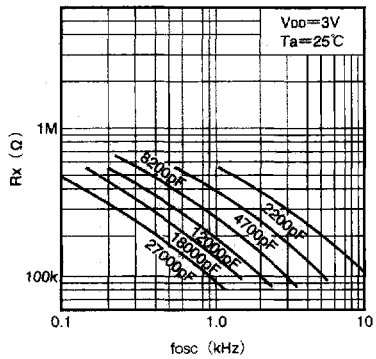


Fig. 6 Rx vs. oscillation frequency characteristic (oscillator circuit 2)

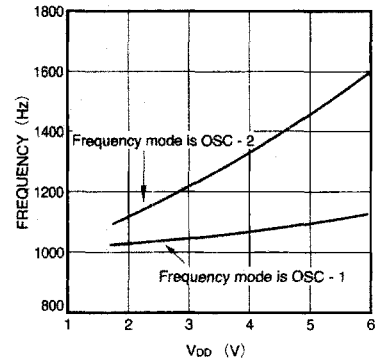


Fig. 7 Oscillation frequency - power supply voltage characteristic

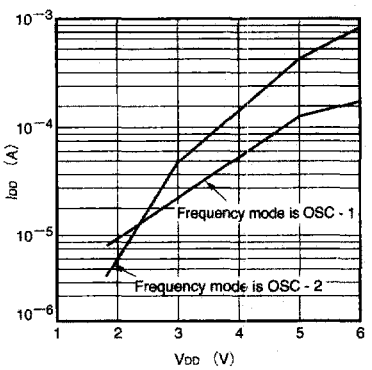


Fig. 8 Current consumption - power supply voltage characteristic

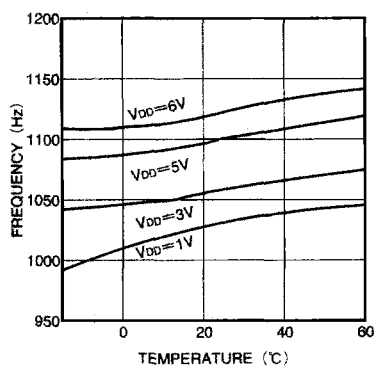


Fig. 9 Oscillation frequency - temperature characteristic (circuit 1)

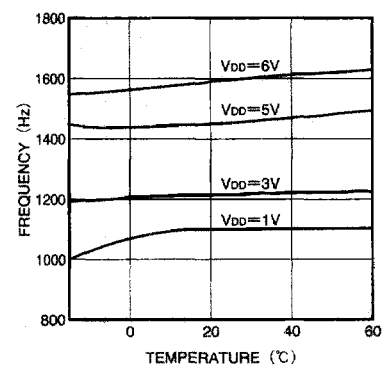


Fig. 10 Oscillation frequency - temperature characteristic (circuit 2)

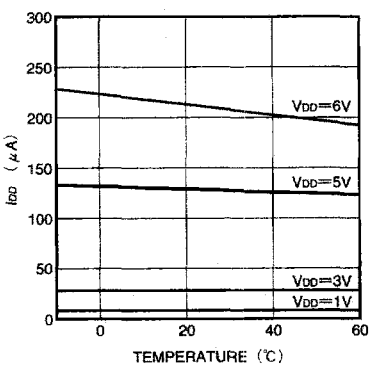


Fig. 11 Current consumption - temperature characteristic (circuit 1)

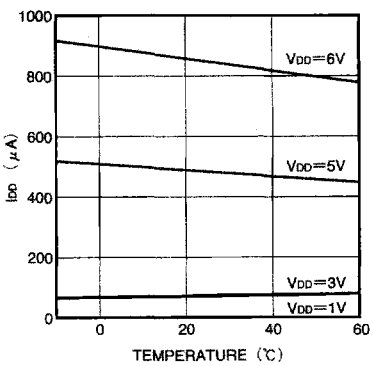


Fig. 12 Current consumption - temperature characteristic (circuit 2)

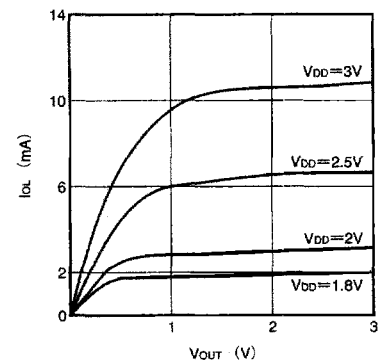


Fig. 13 Output voltage - output current characteristic

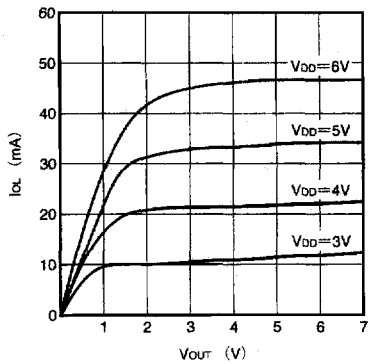


Fig. 14 Output voltage - output current characteristic

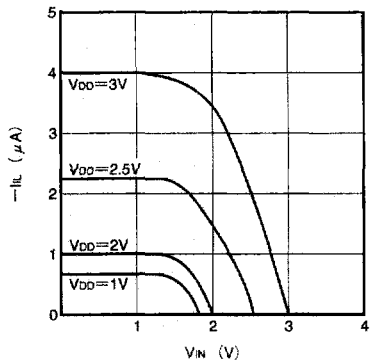


Fig. 15 RESETB and SETB pins: pull-up resistance characteristic

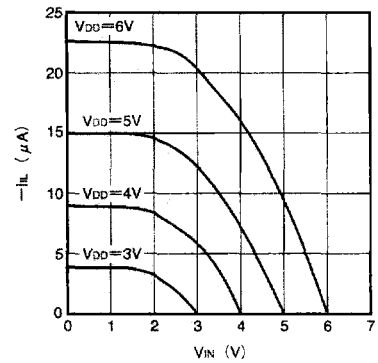
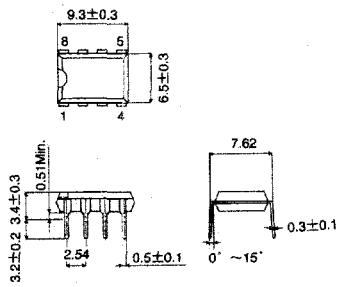


Fig. 16 RESETB and SETB pins: pull-up resistance characteristic

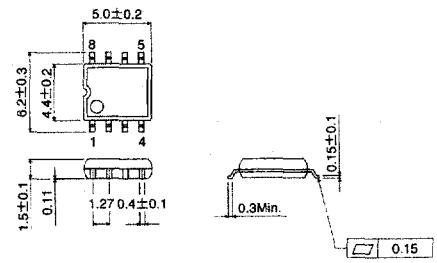
●External dimensions (Units: mm)

BU2302/BU2305



DIP8

BU2302F/BU2305F



SOP8