# Am90CL257

Low-Power 256K x 1 CMOS Static Column Mode DRAM



## OVERVIEW

The 256K x 1 CMOS Low-Power ('L') DRAM versions share common functional descriptions, DC and AC characteristics with the corresponding standard CMOS (non-'L') versions. The only additions to these sections are:

## DISTINCTIVE CHARACTERISTICS

- Extended refresh period
  — 32 ms (Max.) during standby
- Low data retention current
  — 230 μA (Max.)
- Low-power dissipation
  — 0.55 mW (Max.)

## ORDERING INFORMATION

The Ordering Information for the Low-Power DRAM versions are the same as for the Standard CMOS DRAMs, with the exception of an 'L' inserted within the device number to denote 'Low-Power.' For example, the Am90CL255 is = a 256K x 1 CMOS "Low-Power" Nibble Mode DRAM. All temperature ranges, speed and package options remain the same as those listed in Ordering Information sections for the respective Standard CMOS DRAMs.

## DC CHARACTERISTICS

The low-power version DRAMs are screened for one additional parameter, viz, CMOS standby current. All other DC characteristics remain the same for both families.

| Parameter Symbol | Parameter Description | Test Conditions | | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{CC6}$ | $V_{CC}$ Supply Current CMOS Standby | $\overline{RAS} \geq V_{CC} - 0.5$ V and $\overline{CAS}$ at $V_{IH}$, all other inputs and outputs $\geq V_{SS}$ | Am90CL257 | | 0.1 | mA |

The Am90CL257-15 is screened for $I_{CC1}$ = 55 mA, $I_{CC3}$ = 55 mA, and $I_{CC4}$ = 55 mA.

## AC CHARACTERISTICS

AC Characteristics remain unchanged on the low-power 100 ns and 120 ns versions. The AC characteristics corresponding to the 150 ns speed are on the following page.

## FUNCTIONAL DESCRIPTION

The Functional Descriptions for low-power versions are the same as the corresponding standard versions. The low-power devices, however, support Extended Refresh cycles described below:

### Extended Refresh Cycle

All low-power versions extend the Refresh Cycle period to 32 ms for $\overline{RAS}$-Only Refresh cycles. This feature reduces the total current consumption to a maximum of 230 μA for data retention. The low-standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC})\ (I_{ACTIVE}) + (t_{RI} - t_{RC})\ (I_{STANDBY})}{T_{RI}}$$

where $t_{RC}$ = Refresh Cycle Time

and $t_{RI}$ = Refresh Interval Time or $t_{REF}/256$

Before entering or leaving an Extended Refresh period, the entire array must be refreshed at the normal interval of 4 ms. This can be accomplished by either a burst or distributed refresh.



Publication # 07412 | Rev. A | Amendment /0
Issue Date: May 1986

## SWITCHING CHARACTERISTICS ($T_A$ = 0 to +70°C, $V_{CC}$ = 5 V ±10%, $V_{SS}$ = 0 V unless otherwise noted)

| No. | Parameter Symbol | Parameter Description | Am90CL257-15 Min. | Am90CL257-15 Max. | Units |
|---|---|---|---|---|---|
| **READ/WRITE/READ-MODIFY-WRITE AND REFRESH CYCLES** | | | | | |
| 1 | $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 150 | 75,000 | ns |
| 2 | $t_{RC}$ | Random R/W Cycle Time | 245 | | ns |
| 3 | $t_{RP}$ | $\overline{RAS}$ Precharge Time | 85 | | ns |
| 4 | $t_{CSH}$* | $\overline{CS}$ Hold Time | 150 | | ns |
| 5 | $t_{WRP}$ | Write-to-$\overline{RAS}$ Precharge Time | 0 | | ns |
| 6 | $t_{ASR}$ | Row Address Setup Time | 0 | | ns |
| 7 | $t_{RAH}$ | Row Address Hold Time | 15 | | ns |
| 8 | $t_{AR}$ | Column Address Hold Time from $\overline{RAS}$ | 130 | | ns |
| 9 | $t_{RHZ}$ | $\overline{RAS}$-to-Output High Impedance (Note 1) | | 20 | ns |
| 10 | $t_{RLZ}$ | $\overline{RAS}$-to-Output Low Impedance (Note 1) | 30 | | ns |
| 11 | $t_{HZ}$* | $\overline{CS}$-to-Output High Impedance (Notes 1 & 2) | | 25 | ns |
| 12 | $t_{LZ}$* | $\overline{CS}$-to-Output Low Impedance (Notes 1 & 2) | | | |
| 13 | $t_{REF}$ | Time Between Refresh | | 4 | ms |
| 14 | $t_T$ | Transition Time (Rise and Fall) (Note 3) | 3 | 50 | ns |
| **READ CYCLE** | | | | | |
| 15 | $t_{RAC}$ | Access Time From $\overline{RAS}$ (Notes 4 & 5) | | 150 | ns |
| 16 | $t_{CAC}$* | Access Time From $\overline{CS}$ (Note 5) | | 30 | ns |
| 17 | $t_{CAA}$ | Access Time from Column Address (Note 5) | | 65 | ns |
| 18 | $t_{CS}$ (R)* | $\overline{CS}$ Pulse Width (Read Cycle) | 30 | | ns |
| 19 | $t_{RSH}$ (R)* | $\overline{RAS}$ Hold Time (Read Cycle) | 10 | | ns |
| 20 | $t_{RCS}$* | Read Command Setup Time | 0 | | ns |
| 21 | $t_{CAR}$ | Column Address-to-$\overline{RAS}$ Setup Time | 65 | | ns |
| 22 | $t_{RCH}$* | Read Command Hold Time Referenced to $\overline{CS}$ | 0 | | ns |
| 23 | $t_{RRH}$ | Read Command Hold Time Referenced to $\overline{RAS}$ | 10 | | ns |
| 24 | $t_{ARH}$ | Column Address Hold Time Referenced to $\overline{RAS}$ | 0 | | ns |
| 25 | $t_{RAD}$ | $\overline{RAS}$-to-Column Address Delay Time (Note 6) | 20 | 85 | ns |
| 26 | $t_{CS}$ (W)* | $\overline{CS}$ Pulse Width (Write Cycle) | 30 | | ns |
| 27 | $t_{RSH}$ (W)* | $\overline{RAS}$ Hold Time (Write Cycle) | 30 | | ns |
| **WRITE CYCLE** | | | | | |
| 28 | $t_{WDR}$ | $\overline{RAS}$-to-Write Command Delay Time | 20 | | ns |
| 29 | $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 30 | | ns |
| 30 | $t_{CWL}$* | Write Command to $\overline{CS}$ Lead Time | 30 | | ns |
| 31 | $t_{WP}$ | Write Command Pulse Width | 30 | | ns |
| 32 | $t_{WCP}$ | Write Command Precharge Time | 10 | | ns |
| 33 | $t_{WCS}$* | Write Command Setup Time | 0 | | ns |
| 34 | $t_{WCH}$* | Write Command Hold Time | 30 | | ns |
| 35 | $t_{WCR}$ | Write Command Hold Time from $\overline{RAS}$ | 120 | | ns |
| 36 | $t_{AWS}$ | Column Address-to-Write Command Setup Time | 0 | | ns |
| 37 | $t_{AWH}$ | Column Address-to-Write Command Hold Time | 25 | | ns |
| 38 | $t_{DS}$ | Data-In Setup Time | 0 | | ns |
| 39 | $t_{DH}$ | Data-In Hold Time | 25 | | ns |
| 40 | $t_{OW}$ | Output Active from End of Write | 0 | | ns |

*This parameter not applicable if operated with $\overline{CS}$ grounded.
Notes: See next page for notes.

## SWITCHING CHARACTERISTICS

($T_A$ = 0 to +70°C, $V_{CC}$ = 5 V ±10%, $V_{SS}$ = 0 V unless otherwise noted)

| No. | Parameter Symbol | Parameter Description | Am90CL257-15 Min. | Am90CL257-15 Max. | Units |
|---|---|---|---|---|---|
| **READ-MODIFY-WRITE (RMW) CYCLE** | | | | | |
| 41 | $t_{RWC}$ | RMW Cycle Time | 280 | | ns |
| 42 | $t_{RRW}$ | RMW Cycle $\overline{RAS}$ Pulse Width | 185 | 75,000 | ns |
| 43 | $t_{CRW}$* | RMW Cycle $\overline{CS}$ Pulse Width | 65 | | ns |
| 44 | $t_{WRH}$ | $\overline{WE}$-to-$\overline{RAS}$ Hold Time | 5 | | ns |
| 45 | $t_{RWD}$ | $\overline{RAS}$-to-$\overline{WE}$ Delay Time (Note 7) | 150 | | ns |
| 46 | $t_{AWD}$ | Column Address-to-$\overline{WE}$ Delay Time (Note 7) | 75 | | ns |
| 47 | $t_{CWD}$ | $\overline{CS}$-to-$\overline{WE}$ Delay Time (Note 7) | 30 | | ns |
| **STATIC COLUMN MODE CYCLE** | | | | | |
| 48 | $t_{OHA}$ | Output Hold Time from Address Change | 10 | | ns |
| 49 | $t_{OHW}$ | Output Hold Time from End of Write | 0 | | ns |
| 50 | $t_{WPA}$ | RMW Write Precharge Access Time | | 75 | ns |
| 51 | $t_{WRA}$ | RMW Write-Read Access Time | | 110 | ns |
| 52 | $t_{WPS}$ | RMW Write Command Precharge Time | 75 | | ns |

*This parameter not applicable if operated with $\overline{CS}$ grounded.

Notes:
1. Assumes three-state test load (5 pF and a 380 Ω Thevenin equivalent).
2. At any given temperature and voltage combination, $t_{HZ}$ (Max.) is less than $t_{LZ}$ (Min.) from device to device.
3. $t_T$ is measured between $V_{IH}$ (Min.) and $V_{IL}$ (Max.).
4. Assumes that $t_{RAD} \leq t_{RAD}$ (Max.). If $t_{RAD} > t_{RAD}$ (Max.), then $t_{RAC}$ will increase by the amount that $t_{RAD}$ exceeds to $t_{RAD}$ (Max.).
5. Load = 2 TTL loads and 100 pF.
6. $t_{RAD}$ specified for reference only.
7. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$ and $t_{AWD}$ are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an Early Write Cycle and the data-out pin will remain in high impedance for the duration of $\overline{WE}$. If $t_{WCD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), then the cycle is a Read-Modify-Write Cycle and the data-out will contain the data read from the selected address. If any of the above conditions are not satisfied, data-out is indeterminate.
8. Access time from a write command to a determined by the latter of $t_{CAA}$ or $t_{WPA}$ or $t_{WRA}$.

4