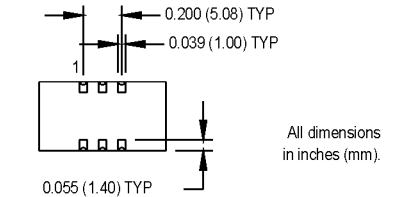
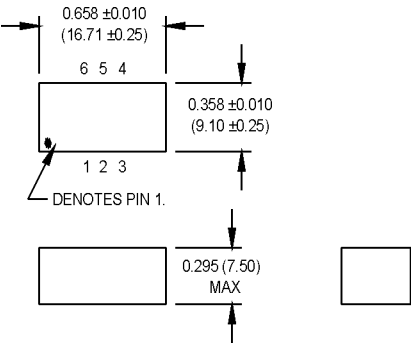


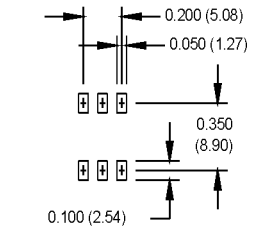
# M5003/M5004 Series High Precision FR-4 Based Surface Mount HPV CXO



- Excellent stability inclusive of all variations and 20 year life
- Ideal for SONENT, PCS base stations and reference clock applications



SUGGESTED SOLDER PAD LAYOUT



## Ordering Information

	M5003/M5004	2	0	R	1	P	K	00.0000 MHz
Product Series								
M5003 = 3.3 V								
M5004 = 5.0 V*								
Temperature Range								
1: 0°C to +70°C								
2: -40°C to +85°C								
6: -20°C to +70°C								
7: 0°C to +85°C								
Stability								
0: Nominal per APR selection								
Output Type								
R: Complementary tri-state (LVPECL/LVDS)								
T: Tri-state (LVCMOS)								
Absolute Pull Range (APR)								
1: ±25 ppm (±10 ppm typical stability)*								
2: ±15 ppm (±20 ppm typical stability)*								
Symmetry/Logic Compatibility								
D: 45/55% LVCMOS/TTL								
L: 45/55% LVDS								
P: 45/55% LVPECL								
Package/Lead Configurations								
K: FR-4, 6-Pad								
Frequency (customer specified)								

\* APR includes stability over temperature, initial tolerance, and aging. Contact the factory for 5.0 V availability.

## Pad Connections

PIN	FUNCTION
1	Control Voltage
2	Tri-state
3	Ground
4	Output 1
5	N/C or Output 2
6	+Vdd

M-tron reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of such product.

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Electrical Specifications	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
	Frequency Range	F	1 1		160 800	MHz MHz	LVC MOS LVPECL/LVDS
	Frequency Stability <sup>1</sup>	ΔF/F	(See Ordering Information)				
	Operating Temperature	T <sub>A</sub>	(See Ordering Information)				
	Input Voltage	V <sub>cc</sub> /V <sub>dd</sub>	3.0	3.3	3.6	VDC	LVC MOS/LVPECL/LVDS
	Input Current <sup>2</sup>	I <sub>cc</sub> /I <sub>dd</sub>	5 5 50		50 75 120	mA mA mA	LVC MOS LVDS LVPECL
	Symmetry (Duty Cycle)		(See Ordering Information)				
	Load		2 TTL or 15 pF Max. 50 Ohms to V <sub>cc</sub> -2 VDC 50 Ohm Differential Load				LVC MOS/TTL LVPECL LVDS
	Rise/Fall Time	Tr/Tf	2 0.25		10 3	ns ns	LVC MOS LVPECL/LVDS
	Logic “1” Level	Voh	2.5 2.2 1.375		2.4	VDC VDC VDC	LVC MOS LVPECL LVDS
	Logic “0” Level	Vol	1.4		0.5 1.7 1.125	VDC VDC VDC	LVC MOS LVPECL LVDS
	Phase Jitter	ϕ J			4	ps RMS	Integrated 12 kHz - 20 MHz Or 50 kHz to 80 MHz
	Phase Noise		-105 dBc/Hz at 10 kHz typ. at 622.080 MHz				LVPECL
	Aging				6	ppm	20 years
	Modulation Bandwidth	f <sub>m</sub>	10			kHz	-3 dB
	Control Voltage	V <sub>c</sub>	0.3		3.0	V	LVC MOS/LVPECL/LVDS
	Center Frequency	V <sub>c0</sub>		1.65		V	LVC MOS/LVPECL/LVDS
	Pullability	APR	(See Ordering Information)				Over control voltage
	Linearity				10	%	
	Tri-State Function		Logic Level “1” for enabled output(s) Logic Level “0” for disabled output(s)				
Environmental							
	Mechanical Shock	Per MIL-STD-202, Method 213, Condition E					
	Thermal Shock	Per MIL-STD-883, Method 1011, Condition A					
	Vibration	Per MIL-STD-883, Method 2007, Condition A					
	Reflow Solder Conditions	240°C for 10 s max.					

1. Stability includes initial tolerance, deviation over temperature, supply and load variation, and aging for 20 years @ 25°C.
2. Actual value of this parameter is frequency dependent.

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