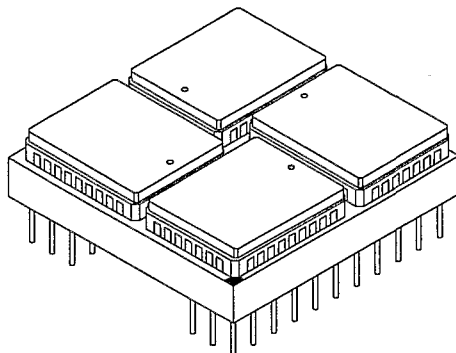


DESCRIPTION:

The DPE832V is a high-performance Electrically Erasable and Programmable Read Only Memory (EEPROM) module and may be organized as 8K X 32, 16K X 16 or 32K X 8.

The module is built with four low-power CMOS 8K X 8 EEPROMs. The four chip enables are used for individual BWDW* selection. The DPE832V is ideally suited for those computer systems having 16-bit or 32-bit architectures.

The DPE832V contains a 32-BWDW page register to allow writing of up to 32 BWDWs simultaneously. During a write cycle, the address and 1 to 32 BWDWs of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the module will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA Polling of the most significant data bit in each byte. Once the end of a write cycle has been detected, a new access for a read or write can begin.

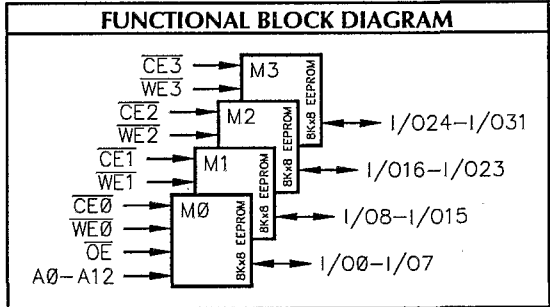


FEATURES:

- Fast Access Times: 55, 70, 90, 120, 150, 200, 250ns
- Automatic Page Write Operation
 - Internal Address and Data Latches
 - Internal Control Timer
- Fast Write Cycle Times
 - Page Write Cycle Time: 10ms maximum
 - 1 to 32 BWDW* Page Write Operation
- DATA Polling for END of Write Detection
- High Reliability CMOS Technology
 - Endurance: 10^4 Cycles
 - Data Retention: 10 years
- Single +5V Power Supply, $\pm 10\%$ Tolerance
- CMOS and TTL Compatible Inputs and Outputs
- Available with All Semiconductor Components used to Construct the Module Compliant to MIL-STD-883; Class B
- 66-Pin PGA (Grid Array) Package
- Same Package as other Versapac Versions (SRAMs, EPROMs, and Mixed)

* Byte, Word or Double Word (BWDW)

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0 - A12	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE0} - \overline{CE3}$	Chip Enables
$\overline{WE0} - \overline{WE3}$	Write Enables
\overline{OE}	Output Enable
V _{DD}	Power (+5V)
V _{SS}	Ground
N.C.	No Connect

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PIN-OUT DIAGRAM

1 I/O8	12 $\overline{WE1}$	23 I/O14			34 I/O24	45 VDD	56 I/O30
2 I/O9	13 $\overline{CE1}$	24 I/O13			35 I/O25	46 $\overline{CE3}$	57 I/O29
3 I/O10	14 VSS	25 I/O12			36 I/O26	47 $\overline{WE3}$	58 I/O28
4 N.C.	15 I/O15	26 I/O11			37 A6	48 I/O31	59 I/O27
5 N.C.	16 A10	27 \overline{OE}			38 A7	49 A3	60 A0
6 N.C.	17 A11	28 N.C.			39 N.C.	50 A4	61 A1
7 N.C.	18 A12	29 $\overline{WE0}$			40 A8	51 A5	62 A2
8 N.C.	19 VDD	30 I/O6			41 A9	52 $\overline{WE2}$	63 I/O22
9 I/O0	20 $\overline{CE0}$	31 I/O5			42 I/O16	53 $\overline{CE2}$	64 I/O21
10 I/O1	21 N.C.	32 I/O4			43 I/O17	54 VSS	65 I/O20
11 I/O2	22 I/O7	33 I/O3			44 I/O18	55 I/O23	66 I/O19

RECOMMENDED OPERATING RANGE ¹					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.3	V
V _{IL}	Input LOW Voltage	-0.1 ²		0.8	V

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-65 to +150	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.3 to +6.25	V
V _{I/O}	Input/Output Voltage ¹	-0.3 ² to +6.25	V

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Float	C _L	Parameters Measured
1	100 pF	except t _{DF}
2	5 pF	t _{DF}

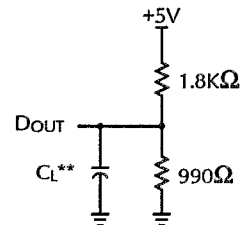
TRUTH TABLE				
Mode	CE	OE	WE	I/O PIN
Standby	H	X	X	HIGH-Z
Read	L	L	H	D _{OUT}
Write	L	H	L	D _{IN}
Write Inhibit	X	L	X	HIGH-Z
Write Inhibit	X	X	H	HIGH-Z

L = LOW H = HIGH X = Don't Care

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{CE}	Chip Enable	30	pF	V _{IN} = 0V
C _{ADR}	Address Input	70		
C _{WE}	Write Enable	70		
C _{OE}	Output Enable	70		
C _{I/O}	Data Input/Output	30		

Figure 1. Output Load

** Including Probe and Jig Capacitance.



DC OPERATING CHARACTERISTICS: Over the operating ranges.									
Symbol	Characteristics	Test Conditions	X 32		X 16		X 8		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	Operating Supply Current	CE = OE = V _{IL} , all I/O = 0mA f = t _{RC} Min.		320		170		90	mA
I _{SB1}	V _{DD} Current Standby (TTL)	CE = V _{IH}		12		12		12	mA
I _{SB2}	V _{DD} Current Standby (CMOS)	CE = V _{DD} - 0.3Vdc		1.0		1.0		1.0	mA
I _{IL}	Input Leakage Current	V _{IN} = V _{DD} Max.	-20	20	-20	20	-20	20	μA
I _{OL}	Output Leakage Current	V _{OUT} = V _{DD} Max.	-5	5	-10	10	-20	20	μA
V _{IL}	Input Voltage Low		-0.1	0.8	-0.1	0.8	-0.1	0.8	V
V _{IH}	Input Voltage High		2.0	V _{DD} +0.3	2.0	V _{DD} +0.3	2.0	V _{DD} +0.3	V
V _{OL}	Output Voltage Low	I _{OUT} = 2.1mA		0.45		0.45		0.45	V
V _{OH}	Output Voltage High	I _{OUT} = -400μA	2.4		2.4		2.4		V

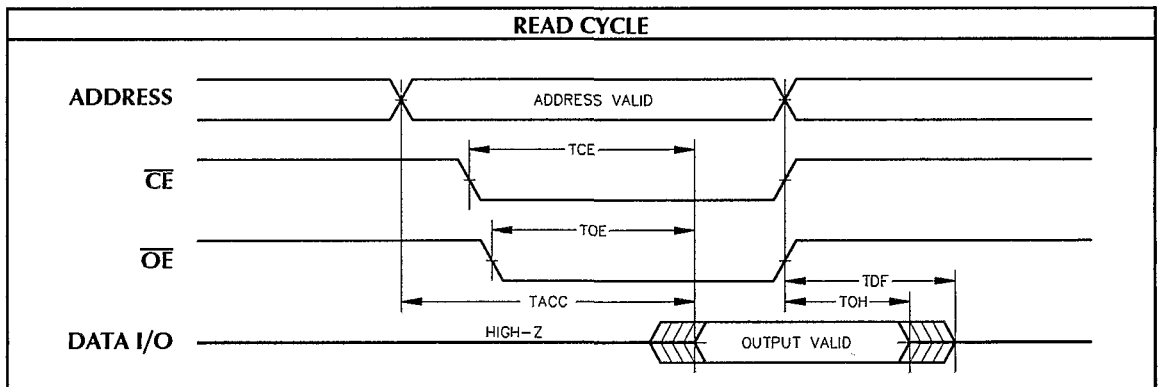


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges ^{6,7}											
No.	Symbol	Parameter	-55		-70		-90		-120		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{ACC}	Address to Output Valid		55		70		90		120	ns
2	t _{CE}	Chip Enable to Output Valid		55		70		90		120	ns
3	t _{OE}	Output Enable to Output Valid		30		35		40		50	ns
4	t _{DF}	Chip Enable or Output Enable to Output Float ⁴		30		35		40		50	ns
5	t _{OH}	Output Hold from Chip Enable, Output Enable, or Address, Whichever Occurs First	0		0		0		0		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges ^{6,7}									
No.	Symbol	Parameter	-150		-200		-250		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{ACC}	Address to Output Valid		150		200		250	ns
2	t _{CE}	Chip Enable to Output Valid		150		200		250	ns
3	t _{OE}	Output Enable to Output Valid		70		80		100	ns
4	t _{DF}	Chip Enable or Output Enable to Output Float ⁴		50		60		60	ns
5	t _{OH}	Output Hold from Chip Enable, Output Enable, or Address, Whichever Occurs First	0		0		0		ns

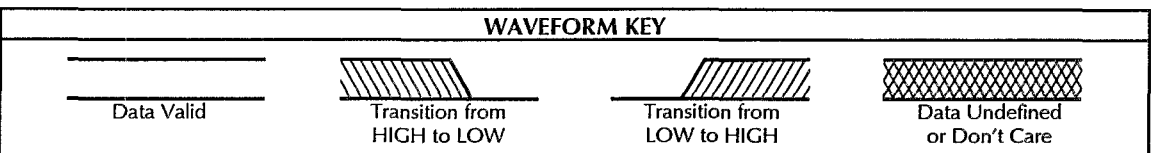
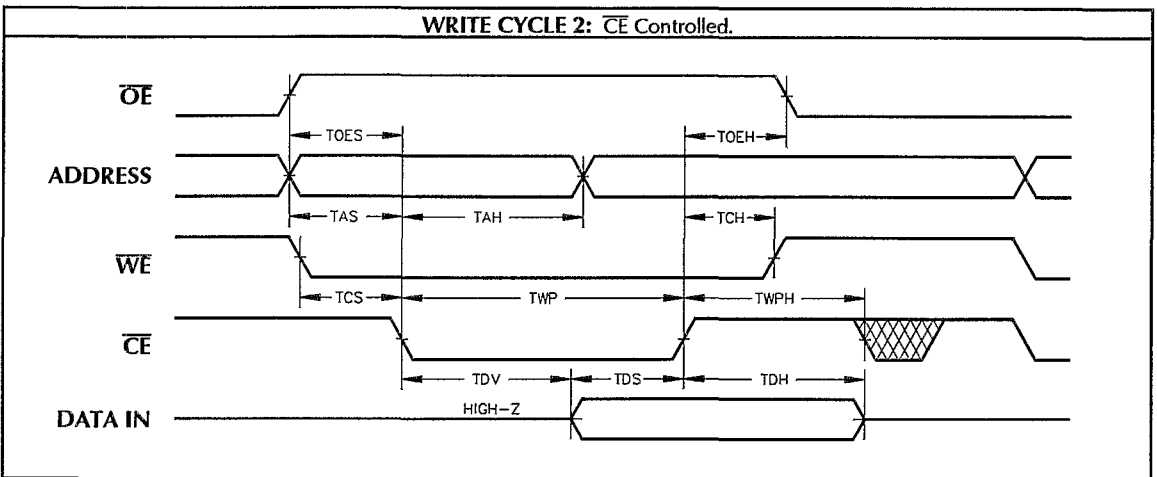
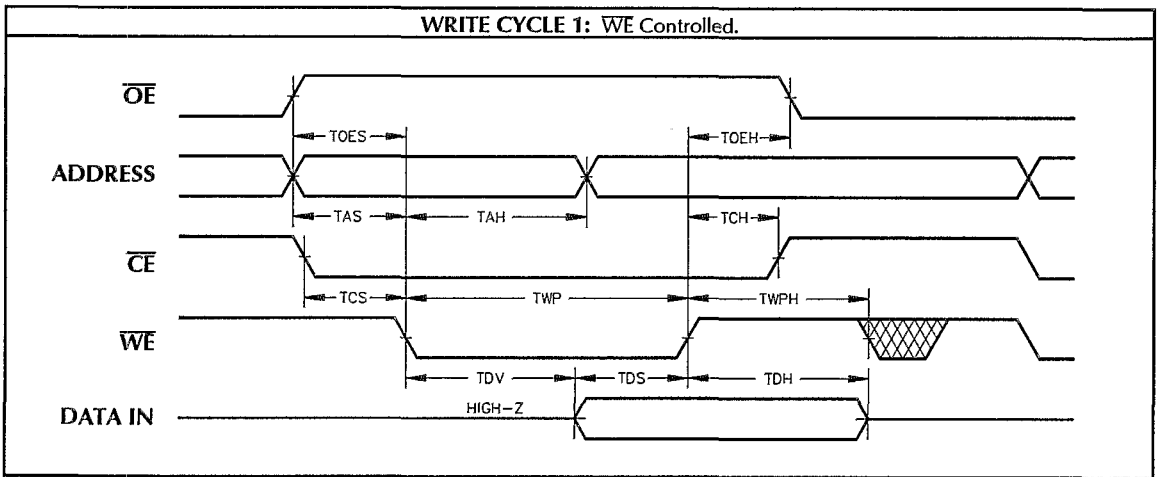
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges ^{6,7}						
No.	Symbol	Parameter	MIN.		MAX.	Unit
6	t _{WC}	Write Cycle Time			10	ms
7	t _{AS}	Address Set-up Time *	0			ns
8	t _{AH}	Address Hold Time	50			ns
9	t _{CS}	Chip Select Set-up Time	0			ns
10	t _{CH}	Chip Select Hold Time	0			ns
11	t _{WP}	Write Pulse Width (CE or OE)	100		1000	ns
12	t _{DS}	Data Set-up Time	50			ns
13	t _{DH}	Data Hold Time	0			ns
14	t _{DV}	Time to Data Valid			1	μs
15	t _{OES}	OE Setup Time	0			ns
16	t _{OEH}	OE Hold Time	0			ns
17	t _{WPH}	Write Pulse Width High	50			ns
18	t _{BLC}	Byte Load Cycle Time	150			ns
19	t _{PLW}	Page Load Width			150	μs

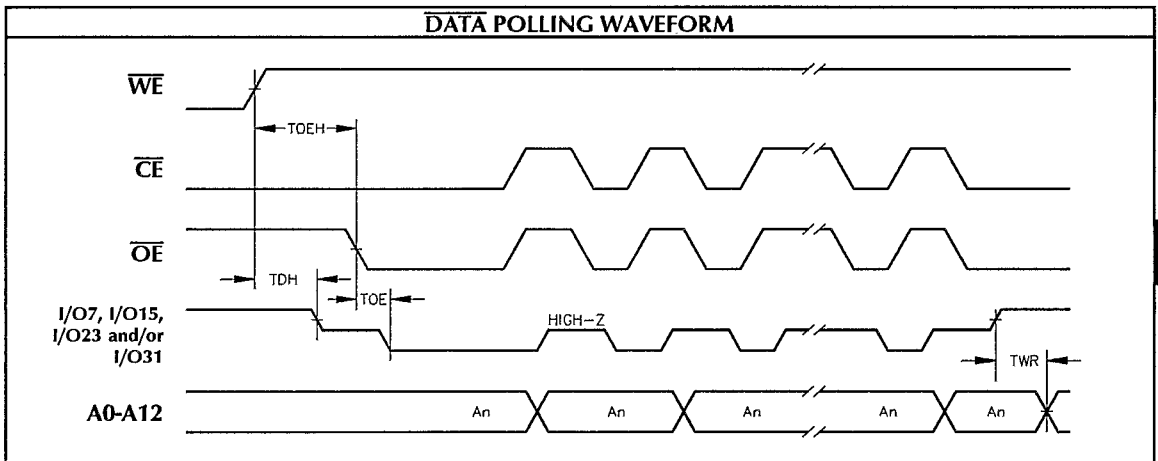
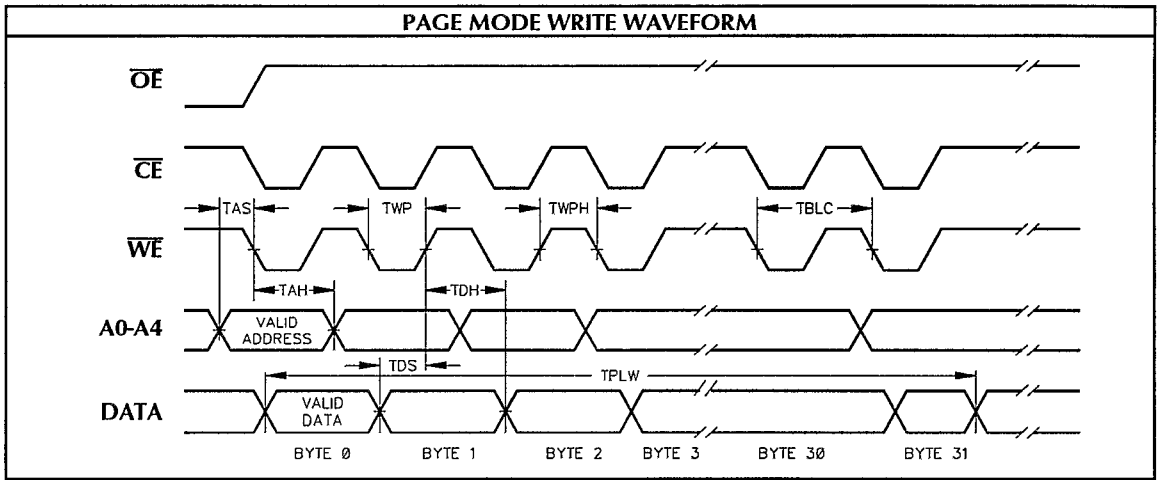
* Valid for both Read and Write Cycles.



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DEVICE OPERATION

READ: The DPE832V is accessed like a Static RAM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by address pins is asserted on the outputs. The outputs are put in the high impedance state whenever \overline{CE} or \overline{OE} is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high initiates a write cycle. The address is latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} . Once a BWDW* write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the DPE832V allows 1 to 32 BWDWs of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data BWDW has been loaded into the device, successive BWDWs may be loaded in the same manner. Each new BWDW to be written must have its high to low transition on \overline{WE} (or \overline{CE}) within 150µs

* Byte, Word or Double Word

of the low to high transition of \overline{WE} (or \overline{CE}) of the preceding BWDW. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A5 to A12 specify the page address. The page address must be valid during each high to low transition of \overline{WE} (or \overline{CE}). A0 to A4 are used to specify which BWDWs within the page are to be written. The BWDWs may be loaded in any order and may be changed within the same load period. Only BWDWs which are specified for writing will be written; unnecessary cycling of other BWDWs within the page does not occur.

DATA POLLING: The DPE832V features \overline{DATA} Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on $I/O7, I/O15, I/O23$ and/or $I/O31$. Once the the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. \overline{DATA} Polling may begin at any time during the write cycle.

ORDERING INFORMATION

DP E832 V - XXX X
 PREFIX DEVICE TYPE PACKAGE SPEED GRADE

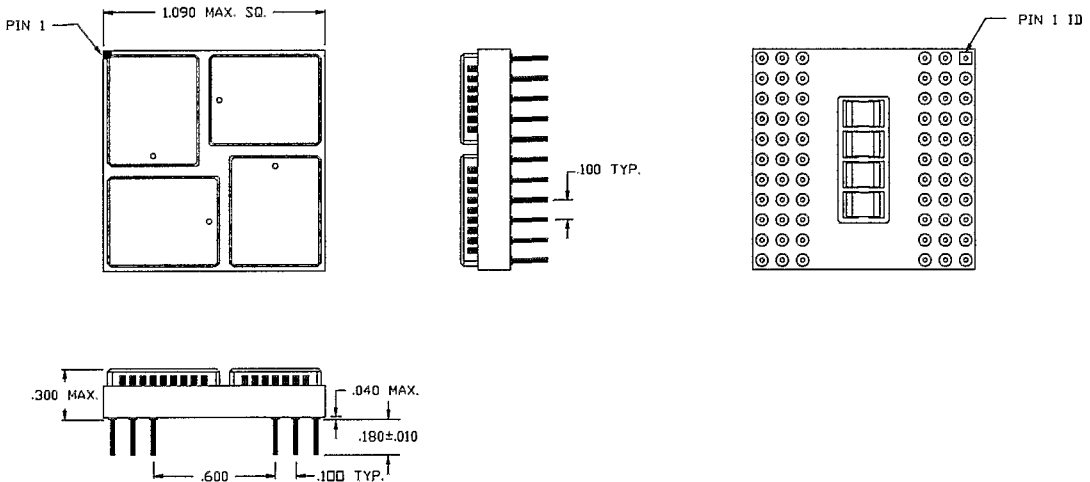
C COMMERCIAL 0°C to +70°C
 I INDUSTRIAL -40°C to +85°C
 M* MILITARY -55°C to +125°C
 B* MIL-PROCESSED -55°C to +125°C

55 55ns (COMMERCIAL ONLY)
 70 70ns
 90 90ns
 120 120ns
 150 150ns
 200 200ns
 250 250ns

V 66-PIN PGA VERSAPAC
 CMOS EEPROM 8Kx32, 16Kx16 OR 32Kx8

* B grade modules are constructed with 883 devices.

MECHANICAL DIAGRAMS



NOTES:

1. All voltages are with respect to V_{SS} .
2. -1.0V min. for pulse width less than 20ns (V_{IL} min. = -0.3V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of $\pm 500mV$ from steady state voltage.
6. When \overline{OE} and \overline{CE} are LOW and \overline{WE} is HIGH, I/O pins are in the output state; and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when \overline{WE} is LOW.

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