

# IH5110—IH5115

## General Purpose Sample & Hold



### GENERAL DESCRIPTION

Each of the 5110 family is a complete Sample and Hold circuit, (except for sampling capacitor) including input buffer amplifier, output buffer amplifier and CMOS switching logic. The devices are designed to operate from  $\pm 15V$  and  $+5V$  supplies. The input logic is designed to "Sample" and "Hold" from standard TTL logic levels.

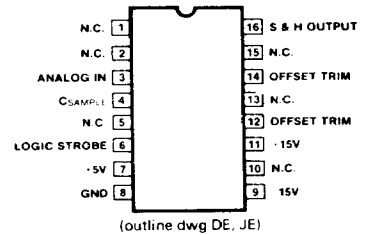
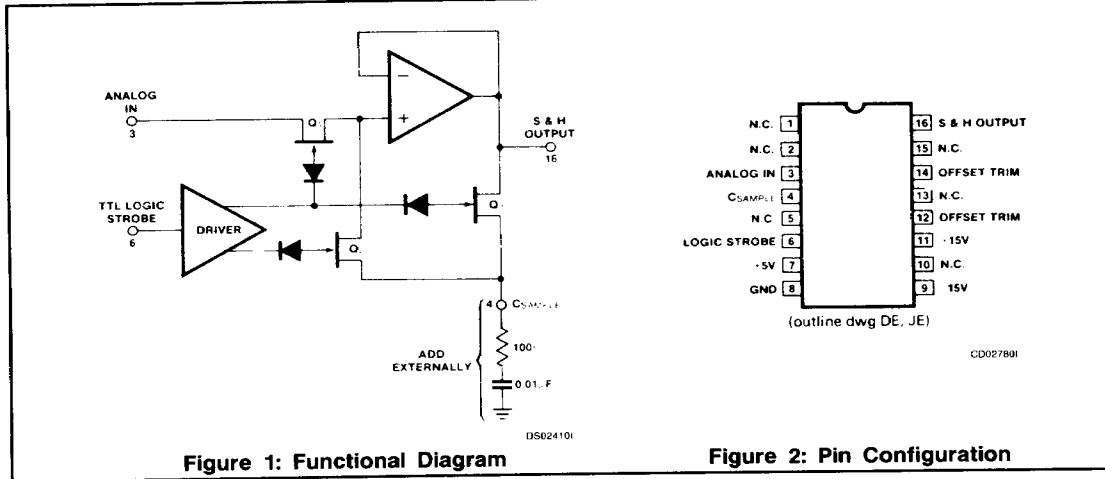
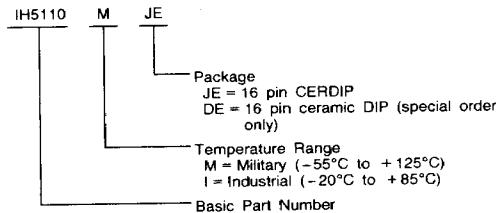
The design is such that the input and output buffering is performed with only one operational amplifier, by switching the sampling capacitor from the output back to input. Switches  $Q_1$ ,  $Q_2$ , and  $Q_3$  (see Figure 1) accomplish this switching. In the sampling mode  $Q_1$  and  $Q_3$  are shorted and  $Q_2$  is open; thus the op. amp. charges up the sampling capacitor. In the hold mode  $Q_1$  and  $Q_3$  are open and  $Q_2$  is shorted; thus the sampling cap. is switched back to the noninverting input of the op. amp.

This structure provides a very accurate d.c. gain of 1 with very fast settling times (i.e.  $5\mu s$ ). Additionally the design has internal feedback to cancel charge injection effects (sample to hold offsets).  $Q_1$  and  $Q_2$  are driven 180 degrees out of phase to accomplish this charge nulling.

### FEATURES

- Low Cost
- Military and Industrial Temperature Ranges
- $\pm 10V$  Input Voltage Range
- $0.5mV/Sec$  Drift Typical @  $C_S = 0.01\mu F$
- TTL and CMOS Compatible
- Short Circuit Protected
- Input Offset Voltage Adjustable to  $< 100\mu V$  Using A  $20k\Omega$  Potentiometer
- 0.1% Guaranteed Sample Accuracy With  $10V$  Signals and  $C_S = 0.01\mu F$
- Sample to Hold Offset Is  $5mV$  Max

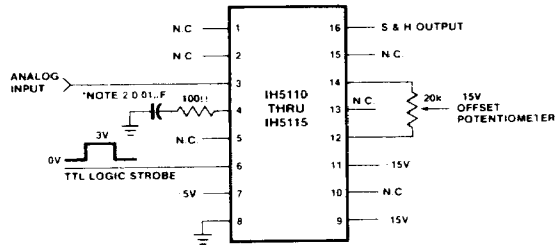
### ORDERING INFORMATION



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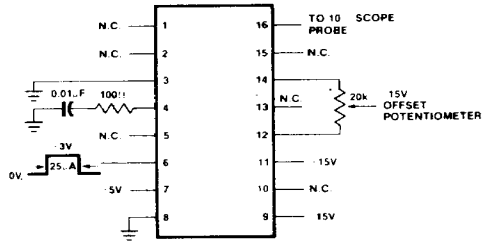
APPLICATIONS INFORMATION



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- NOTES:** 1. To trim output offset to 0mV, set strobe input to sample mode (3V), set analog input to GND, adjust potentiometer until S & H output is 0mV.  
 2. Use a low dielectric absorption capacitor such as polystyrene.  
**SAMPLE MODE** occurs when logic input is greater than 2.4V.  
**HOLD MODE** occurs when logic input is less than 0.8V.

Figure 3: Typical Connection Diagram

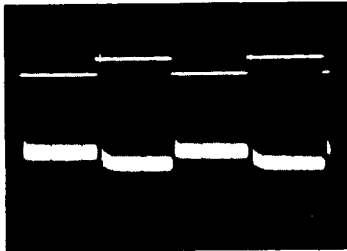


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Adjust offset to 0mV before testing for charge injection. See note 1.

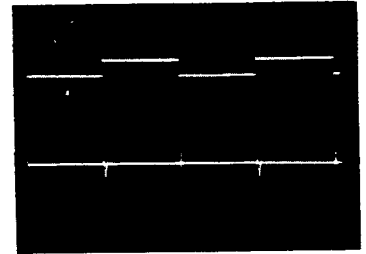
CHARGE INJECTION

SWITCHING TRANSIENTS



V<sub>s</sub> - GND  
 LOGIC INPUT  
 C - 0.01.F

UPPER TRACE - 3V  
 LOWER TRACE - 5mV/DIV.  
 TIME - 10.μs/cm



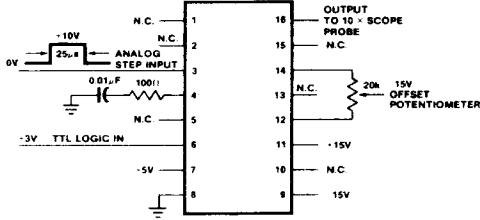
V<sub>s</sub> - GND  
 LOGIC INPUT  
 C<sub>s</sub> - 0.01.μs

UPPER TRACE - 3V  
 LOWER TRACE - 500mV/DIV.  
 TIME - 10.μs/cm

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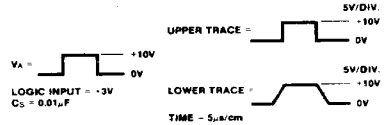
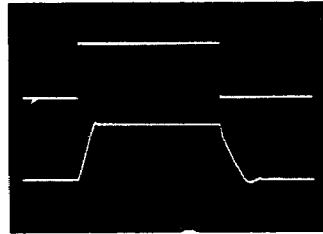
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Figure 4: Charge Injection (sample to hold offset) Measurement Circuit; also Switching Transients Test Circuit



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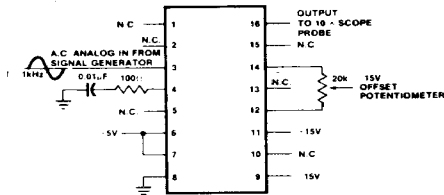
ACQUISITION TIME



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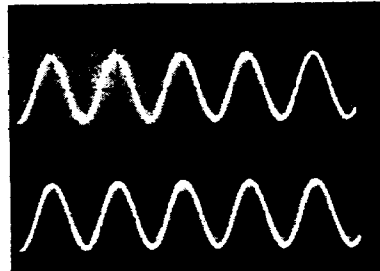
**NOTE:** The acquisition time is actually a settling time spec, since the reading is only taken when the output has settled within 1% of its final value. The 6µs spec. (IH5111, 5113 & 5115 is the worst reading of the  $t_{on}$  or  $t_{off}$  settling time shown above. The above test can be performed with a 0 to +7.5V or 0 to -7.5V step for the IH5110, 5112, 5114.

**Figure 5: Typical Circuit for Measurement of A.C. Signal Handling Capability**



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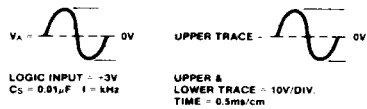
A.C. PEAK TO PEAK



TYP. IH5111

HT00003I

To test this parameter, increase the amplitude of the signal generator until the output starts to distort (it will always show up on the positive excursion of the sine wave first); then back off until all distortion is gone. The resultant peak to peak swing must be greater than 15Vpp for the IH5110, 5112, 5114 and greater than 20Vpp for the IH5111, 5113, 5115.



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**Figure 6: Typical Circuit for Measurement of A.C. Peak to Peak Signal Handling Capability**

## APPLICATION TIPS

The following text serves as a guide in choosing the correct device from the IH5110 family.

First, determine the input voltage range.

The even numbered parts are designed to switch smaller A.C. signal amplitudes with the goal being to minimize the charge injection effects (sample to hold offsets). This charge injection error is shown in Figure 4. Once the voltage offset is zeroed, the 5110 has typical error amplitudes of 1 to 2mVp-p (corresponds to 10pc to 20pc of charge). Thus one could sample very low level d.c. signals with extreme accuracy. If very low level A.C. signals are being sampled, voltage offset potentiometer can be adjusted for a zero charge injection effect. Once the potentiometer has been adjusted, there will be a zero error going from sample to hold; however there will be a d.c. error caused by adjusting the potentiometer for zero charge injection and not for zero voltage offset. In general, this d.c. error will be in the area of 2mV to 5mV.

The odd numbered parts are primarily designed to handle any input in the plus or minus 10V range, regardless of whether it is A.C. or D.C.; to obtain this, the charge injection is about a factor of 2 higher than the even numbered parts.

The use of Varafet switching elements similar to Intersil's IH401/401A leads to a trade-off between AC signal swing and charge injection.

After the voltage range and charge injection requirements have been determined, all that remains is to determine the input offset voltage the system can tolerate. By using the higher numbered parts, it is possible to eliminate the offset potentiometer if system accuracy will allow 5mV (5114, 5115) or 10mV (5112, 5113) due to the low input offset voltage on these devices.

The drift rate is specified at 10mV/sec. Max. for all models: this corresponds to approximately 100pA total leakage into a 0.01 $\mu$ F sampling capacitor ( $C_S$ ). While the 10mV/sec. is the Max. encountered, a more typical reading is less than 1mV/sec. (true for any input between -10V and +10V); thus the IH5110 family is ideal for applications requiring very low drift or droop rates.

The aperture time is spec'd at 200ns Max. for all models, but a more typical value is 150ns; this is basically the off time of switch  $Q_1$ . The way this aperture time affects system accuracy is shown below:

Assume the input signal to the Sample and Hold is an A.C. signal of peak amplitude A (peak to peak swing is 2A) and frequency  $2\pi f = \omega$ , then  $V_{input} = Ae^{j\omega t}$  and  $dV/dt$

$= jA\omega e^{j\omega t}$ . This means the slope of input signal  $= (dV/dt)$  is a maximum at  $t$  (time) = 0. This maximum value is  $\omega A$  (A = amplitude). (i.e.) input frequency is 10kHz, therefore  $dV/dt = \omega A = 6.28 \times 10^4 \times 10V = 6.3 \times 10^5 V/sec$ .  $A = 10V$ , the slope or  $dV/dt = 0.63V/\mu s$ . Now if we wish error to be Max. of say 1% of full scale 10V, we see that 100mV (1% aperture time = 0.63V/ $\mu s$ ). Solving this equation we see the aperture time must be 160ns or less to get 1% holding accuracy. Since our aperture time is 150ns typical, we have 1% accuracy in holding 10kHz varying signals; for signal frequencies 1kHz and less, Max. error is 0.1%. The simple interpretation of just how the off time of the switch causes this system error is due to the fact a finite time is required for the switch to react to a hold command; this reaction time manifests itself with a system voltage error because the time varying input signal is changing to a new value before the switch has actually turned off. (i.e.) in the above example off = 10kHz and  $A = 10V$ , suppose we gave the hold command (thru TTL logic) at  $t = 0$  (A.C. signal goes thru zero pt.) At this point we have calculated the slope to be a Max. and equal to 0.63V/ $\mu s$ . If there were no aperture time error, we would read 0V at output of Sample and Hold; however because of finite time for switch to respond to hold command, 150ns passes before switch goes off. During the 150ns, the input signal has gone to 100mV above or below 0V, thus the stored value of signal will be 100mV and that is the reading at the output of the Sample and Hold. If the input frequency were 1kHz, the "error voltage" would be 10mV.

## DEFINITION OF TERMS

**Aperture Time:** The time it takes to switch from sample mode to hold mode and the actual opening of switch.

**Charge Injection:** The amount of charge coupled across the switch with no input voltage.

**Drift Rate:** The amount of drift of output voltage at a rate caused by current flow through the storage capacitor.

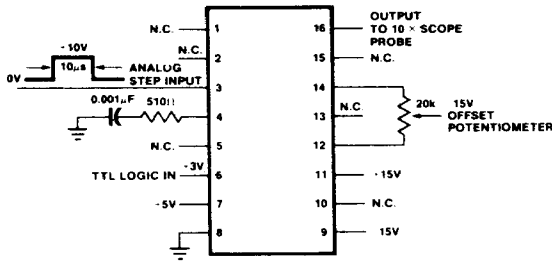
$$\left( \frac{dV}{dt} = \frac{i}{C} \right)$$

This current is the leakage across the switch and the amplifier's bias current.

**Feed Through:** The amount of input signal that appears at the output when in the hold mode. Normally caused by capacitance across the switch.

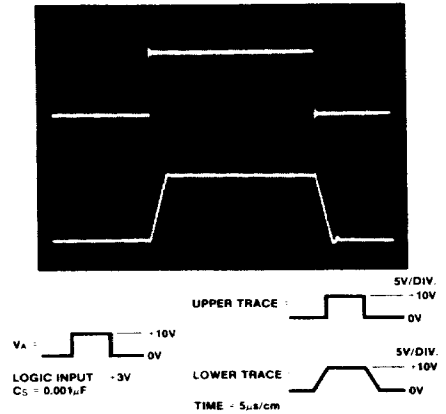
**Offset Voltage:** Voltage measured at output with no input voltage and circuit in sample mode.

**Acquisition Time:** The time it takes amplifier to reach full scale output either plus or minus.



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HI-SPEED SAMPLE AND HOLD



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**NOTE:** Typical times for the Sample and Hold to acquire the input are  $2\mu\text{s}$  for turn on (output goes to +10V) and  $3\mu\text{s}$  for turn off (output goes down to 0V). As a general note, all the electrical specifications are guaranteed with a sampling capacitor equal to  $0.01\mu\text{f}$ . As the above application (Fig. 6) shows, other values of sampling capacitors can be used but the best combinations of S & H specs may not result with values other than  $0.01\mu\text{f}$ . The only advantage of using a  $0.001\mu\text{f}$  for  $C_S$  is the acquisition time is  $2\mu\text{s}$  typical instead of  $5\mu\text{s}$  typical (with  $0.01\mu\text{f}$ ; however the drift rate would be worse and charge injection would be affected). To minimize drift rate, use a  $0.1\mu\text{f}$  capacitor; this should produce a  $0.1\text{mV}/\text{sec}$  rate of change and a charge injection amplitude of  $0.2\text{mVp-p}$ . Of course the acquisition time will be slowed down to the  $25\mu\text{s}$  area. Also use a  $0.1\mu\text{s}$  system for slow speed changes (i.e., input frequency is less than  $1\text{kHz}$ ). The series resistor should be about  $100\Omega - 200\Omega$  to stabilize the system.

**Figure 7: Connection For Hi-Speed Sample and Hold With Following Typical Performance:  $W/C_S = 0.001$**

- a.  $2\mu\text{s}$  settling time (acquisition time) to 1% accuracy
- b.  $25\text{mV}$  charge injection amplitude
- c.  $10\text{mV}/\text{sec}$  drift rate