Document No.	853–1084
ECN No.	91141
Date of Issue	October 27, 1987
Status	Product Specification
Memory Products	

82S141 / 82S141A
4K-bit TTL bipolar PROM

DESCRIPTION

The 82S141 and 82S141A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S141 and 82S141A are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

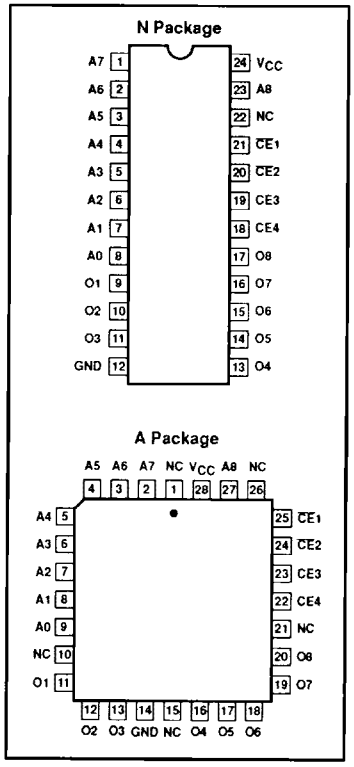
These devices include on-chip decoding and 4 Chip Enable inputs for ease of memory expansion. They feature 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

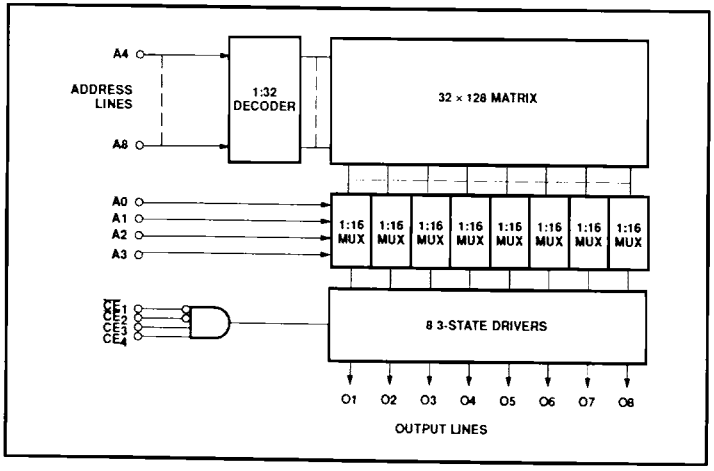
FEATURES

- Address access time:
  - N82S141: 60ns max
  - N82S141A: 45ns max
- Power dissipation: 76µW/bit typ
- Input loading: -100µA max
- On-chip address decoding
- Four Chip Enable inputs
- Outputs: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

PIN CONFIGURATIONS



BLOCK DIAGRAM



APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

4K-bit TTL bipolar PROM (512 × 8) — 82S141 / 82S141A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 300mil-wide	N82S141 N3, N82S141A N3
24-Pin Plastic Dual-In-Line 600mil-wide	N82S141 N, N82S141A N
28-Pin Plastic Leaded Chip Carrier 450mil-square	N82S141A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	I_{IN} = -12mA		-0.8	-1.2	V
Output voltage[2]						
		$\overline{CE}$1,2 = Low, CE3,4 = High				
V_{OL}	Low	I_{OUT} = 9.6mA			0.45	V
V_{OH}	High	I_{OUT} = -2mA	2.4			V
Input current[1]						
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}$1,2 = High, CE3,4 = Low, V_{OUT} = 5.5V			40	µA
		$\overline{CE}$1,2 = High, CE3,4 = Low, V_{OUT} = 0.5V			-40	µA
I_{OS}	Short circuit[4]	$\overline{CE}$1,2 = Low, CE3,4 = High, V_{OUT} = 0V High stored	-15		-70	mA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V		125	175	mA
Capacitance						
		$\overline{CE}$1,2 = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Typical values are at V_{CC} = 5V, T_{amb} = +25°C.
4. Duration of short circuit should not exceed 1 second.
5. Measured with all inputs grounded and all outputs open.

4K-bit TTL bipolar PROM (512 × 8) — 82S141 / 82S141A

AC ELECTRICAL CHARACTERISTICS

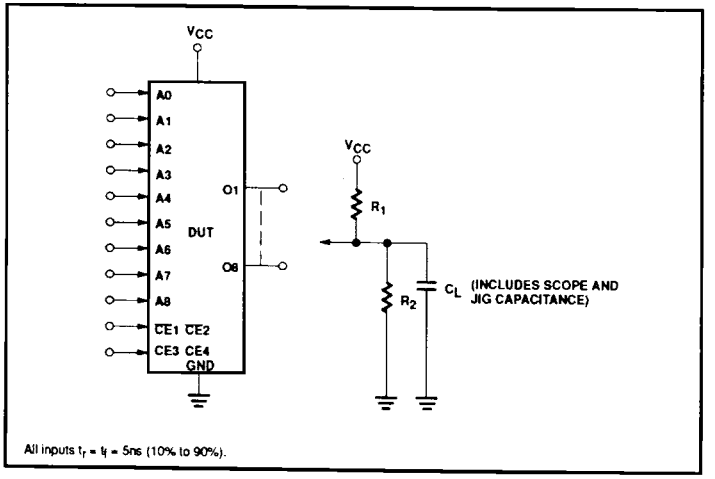
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S141			N82S141A			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	
Access time[2]										
t_{AA}		Output	Address			60			45	ns
t_{CE}		Output	Chip Enable			40			30	ns
Disable time[3]										
t_{CD}		Output	Chip Disable			40			30	ns

NOTES:

1. Typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. Tested at an address cycle time of 1µs.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.

TEST LOAD CIRCUIT



All inputs $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS