INTERFACE SPECIFICATION
SMDS CONTROL AND REASSEMBLY FORMATTER
UGA-210

1. INTRODUCTION

The SMDS Control and Reassembly Formatter (SCARF) provides a single-access SMDS service termination for connectionless data "datagram" transfer according to Bellcore TR-TSV-000772 and TR-TSV-000773. Both CPE and Switching System interface functions are provided; maintenance and billing functions specified in TA-TSY-000774 and TR-TSV-000775 are supported. The SCARF provides DS1, E1, DS3, and E3 physical layer convergence procedure (PLCP) functions and provides for the segmentation and reassembly of SMDS Interface Protocol (SIP) Level 3 messages. Up to 128 messages can be reassembled concurrently. The host system can transfer data either through a dedicated host input/output port or to and from a local microprocessor.

The SCARF provides many features that are a part of IEEE Standard 802.6-1990, "Distributed Queue Dual Bus (DQDB) Subnetwork of a Metropolitan Area Network (MAN)". In particular, the features required to implement connectionless data transfer at "Head of Bus A" node for the dual bus are included.

The DS1, DS3, E1, and E3 data stream interfaces connect directly to framer products available from $Base_2$ Systems. The E1 PLCP function conforms to ETSI draft standard T/NA(91)17, "Metropolitan Area Network Physical Layer Convergence Procedure for 2.048 Mb/s;" the E3 PLCP function conforms to ETSI draft standard T/NA(91)18, "Metropolitan Area Network Physical Layer Convergence Procedure for 34.368 Mb/s."

The SCARF provides access to the SMDS protocol at all levels for test and diagnostic functions. Multiple host interface formats and functions are supported. Octet-wide simultaneous interfaces are provided for transmit and receive access to PLCP slots (57 octets), L2_PDUs (53 octets), segments (48 octets), or segment payload only (44 octets). This interface allows the implementation of test and diagnostic systems.

Direct host interfaces to support HDLC formats and computer bus interfaces for L3_PDU message transfer are provided. The SCARF provides both transmit and receive functions for all line rates up to 52 Mbit/s and transfer to and from the host in bursts at up to 250 Mbit/s. The functions of the SMDS Data Exchange Interface (DXI) described in the SMDS Interest Group document SIG-TS-001/1991 are also supported.

All control and status functions are provided via a direct local processor interface. The local processor can also control the DS1, DS3, E1, or E3 framer as required.

The local processor interface requires a 16-bit data bus and 1 Mbyte of address capability, with either multiplexed or separate address and data signals. Two interrupt outputs are provided, one for message transfer and the other for status information on protocol and PLCP performance. Typical microprocessors that can be used with the SCARF are the Intel 80C186 and Motorola 680x0 microprocessors. Direct interfacing is also provided for the Intel 80960CA and 80960SA. Only 16-bit word transfer is supported.

The local processor or host interface can also provide input to the buffer RAM for entire PLCP slots or frames, or access at any other level of the protocol for test or diagnostic purposes.

1.1. Block Diagram

A block diagram of the SCARF is shown in Figure 1.1. The part set to realize a complete SMDS interface consists of a microprocessor, a framer for the transmission line, buffer RAM realized with static RAM ICs, and the SCARF IC. A line interface unit (LIU) is generally required at the framer to provide the electrical or optical interface to the transmission line. The microprocessor can also manage the framer. The host system can be realized as a computer bus, a direct HDLC interface, or other physical transmission link.

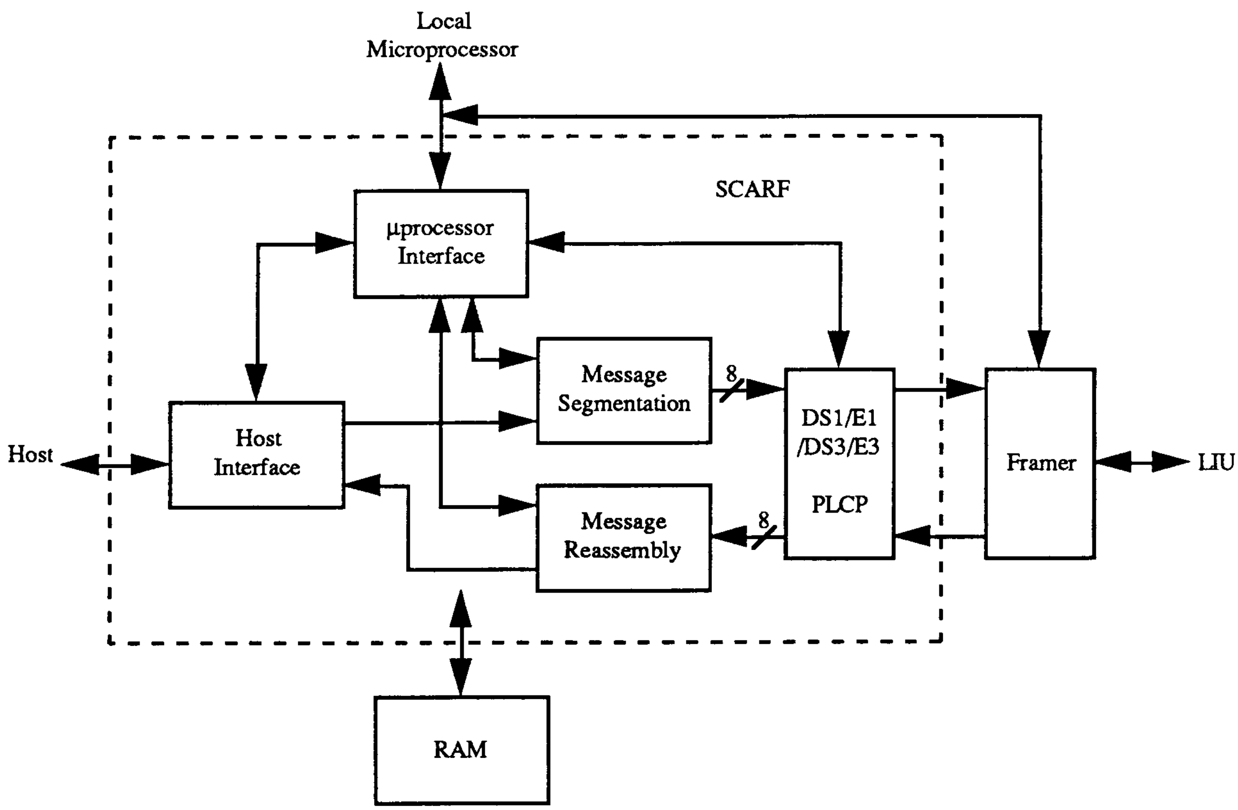


Figure 1.1. SCARF Block Diagram

The message flow from the host interface is through the buffer RAM, to the segmentation block, and then to the transmit PLCP block. Segmentation message status is conveyed between blocks and to the local processor by means of a "stack" realized in buffer RAM and pointers to the stack in registers available to the local processor.

In the receive direction, the PLCP signal is framed, L2_PDUs are checked for status, and L3_PDUs are reassembled in the buffer RAM. When a message is completed, a stack protocol enables transfer to the host through the host interface.

Alternative modes allow access to the SIP protocol at any level. The PLCP clock, sync, and octet outputs and inputs can be provided at the host interface pins, providing direct access to the PLCP data. L2_PDUs or segments can be transferred through the host interface as well as L3_PDUs. A test mode is provided that allows entire PLCP frames to be transmitted to and from the buffer RAM for test equipment or diagnostic applications. All protocol verification can be disabled selectively.

1.2. PLCP Functions

The SIP Level 1 functions provided include generation of the PLCPs for the appropriate transmission rate and framing of the received PLCP signals. The framing octets, path-overhead identifier octets, and bit-interleaved parity are all generated by the transmitter. These signals are recovered in the receiver and all necessary maintenance functions are performed. The octet bit interleaved parity (BIP-8) code is checked and error status generated for the far-end block error (FEBE) function, yellow alarm status, and link status code. BIP-8 code violations and framing-octet errors are counted. Out-of-frame events are also detected and counted. The PLCP transmit output can be looped to the receiver input for test purposes and to perform startup self tests and diagnostics. PLCP functions are described in section 4.

The line signal interface consists of clock, serial data, and sync signals. Both framed and unframed modes are provided for all PLCPs. In framed mode, the frame bit positions of the transmission format are located via a synchronization signal and are generated as idle bits or ignored. In unframed mode, the external clocks are assumed to be "gapped," and no transmission-layer framing information is expected. At DS3 rates, the unframed mode can be used to support the proposed (IEEE 802.6) SDS3 line format. External hardware is required to perform 8B/10B conversion.

The transmitter interface has a clock and frame sync signal input and provides the data output. The receive signal interface consists of input clock, data, and frame synchronization signals from the transmission physical-layer framer. The transmit and receive sections of the interface are clocked independently.

An external 8-kHz signal input can be provided for the synchronization of the transmit PLCP frames in DS3 and E3 modes. Otherwise, synchronization is provided by the received PLCP, and "cycle stuffing" is used if the received PLCP goes out of frame. In all PLCP modes, an external out-of-frame input from the framer can be used to indicate that the received signal is not being received correctly. This input will inhibit reassembly and initiate cycle stuffing when required.

PLCP status indications include 16-bit counters for PLCP out-of-frame events, framing-octet errors, and BIP-8 code violations for both the near and far end. All alarm indications are provided, and can be programmed to generate interrupts. PLCP error counters can be programmed to accumulate errors over one-second periods and latch the results.

An external PLCP option is provided in which PLCP octet clock, sync and data are provided to and from the host interface. One-half of the 16-bit interface is used for input data and the other for output data. Clock, slot/segment sync, and PLCP frame sync are all provided for both transmit and receive. In addition, test modes are available that allow entire PLCP frames or L2_PDUs to be inserted from RAM and to be written to RAM. This allows the flexible generation of test sequences.

1.3. SIP Segmentation Functions

Segmentation refers to the subdividing of level 3 messages, or L3_PDUs, to segments that are transmitted within level 2 slots, or L2_PDUs. The SCARF provides modes that perform this segmentation function as well as modes that just pass L2_PDUs or segments. The segmentation functions are described in detail in section 6.

There are six segmentation modes. Two test modes allow the generation of repeating PLCP frames or L2_PDUs from buffer RAM. Two pipeline modes allow either 53-octet or 52-octet L2_PDUs or 48-octet segments to be transferred from the host. The L2_PDU is transferred across the host interface with or without the header check sequence (HCS) overhead; if the HCS position is present it is ignored and the HCS is recalculated and inserted by the SCARF. The payload CRC can either be inserted or checked and transferred without modification. Both the HCS and the payload CRC can be optionally disabled or errored on a single-event basis. Two modes are provided for L3_PDU segmentation; the L3_PDUs can be segmented either after the complete L3_PDU arrives from the host or on a segment-by-segment basis, as the host transfers segments.

The SCARF is capable of performing as head of bus A, as required for the switching system side of the SIP. These functions include implementing a single instance of the DQDB state machine and implementing the message ID (MID) allocation algorithm specified in section 4.2.3 of TR-TSV-000772. In addition, the bandwidth-balancing modulus of IEEE 802.6 is supported.

When L3_PDU segmentation is performed, L3_PDU messages are transferred from the host to the segmentation buffer area of the RAM. Each message to be transmitted is segmented into 44-octet payload segments. Each segment is then prefaced by both a five-octet L2_PDU header and the two-octet type, sequence number, and message ID payload header. The access control field and the header are programmable; this allows the use of other than the default virtual channel identifier (VCI) for connectionless data transfer. The segment header is generated by the segmentation circuit, with the message ID inserted from a memory location that the local processor writes. The payload length and the payload CRC fields are calculated as required and appended at the end of the segment.

All L3_PDU format fields can be provided by the SCARF or can be selectively transferred from the host block. L3_PDU overhead that is transmitted from the host can be overwritten by the SCARF. The segmentation block can provide the 32-bit CRC that is an optional feature of the IEEE 802.6 standard. The CRC is generated as a part of the segmentation process and inserted in the transmitted message.

All address screening functions required in TR-TSV-000772 section 3.2.6 are supported for egress screening in the segmentation circuit. The source address of group addressed packets can be screened to determine if the source address is listed as a local originating address. Four individual address screens of the source address totaling 128 addresses are supported.

The message generation process is controlled by a "stack" protocol that operates between the host interface circuit and the segmentation block. Depending on the characteristics of the information transfer to and from the host, message generation can be autonomously controlled by the host or can be controlled by the local processor. In cases where the message transfer from the host is faster than the PLCP can accommodate, L3_PDU transmission can start as soon as the first few octets of the message are received from the host.

Multiple SCARF ICs can be bit-synchronized and connected to a single transmission framer and thus share a single access port to SMDS. Priority for L2_PDU transmission can be externally controlled or can be allocated in sequence.

Status counts are maintained of non-idle L2_PDUs transmitted and L3_PDUs transmitted.

1.4. SIP Reassembly Functions

Reassembly refers to the concatenation of received L2_PDU payloads to reconstitute an L3_PDU. SCARF provides modes both for reassembly of messages and for delivery of L2_PDU slots or segments. The reassembly process is described in detail in section 7.

There are six modes available for reassembly. Two test modes are provided that write entire PLCP slots or entire L2_PDUs directly to memory. Two pipeline modes are available; one delivers entire L2_PDUs and the other delivers 48-octet segments to the host, after any specified level 2 checks are completed. Two modes provide reassembly of L3_PDUs. One does logical reassembly only; it delivers to the host 48-octets that are accepted as a part of a message with segment overhead intact. The other reassembles complete L3_PDUs in memory; the L3_PDUs are transferred to the host in the order that they complete the reassembly process.

SIP Level 2 protocol verification provided includes HCS validation, L2_PDU header validation, validation of segment type and MID value, valid payload length, and correct payload CRC value.

Continuation segments are checked for correct sequence number and against the specified message length. Up to 128 messages can be reassembled concurrently as long as adequate buffer memory space is available. Each validation step can be individually disabled.

Each message is allocated storage space in the buffer memory. The local processor provides a timer associated with each message that is started when the beginning-of-message segment is received and updated using an interrupt-driven/message control stack system.

At the completion of a received message of the correct length with matching beginning and end tags, the local processor is notified of message completion. Depending on the characteristics of the particular host interface option selected, the message may be autonomously transferred to the host or stored pending local processor communication with the host. Each Level 3 message validation step can be selectively disabled.

If the message timer expires before the message is complete, the local processor can intervene to halt the reassembly process on that specific message.

Each received reassembled message that includes the 32-bit CRC can be checked either simultaneously with the transfer to the host or by an autonomous check function after reassembly. A failure of the CRC can interrupt the local processor. The CRC check can be optionally disabled.

All address screening functions required in TR-TSV-000772 section 3.2.6 are supported for ingress screening in the reassembly circuit. The source address can be screened to determine if the source address is listed as a local originating address and the destination address screened to determine that it is not a local address. Four individual address screens and four group address screens totaling 128 addresses are supported. In CPE, the address screen function can be used to identify addresses reserved for loopback functions, and thus allow the generation of loopbacks at the SMDS level, either as a maintenance function or a diagnostic tool.

Level 2 status information consists of counts of segment header errors, MID/type conflicts, length errors, payload CRC errors, and end-of-message segments for inactive reassembly processes. In addition, counts of processed segments and discarded segments are provided.

Each Level 3 message termination, whether valid or invalid, will be accompanied by specific status information for that message. The errors detected include Level 2 sequence error, a beginning-of-message to an active reassembly process, a beginning-end tag error, a length field error, or a CRC failure. This allows failures to be associated with particular messages and source addresses. Counts are maintained of L3_PDU format errors and of total messages accepted and discarded. In the case of message time-out at reassembly, the reassembly process is halted by the local processor. If an end-of-message indication arrives after time-out, the local processor will be notified and this event will be counted.

All counters can be programmed to cause an interrupt on overflow. Reading the interrupt source register will allow the local processor to identify overflows and thus update internal counts. All counters can be read by the local processor and are cleared when read.

1.5. Logic Diagram

A logic diagram of the SCARF is shown in Figure 1.2. The PLCP interface consists of eight pins. The host interface consists of sixteen data pins, five control inputs, and seven control outputs. The control pin functions are determined by the selected host mode. The RAM interface consists of address, data, and control pins for a 256K x 16 RAM configuration.

The local processor interface consists of eight clock and control inputs, a multiplexed address-data bus, an address bus, and two interrupt outputs. Either separate or multiplexed address and data signals are used, depending on the Processor Select and A/D Multiplex inputs.

Clock and control inputs consist of the system clock that controls the RAM operation, an external 8-kHz reference for the PLCP at E3 and DS3, a one-second input to synchronize PLCP status timing in multiple-port applications, priority inputs and outputs to control L2_PDU generation in multiple-SCARF applications, a "signaling freeze" input that can externally disable reassembly when an external framer loses frame or signal, and one test input. A one-second clock output is provided to allow synchronization of the status for multiple SCARFs or for SCARFs and framers; when a single SCARF is used, ONESECO should be connected to ONESECI. This timing output is derived either from the external 8-kHz reference or from the received PLCP. The MUXPROUT output is used for multiplexing multiple SCARF ICs.

The SCARF is a single CMOS integrated circuit and is packaged in a 160-pin plastic quad flat pack (PQFP) package. Static RAM parts are available in configurations of 32Kx8, 64Kx4, 128Kx8, and 256Kx4, depending on the access time required; SCARF will support all of these RAM configurations.

1.6. Organization of this Interface Specification

Section 2 of this document describes the register functions of the local processor. The overall system configuration options are described in section 3 and the PLCP functions are given in section 4. Operation of the host interface is described in section 5. Segmentation and reassembly functions are given in sections 6 and 7. Address screening is described in section 8. Detailed electrical characteristics and timing information are provided in section 9.

2. LOCAL PROCESSOR INTERFACE

The SCARF is managed by a local microprocessor interface; typical processors that are supported are Intel 80C186, 80960SA, or 80960CA processor or Motorola 680x0. A block diagram of this interface is shown in Figure 2.1.

The SCARF is connected to the local processor as if it were external memory. The local processor can read from or write to registers in the integrated circuit which contain mode control and status information respectively for the SMDS Subscriber-Network Interface.

The local processor can read or write to two different kinds of registers within the SCARF chip. "Direct" read and write operations are to and from latches in the circuit that contain mode control and status indicators. Write and

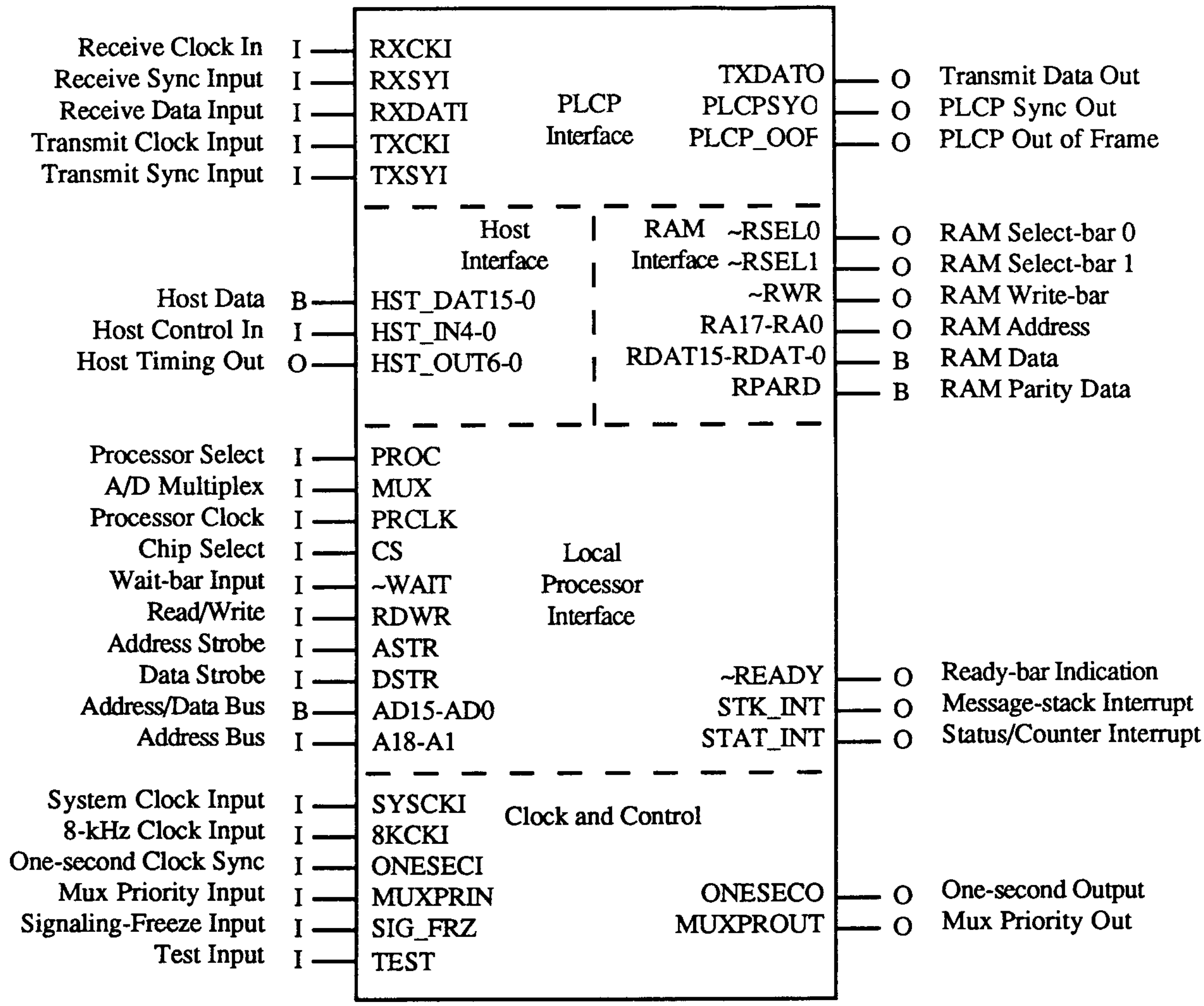


Figure 1.2. SCARF Logic Diagram

"indirect" read operations are to memory locations in the internal RAM in the circuit. These locations contain information associated with protocol overhead, message segmentation and reassembly, and address screening. The buffer RAM interface includes an optional parity bit that can be used to verify RAM accuracy.

Configuration of the SCARF chip, including enabling of interrupts, is selected by setting values in 25 different control registers. These registers can be read as well as written.

There are 35 status registers and counters. PLCP error counters can either be latched at one-second intervals to be read within the following second or can be read independent of that reference. This allows precise counts of one-second accumulations of alarm status and error events without loss of information or distortion due to nonuniform reading intervals or concern for rapid response to the one-second timing mark.

There are two registers which form a direct interface between the local processor and the message segmentation and reassembly sections. This allows the SCARF to be used without a separate host interface.

The local processor can be programmed to be interrupt-driven. All status events, error events, and counter overflows can be programmed to cause interrupts.

2.1. Local Processor Interface Signals

The local processor interface to the SCARF consists of forty-four pins: Address/Data Multiplex Select (MUX), Processor Select (PROC), Chip Select (CS), Address Strobe (ASTR), Data Strobe (DSTR), read/write control (RDWR), processor clock (PRCLK), sixteen multiplexed address/data pins (AD15-AD0), eighteen address pins (A18-A1), a ready-indication output (~READY), a wait input (~WAIT), and two interrupt pins STAT_INT and STK_INT.

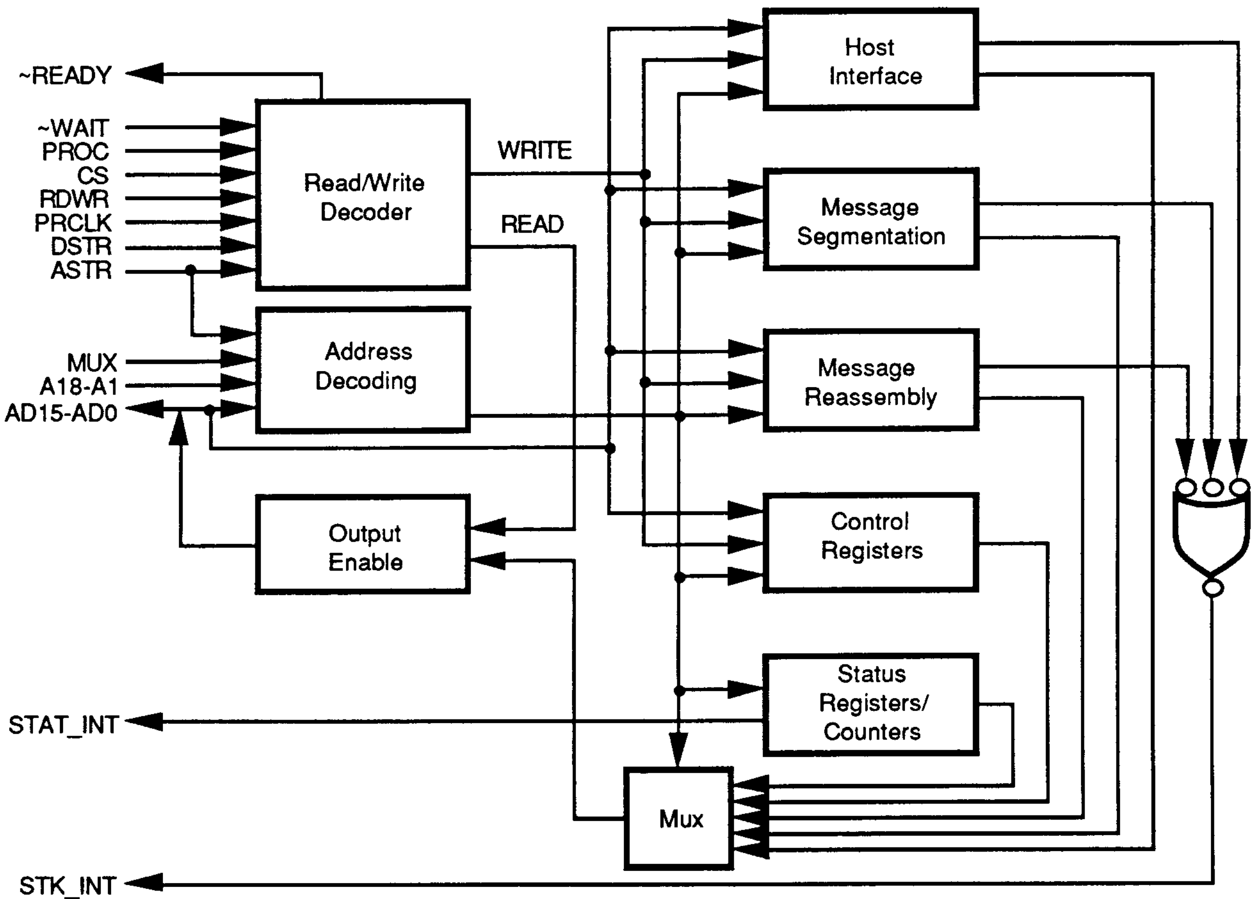


Figure 2.1. Local Processor Interface Block Diagram

The table below give the connections for four representative microprocessors. All of the processors except the 80960SA can be connected directly to the SCARF IC without external logic. The 80960SA requires that the CLK2 input be divided by two externally to be supplied to the SCARF as is required for other peripheral circuits. The MUX and PROC pins must be set as shown to select the appropriate processor interface.

The timing of the Chip Select input must be the same as for the upper address bits normally provided from the microprocessor. The "non-mux/strobe" type provides a generalized non-multiplexed interface with active-low read and write strobes; it thus emulates a static-RAM interface. The clock provided in this case must have a rising edge during the read and the write strobe intervals.

Byte addressing is not supported; only two-byte words may be read from and written to the local processor interface. Pipelined access from the 80960CA will not be supported. All operations will be completed without wait states, except for the 80960CA and 80960SA processor. In their case, the ~READY output is used to provide wait states when burst-mode addressing is used by the processor. ~READY is an active low open drain output requiring and external pull-up.

A ~WAIT input pin is provided as an external ~READY control. When ~WAIT is asserted low the ~READY output is forced high. If ~WAIT is not used it should be tied high.

Microprocessor Type	A/D Mux MUX	Proc. Select PROC	Chip Select CS	Address Strobe ASTR	Data Strobe DSTR	Read/ Write RDWR	Clock PRCLK	AD15-0 ADn	A18-A1 An
80C186	1	1	CS	ALE	~WR	~RD	CLK	AD15-0	A18-A16
Non-mux/Strobe	1	1	CS	1	~WR	~RD	CLK	AD15-0	A18-A1
80960SA	1	0	CS	ALE	~BLAST	W/~R	PRCLK	AD15-1, D0	A18-A16, A3-A1
80960CA	0	1	CS	~ADS	~BLAST	W/~R	PCLK	D15-D0	A18-A1
680x0	0	0	CS	~AS	~DS	R/~W	CLK	D15-D0	A18-A1

2.2. Local Processor Interrupts

There are two interrupt pins provided for the local processor interface. STK_INT provides interrupts for message processing events: SMDS Data Exchange Interface LMI message and FCS violation, L3_PDU segmented, segmentation BAsize violation, L3_PDU reassembly started, L3_PDU reassembly completed, address screening and CRC violations, access class violations, address type violations, level 3 format errors, and host interface message input and output. STAT_INT provides interrupts for all other status and error conditions.

The interrupts are both active low levels with open drains.

Each interrupt source has a bit in an interrupt enable register and in an interrupt status register to allow the local processor to control which conditions cause interrupts and determine the source of the interrupt. These registers are described in section 2.6 below.

2.3. Address Map

The address map for the local processor is given in Table 1. There are three types of address spaces: Control Registers which can be both written and read, Status Registers which can only be read, and RAM buffers which can be indirectly read and written. Write operations are fully decoded and write operations to undefined addresses will have no effect. Read operations from undefined addresses will have undefined results.

2.4. Control Registers

There are twenty-three control registers as shown in Table 2. The control registers are realized as latches within the SCARF and are programmed by a write operation from the local processor. No initialization is provided for operational purposes except for address pointers. All other registers must be initialized as required for each application by the local processor.

All unused control bits are reserved and must be written to 0. All control registers may be read to verify contents, except those control bits whose functions cause events, and are therefore not latched.

2.5. Status Registers

There are thirty-six status registers, as shown in Table 3. Status registers can be read but not written, although some of the status registers, such as counters, will be cleared when read, or have separate clear functions.

Seven status registers contain seven-bit pointers to "stack" functions (actually organized as circular buffers) that are provided to record the processing of both segmentation and reassembly functions on each L3_PDU that is processed. Status bits that record the occurrence of certain processing events are contained on an L3_PDU by L3_PDU basis at memory locations that are identified by the pointer value. Such events can be programmed to generate interrupts on the STK_INT pin; when such an interrupt occurs, the corresponding stack pointer is latched until read, to enable synchronization between such events and the local processor software. Successive reads of the pointer address will give the pointer value when the interrupt occurred and the current value of that pointer, thus establishing the range of stack addresses that contain the individual status bits that record the event. Further details on these functions is contained in sections 6.5.3 and 7.2.

Figure 2.2 shows the individual bit functions of the Part Number/Version Number Register VERSION, which is a status register with a fixed value. This register is located at address 21. The Version Number provides the version number of the part. Part number UGA-210-1 will have the version number set to 1. The Part Number is a four-bit code unique to the UGA-210 (TBD).

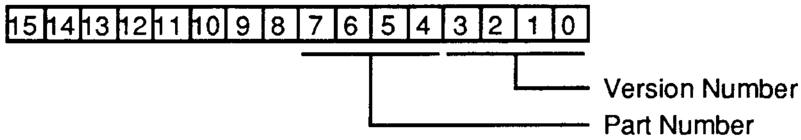


Figure 2.2. VERSION Register (address 21)

2.6. Interrupt Registers

The status and message indications have the capability to interrupt the local processor. As interrupt information is obtained by the local processor the interrupt will be cleared. All interrupt sources are individually enabled by the local processor.

Figure 2.3 shows the individual bit functions of the Interrupt Status Register INT_STATUS. This register is located at address 22. This register indicates which interrupt has occurred. The message event counter overflows, L2_PDU sent, received and discarded, RAM parity error, host L3_PDU input length exceeded, external host errors, and segmentation resources interrupts are indicated in this register, while all other interrupts are indicated by a bit referencing another status register.

If an interrupt is not enabled and the event occurs, the appropriate status bit is still set, even though the interrupt does not occur.

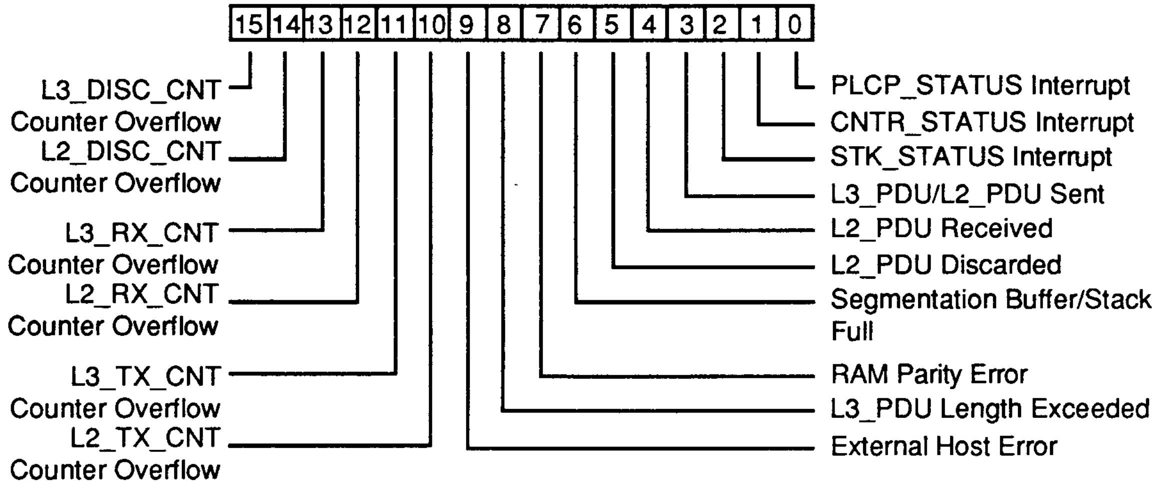


Figure 2.3. INT_STATUS Register (address 22)

PLCP STATUS Interrupt indicates that a status bit has been set in the PLCP_STATUS register; this interrupt is cleared by reading the PLCP_STATUS register at address 24. This interrupt bit will be set only if a status bit is set in PLCP_STATUS and this status bit is enabled to cause an interrupt.

CNTR STATUS Interrupt indicates an overflow status bit has been set in the CNTR_STATUS register at address 23 and that status bit has been programmed to cause an interrupt. The interrupt is cleared by reading that register.

STK_STATUS Interrupt indicates a stack event bit has been set in the STK_STATUS register and it is enabled to cause and interrupt. This interrupt will occur on the STK_INT pin. If this interrupt is processed separately, the STK_STATUS register only has to be read; the summary bit is provided here to allow the two interrupt pins to be connected to the same interrupt input of the local processor if required.

RAM Parity Error indicates that the buffer RAM has determined that a parity error has occurred during a read operation. There is one parity bit for the 16-bit RAM which can optionally be installed. Any detected parity error will set this bit and it will be latched until read.

The other status bits in this register relate to L3_PDU and L2_PDU processing, L3_PDU and L2_PDU activity counters, and the exhausting of segmentation resources by the host.

Figure 2.4 shows the individual bit functions of the Interrupt Enable Register EN_INT. This register is located at address 1C. This register enables interrupts on the status events that are reported in the INT_STATUS register.

If any of the bits in the EN_INT register are set, the corresponding status bit in INT_STATUS will cause an interrupt. The interrupt is level-generated, and remains present until the INT_STATUS register is read. This ensures that no interrupts will be missed. All bits in the register are cleared when the register is read. Note that the RAM Parity Error should not be enabled unless RAM with a parity bit is installed; in this case, as a part of the initialization routine all RAM locations should be written (to any value) to ensure that as locations are read by the circuit RAM parity errors do not occur due to lack of initialization.

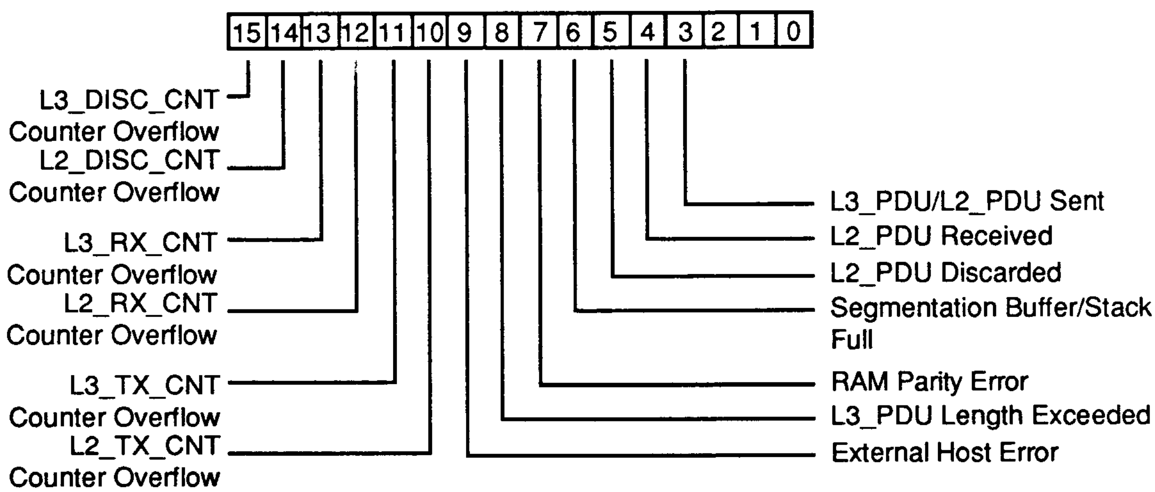


Figure 2.4. EN_INT Register (address 1C)

2.7. Local Processor Host Mode

The local processor can be used as the host interface. In this configuration, the local processor acts as the host as well as the control processor for the SCARF. This mode of operation is described in section 5.1.3.

2.8. Memory Registers

There are locations in the buffer memory that are used for the generation of L2_PDU and segment overhead, for address screening tables, and for other functions associated with the segmentation and reassembly functions of the SCARF.

The local processor is able to read and write all memory buffer locations with addresses of 50 (hex) and above. Writes to buffer memory are direct; a write operation will be completed within fifteen system clock cycles of the end of the write cycle of the local processor.

Read operations from memory are indirect; one read operation passes an address to the SCARF, and the next read operation returns the data from that address. Read operations can be "pipelined;" each read operation to obtain data can pass the address for the next operation. Read and write operations may be interleaved, in which case the data obtained by a read operation corresponds to the address of the last read operation. In general then "N" addresses can be read with "N+1" read operations. Read operations to buffer RAM can be executed once every fifteen system clock cycles.

Although some configuration of RAM is necessary at initialization, few memory buffer read operations are required in normal operation. There is a requirement to read data for logging L3_PDU header information for maintenance and for billing purposes; in addition, the stack contents have to be read in order to time L3_PDU message reassembly.

3. SCARF SYSTEM CONFIGURATION

This section describes the overall system configuration options, including external access to the PLCP.

3.1. System Configuration and RAM Control

The system configuration control word SYS_CONFIG will set the basic system configuration and the RAM options. Its bit map is shown in Figure 3.1.

RAM Size defines the size of the static RAM that is being used for control information, the segmentation buffer, and the reassembly buffer.

Segmentation/Reassembly Buffer Boundary determines the starting address of the reassembly buffer. The segmentation buffer starts at 8K and continues to the start of the reassembly buffer. The reassembly buffer occupies the rest of the RAM contents.

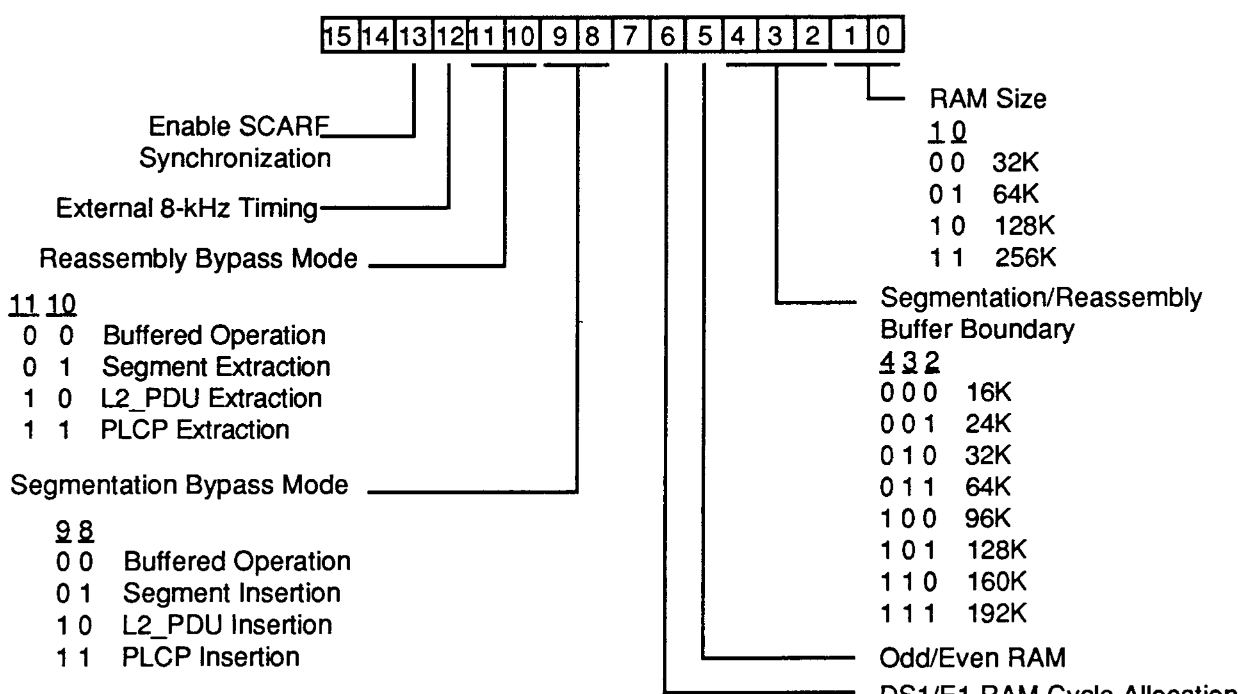


Figure 3.1 SYS_CONFIG Register (address 00)

Odd/Even RAM controls the operation of ~RSEL0 and ~RSEL1. This control allows, for instance, either 128Kx8 or 256Kx4 RAMs in a 256Kx16 configuration. If two "banks" of RAMs are provided (e. g., two sets of 128Kx8 RAMs for a 256Kx16 memory), ~RSEL0 and ~RSEL1 will select between the banks on even (RA0= 0) or odd

(RA1 = 1) addresses; in this case pins RA17-RA1 should be connected to the address pins of the four RAMs. If the control bit is not set, both ~RSEL0 and ~RSEL1 will be active on every RAM operation.

DS1/E1 RAM Cycle Allocation allows the use of a slower system clock when the DS1 and E1 PLCPs are used without greatly reducing the local processor access that is described in section 2.8. When this bit is set, the local processor can execute operations to RAM every nine system clock cycles. However, the maximum transmit or receive PLCP rate is reduced to approximately the system clock frequency. The use of a lower system clock frequency can reduce the power dissipation of the circuit and allow the use of slower static buffer RAM.

The Segmentation Bypass control bits allow direction insertion of octet data at the PLCP, L2_PDU, or Segment level. If both control bits are 0, the host interface functions are determined by the segmentation and host interface control bits, and normal buffered message functions are provided. If these control bits are not both 0, the segmentation block is disabled and the host interface low data bits and control bits are used for message transfer in the segmentation direction. The control bits can allow insertion of 57 octets per slot at the PLCP level, 53 octets per slot at the L2_PDU level, or 48 octets per slot at the Segment level.

In all Segmentation Bypass modes, the PLCP overhead is controlled by the PLCP_CTRL register bits and the insertion of the Header Check Sequence (HCS) and Segment Payload CRC are under the control of the TX_L2_CTRL control register bits. These functions are described in sections 4.1.1 and 6.1.1 respectively.

The functional timing for the external outputs in the PLCP Insertion Mode is shown in Figure 3.2. The clock and sync signals are outputs. Both slot and frame syncs are provided. The slot and frame sync signals transition on the rising edge of the clock signal; the data to be transmitted should transition on the negative edge of the clock signal, as a setup and hold time of approximately one transmit line clock cycle is required relative to the positive clock edge due to internal processing requirements. The Frame Sync is high only on the first slot of each PLCP frame. Both the slot and frame sync signals transition prior to the insertion of the A1 octet in the data.

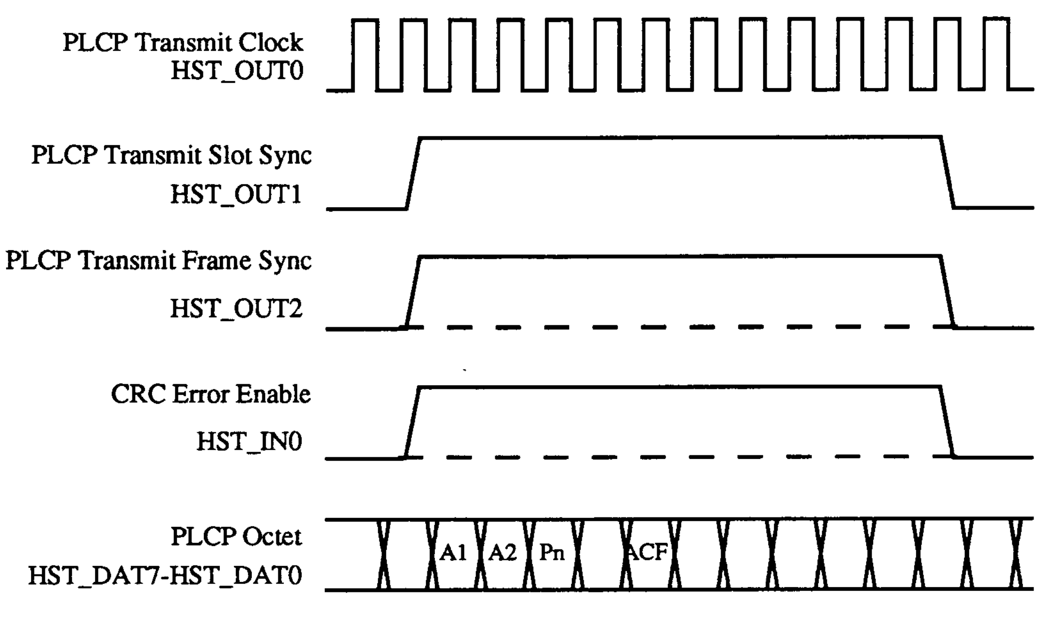


Figure 3.2. Segmentation Bypass Timing - PLCP Insertion

The PLCP octets are entered with the most significant bit (first transmitted on the line) on HST_DAT7 and the least significant bit on HST_DAT0.

In PLCP Insertion Mode, the only PLCP octets that are generated internally are the B1 octet and the C1 octet. This ensures that the proper stuffing and BIP-8 codes can be maintained. If these octets are to be inserted externally, the control bits in the PLCP_CTRL control register that disable the respective octets insertion can be set to disable this function and allow external insertion (see section 4.1.1).

Figure 3.3 shows the functional timing for L2_PDU insertion mode. The transmit clock is "gapped" during the interval when PLCP overhead is inserted by the circuit. The L2_PDU slot sync signal transitions high on the rising edge before the access control field (ACF), which is the first octet of each L2_PDU, is sampled. There are a total of 53 clock cycles per L2_PDU.

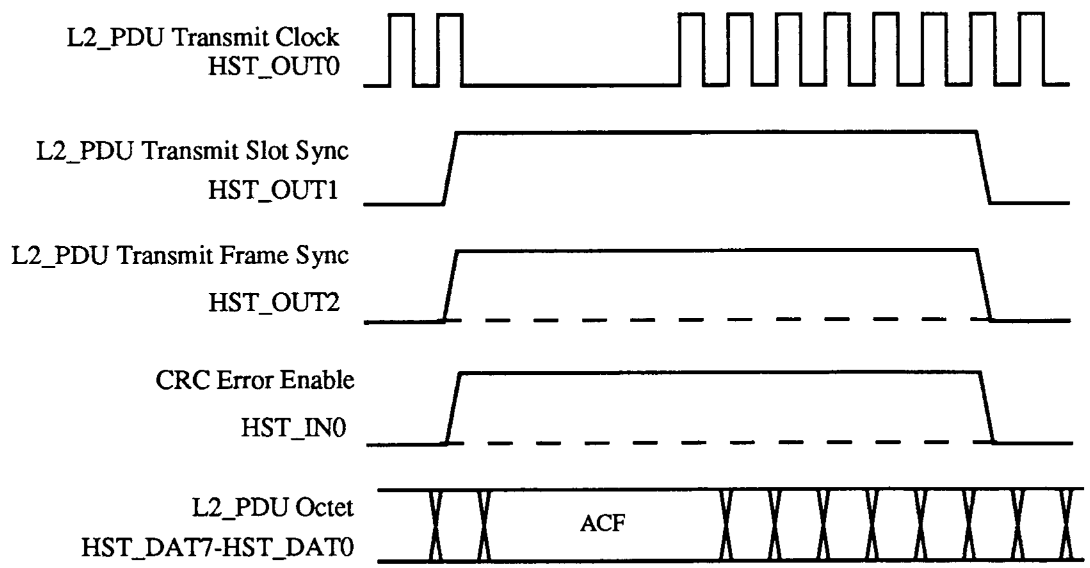


Figure 3.3. Segmentation Bypass Timing - L2_PDU Insertion

In L2_PDU insertion mode, the PLCP_CTRL register controls the PLCP functions. For both L2_PDU insertion and PLCP insertion, the CRC Error Enable signal indicates that the current slot should have an HCS or payload CRC error if one of these functions is enabled in the TX_L2_CTRL register. The first slot to have this signal set after the Error HCS or Error Payload CRC bit is set in TX_L2_CTRL with have the selected field errored.

In Segment access, there are only 48 clocks that are output per slot, and the sync signal is high between the clock edge that samples the last octet of an L2_PDU and the first octet (the first octet of the segment header).

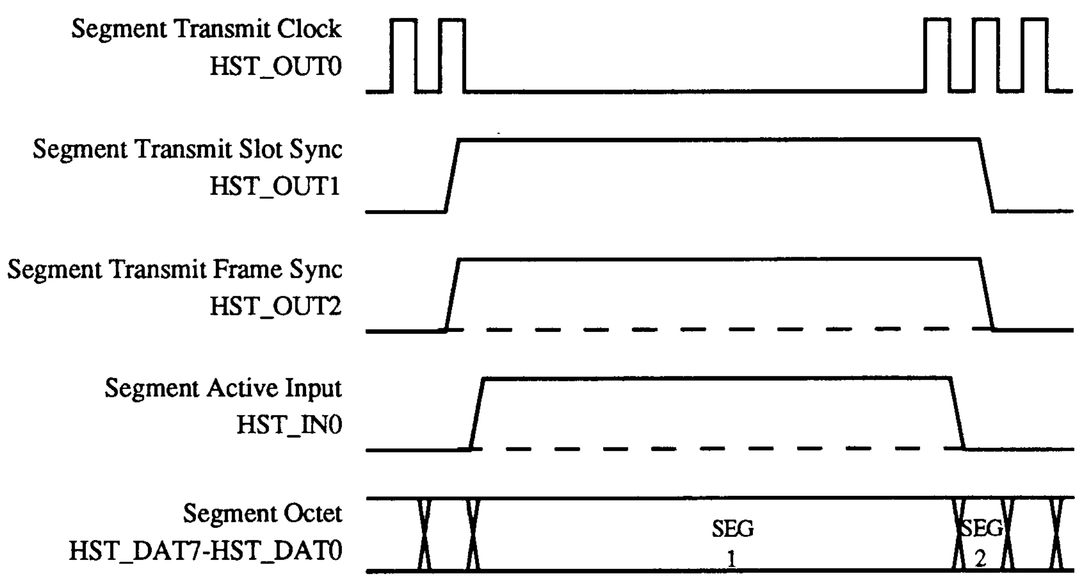


Figure 3.4. Segmentation Bypass Timing - Segment Insertion

In order to set the L2_PDU overhead properly, an additional control input, Segment Active, with the same timing as the first octet is required. This input is set high to generate L2_PDU overhead for active segments and set low to generate L2_PDU overhead for idle or empty segments.

The L2_PDU overhead for active segments in Segment Insertion Mode is defined by the TX_L3_CTRL register as shown in Figure 3.5. The high octet of this register defines the ACF, which is the first octet of the L2_PDU overhead. The low byte of this register defines the third octet of the NCI field, which is the fourth octet of the L2_PDU overhead. The first two NCI octets are set to FFFF (all-1s). For idle segments, all L2_PDU overhead octets are set to 0.

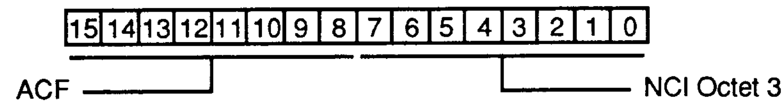


Figure 3.5. TX_L3_CTRL Register (address 04)

The Reassembly Bypass control bits control direct extraction of the received data octets through the host output. Modes are provided for PLCP Extraction, L2_PDU Extraction, and Segment Extraction. The only difference in these three modes is in the clock output, which identifies the octets to be extracted; the synchronization and data outputs are not affected.

Note that for reassembly, the reassembly process can function normally if the buffer RAM is provided. This allows for a physical output function with normal reassembly status outputs provided to the local processor; the local processor can also read reassembled messages from the buffer.

The timing of the outputs for PLCP Extraction is shown in Figure 3.6. A PLCP Receive clock is provided for each PLCP octet; the duty cycle of this clock is nominally 25%. Both PLCP Slot and PLCP Frame synchronization signals are provided; these allow the identification of PLCP overhead as shown in the figure; the PLCP Frame Sync output is low except on the first slot of each PLCP frame. The Slot Sync and Frame Sync signals transition on rising clock edges and can be sampled on the following falling clock edge, along with the received data.

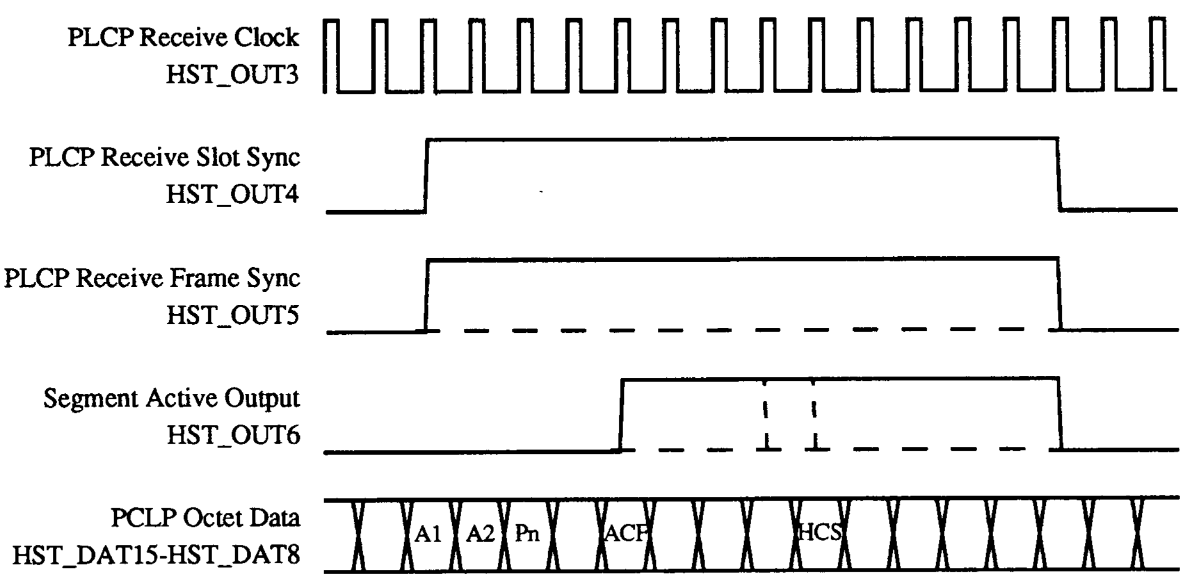


Figure 3.6. Reassembly Bypass Timing - PLCP Extraction

The data octets are received with the most significant bit (first received on the line) on HST_DAT15 and the least significant bit on HST_DAT8.

The Segment Active output is defined by the access control field (ACF), Network Control Information (NCI) field, and header check sequence (HCS) of each received L2_PDU. The Segment Active Output will transition high if the BUSY and the SL_TYPE bits of the ACF meet the criterion specified in the RX_HDR control register (see section 7.7.2). If the NCI field check fails, the Segment Active output will transition after the rising edge of the octet clock that occurs during the last octet of this field. If the HCS check fails, the Segment Active output will transition after the rising edge of the octet clock that occurs during the HCS octet output. Note that these checks can be disabled by control bits in the RX_CHECK register.

The timing of the outputs for L2_PDU Extraction is shown in Figure 3.7. The L2_PDU clock is gapped on the PLCP overhead octets, and the other outputs remain the same as for PLCP extraction.

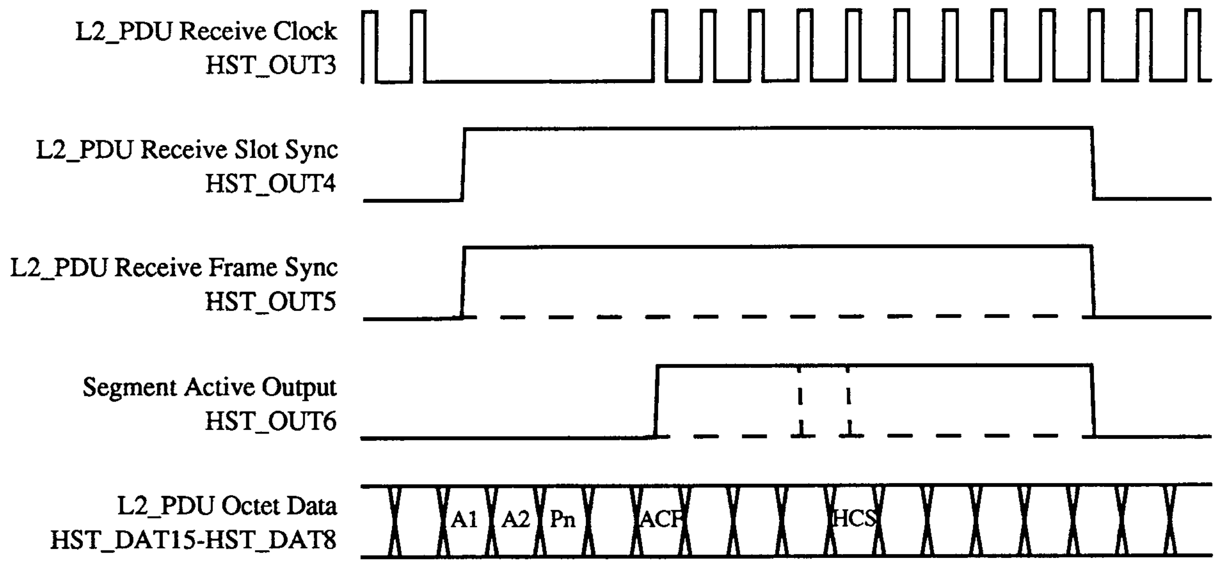


Figure 3.7. Reassembly Bypass Timing - L2_PDU Extraction

The timing of the outputs for Segment Extraction is shown in Figure 3.8. The Segment clock is gapped on the PLCP overhead and L2_PDU header octets, and the other outputs remain the same as for PLCP extraction.

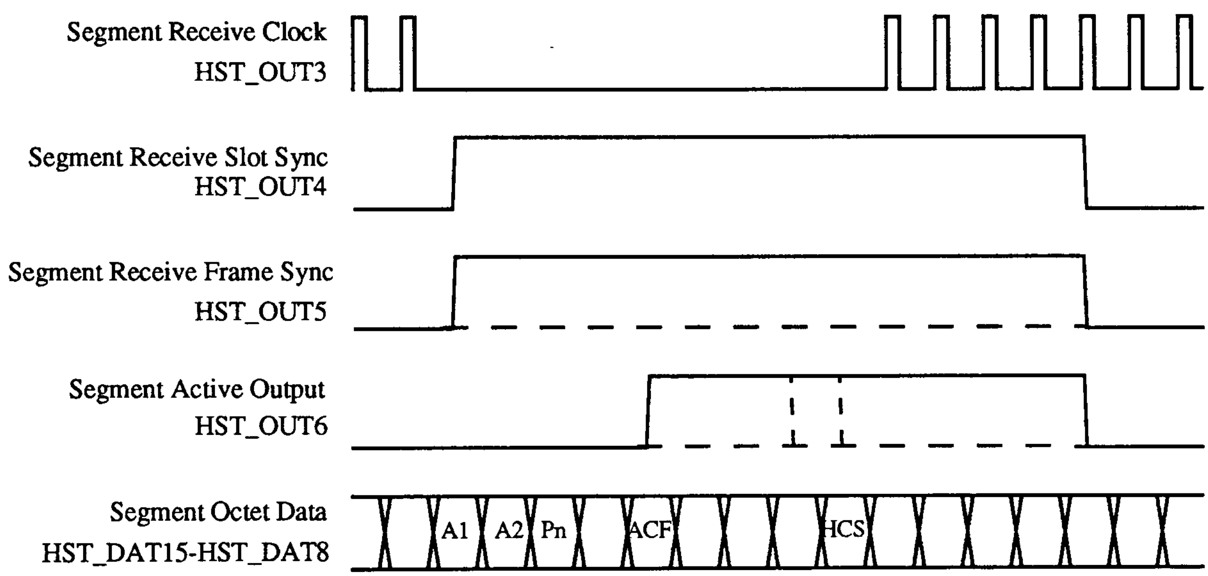


Figure 3.8. Reassembly Bypass Timing - Segment Extraction

In Segment Extraction mode, if either the NCI check or HCS check fails, the Segment Active output will not be high during any of the receive clock transitions.

If both Segmentation Bypass and Reassembly Bypass control bits are set and if the L2_PDU overhead is provided externally for L2_PDU insertion, no buffer RAM or system clock is required for operation of the transmission path.

External 8-kHz Timing forces the transmit PLCP to be synchronized to an external 8-kHz timing reference rather than the received PLCP. This external 8-kHz timing reference is also used as the timing base for a one-second timing circuit that can be used to synchronize the reporting of status information that is required on a one-second basis. To allow this function to be synchronized over multiple parts, an input pin ONESECI is provided to synchronize the counter. When only a single SCARF IC is used, the output of the counter, ONESECO, must be connected to ONESECI.

Enable SCARF Synchronization enables a mode that allows multiple SCARFs to have the transmit PLCPs synchronized.

Bits 14 and 15 are reserved and should be set to 0.

3.2. RAM Buffer Memory

The RAM Buffer Memory contains buffers for segmentation of transmitted messages, reassembly of received messages, and other control functions required for message handling.

The RAM buffer is required for all applications except when both the segmentation functions and the reassembly functions are bypassed. In this case, octets are transferred directly between the PLCP interface and the host interface pins. RAM buffer can be provided but has no application if both the segmentation and reassembly functions are in this mode.

The memory is 16 bits wide and 32K, 64K, 128K, or 256K by option. (This allows use of 32Kx8, 64Kx4, 128Kx8, or 256Kx4 RAMs). This provides a total memory of 0.5, 1, 2, or 4 Mbit. The Odd/Even RAM control bit eliminates the requirement of decoding the address outputs to select between two banks of RAM when that is required.

The bit and byte ordering internal to the memory for internal data signals will be consistent with the IEEE 802.6 and SMDS bit ordering specifications. The most significant bit of the more significant byte of a double-octet will be located in bit 15. This will be the first bit transmitted or received on the serial PLCP line interface. The least significant bit of the less significant byte will be located at bit 0.

4. PLCP INTERFACE AND FUNCTIONS

The SCARF supports physical layer convergence procedures (PLCPs) for DS1, E1, DS3, and E3 rates. At DS3 and E3 rates, all stuffing functions required are supported. Each PLCP is supported in both unframed mode and framed mode.

In unframed mode, the PLCP can respond to a "gapped clock" and provide PLCP support without framing bits. In unframed mode no synchronization signals are provided.

In framed modes, the PLCP transmitter inputs are a clock and a synchronization signal that indicates the position of framing bits in the DS1, E1, DS3, or E3 framing signal. The transmit data stream output is a single serial output. The synchronization signal period can be any multiple of the frame period. The receiver input is a clock signal and synchronization signal as well as the serial received data stream; the synchronization signal can be at any multiple of the frame period.

A multiplexing mode is provided that synchronizes multiple SCARF transmitters and allocates output capacity on a segment by segment basis.

The PLCP transmit and receive interfaces can operate at up to 52 MHz in any mode. Detailed timing information for the PLCP interface is given in section 9.

4.1. PLCP Control

The PLCP Operation is controlled by two control registers, PLCP_CTRL and RX_PLCP_CTRL. The bit map of PLCP_CTRL is shown in Figure 4.1.

PLCP Type sets the PLCP to be used. The PLCP modes are always symmetric; the transmit and receive PLCP modes are identical. The PLCPs for DS1 and DS3 are described in TR-TSV-000773. The E1 and E3 PLCPs are described in ETSI draft standards. The E3 PLCP is based on the frame format that is described in CCITT recommendation G.751.

Framing Mode determines the use of an external sync signal. The normal mode is framed mode; the frame bits in the specific PLCPs are located by a synchronization input and are ignored by the PLCP framer.

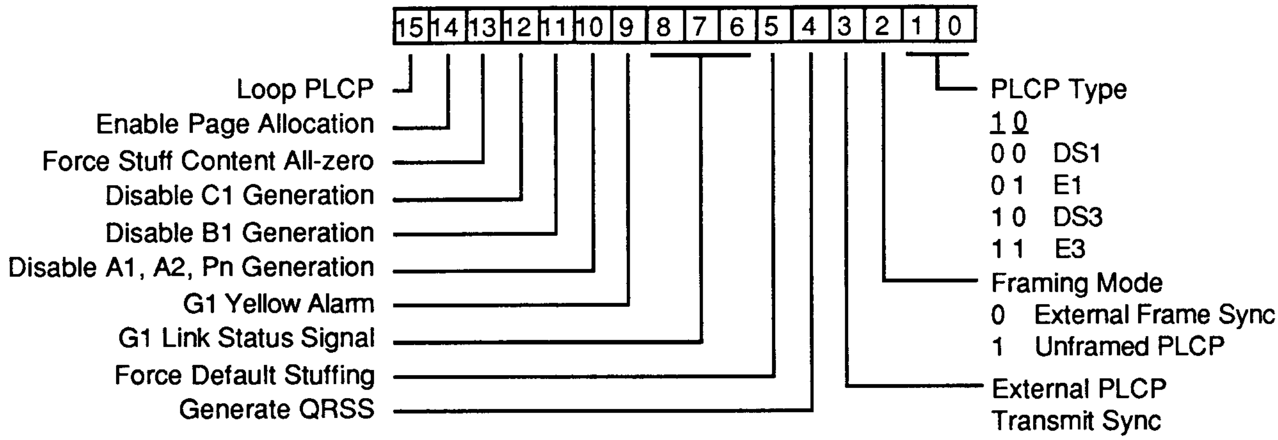


Figure 4.1. PLCP_CTRL Register (address 01)

In unframed mode, frame bits are assumed to be removed externally, or to be non-existent ("gapped clock"). Any PLCP can be used. To provide the "SDS3" format (IEEE standards project 802.6 proposal) the PLCP is set for unframed DS3 operation and the 8B/10B coding and other transmission functions are provided externally.

External PLCP Transmit Sync enables the transmit PLCP to be synchronized by an external signal that is applied to 8KCKI. This function enables multiple SCARFs to be synchronized and is described in section 4.11.

Generate QRSS causes the PLCP content to be replaced by a quasi-random signal stream. This stream is used for certain transmission tests in DS1 systems.

Force Default Stuffing forces the default stuffing operations in DS3 and E3 modes. This bit is ignored in DS1 and E1 modes, which do not perform stuffing. If this bit is not set, stuffing is performed to synchronize the transmit PLCP with either the external 8-kHz frame reference or the receive PLCP, depending on the setting of External 8-kHz Timing in the SYS_CONFIG control word.

The G1 Link Status Signal bits and the G1 Yellow Alarm bit are used to fill the corresponding bit positions in the G1 octet of the PLCP. The FEBE bits of the G1 octet are inserted by the receiver PLCP circuit.

Bits 10-12 of the control word disable PLCP overhead generation on a selective basis; when one of these bits is set, the corresponding overhead is either forced to zero or determined by the external input if that mode is selected in the system configuration register. Disable A1, A2, Pn generation force the first three octets of each PLCP slot to all-zero; this bit also forces the contents of the frame-alignment signal bit positions to all-zero in the E3 PLCP mode. Disable B1 Generation forces the BIP-8 field to be all-zero. Disable C1 Generation forces the C1 field to be all-zero, but does not otherwise affect the stuffing operation in any of the modes.

Force Stuff Content All-zero forces the stuff content of the DS1, DS3 and E3 PLCPs to an all-zero condition. Note that the content of the F1 and Z1-Z4 octets are normally forced to zero by the segmentation process, and so no disabling is provided as this is the default value. The G1, M1, and M2 octets can be disabled directly. The FEBE can be disabled in the RX_PLCP_CTRL register.

The values of the M1 and M2 octets to be transmitted are located in register TX_M1_M2. The page allocation algorithm is required for switch operation, and is defined in TR-TSV-000772, section 4.2.3. This mode can be enabled by setting the Enable Page Allocation bit. This bit enables the insertion of the type 1 layer management octet in the M2 position; the M1 octet is still determined by the contents of the register.

Loop PLCP causes the PLCP receiver input to be taken from the transmitter output in all modes; the transmitter output is unaffected. This function allows the generation of self-diagnostic routines at system startup to ensure the health of the PLCP process as well as the higher-level processes.

Figure 4.2 shows the individual bit functions of the PLCP Receiver Control Register RX_PLCP_CTRL. This register is located at address 06. This register controls PLCP framing, validation, and synchronization.

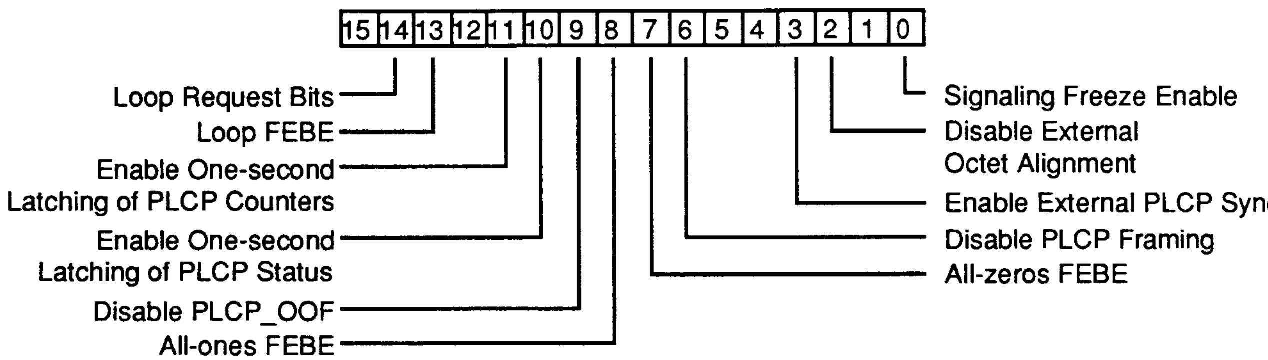


Figure 4.2. RX_PLCP_CTRL Register (address 06)

Signaling Freeze Enable allows an external signal to disable PLCP processing. Internal PLCP functions will operate, but no segments will be accepted by the reassembly state machine. Disable External Octet Alignment inhibits octet alignment of the PLCP framing only as specified by the PLCP. Normally this is effective in all four PLCPs in framed mode; in the DS3 PLCP its effect is to allow nibble alignment. Setting this bit (or setting unframed mode) enables octet alignment to any bit in the data stream.

Enable External PLCP Sync allows the receive PLCP circuit to be synchronized from an external source. To obtain this function, Disable PLCP Framing must be set, Disable PLCP OOF must be set, and the PLCP must be set for unframed E1 mode. This provides a mode in which PLCP slots are received and can be transmitted consecutively.

Disable PLCP Framing prevents PLCP reframing processes.

All-zeros FEBE passes an all-zeros value from the BIP-8 detection circuit to the PLCP transmit block; All-ones FEBE passes all-ones in the FEBE bits. The all-zeros value provides an indication at the far end that no BIP-8 errors are being detected. The all-ones value notifies the far end that the FEBE function is inhibited. In both cases, BIP-8 status and error counts are maintained. It neither of these control bits are set, the normal FEBE based on BIP-8 errors will be generated.

Disable PLCP_OOF allows L2_PDU validation and error counting when the PLCP is out of frame.

Enable One-second Latching of PLCP Status causes PLCP status indications in PLCP_STATUS to be latched at one-second intervals. The one-second interval is determined by successive rising clock edges to ONESECI. If an alarm condition is present during a one-second interval, it is available to be read on the successive interval. Otherwise, the status is latched and held until it is read. If this bit is set and the status word is read twice within a one-second interval, the second read will give the current state of the status word and will clear it. Enable One-second Latching of PLCP Counters provides the same functionality for the counters.

Loop FEBE sets the outgoing FEBE code to be the same as the incoming FEBE. Loop Request Bits causes the transmitted request bits (in the ACF of each L2_PDU) to be the same as those received. These functions are provided for test purposes.

Bits 12 and 15 are reserved for simulation and test functions. They must be set to zero for specified operation.

4.1.1. Segmentation Bypass Mode Operation

This section describes the functions of the PLCP_CTRL register in the Segmentation Bypass modes that are described in section 3.1.

The PLCP Type and the Framing Mode control bits are used to select the PLCP in these modes. External PLCP Sync, Generate QRSS, Force Default Stuffing, Force Stuff Content All-zero and Loop PLCP are also active in all Segmentation Bypass modes.

Enable Page Allocation is active only in Segment Insertion and L2_PDU Insertion modes. In PLCP Insertion mode, the M1 and M2 fields are always taken from the inserted signal.

Disable B1 Insertion and Disable C1 Insertion are active in all modes. In PLCP Insertion modes, if either of these bits is set, the respective field is taken from the inserted input. In L2_PDU Insertion mode and Segment Insertion mode if either of these bits is set the respective fields are all-zero.

G1 Yellow Alarm and G1 Link Status Signal are active only in L2_PDU Insertion and Segment Insertion modes. The respective fields are inserted from the control register. In PLCP Insertion mode, these fields are inserted from the inserted input.

Disable A1, A2, Pn Generation is active in all three modes. In each mode if set it will force these fields to all-zero. If it is not set in PLCP Insertion mode, the inserted signal is used for these octets. If it is not set in L2_PDU Insertion mode or Segment Insertion mode, the standard PLCP overhead octets are provided for the selected PLCP.

4.2. Framed PLCP Transmit Interface

The functional timing for the PLCP transmit interface is similar for all four PLCPs. A transmit clock and a frame-sync signal are provided as inputs to the UGA-210 and the transmit data is generated in response. This interface is compatible with $Base_2$ Systems UGA-300 and UGA-360 framers for DS1, UGA-510 for E1, and UGA-330 for DS3 and E3. To maintain this compatibility and to provide the maximum amount of timing margin at DS3 speeds, the transmit circuit provides data on positive clock edges in DS1 and E1 modes and on negative input clock edges in DS3 and E3 modes.

Figure 4.3 shows the transmit timing for the DS1 PLCP. The clock signal TXCKI is 1.544 MHz. The synchronization signal TXSYI has a rising edge prior to the sampling of the frame bit. Note that this signal does not have to be present every frame; in particular, it can be a superframe synchronization signal with a period of 3 ms. The data stream signal TXDATO is the output signal; it transitions in response to the rising edge of the TXCKI clock signal, and can be sampled on the following falling edge. The framing bit position content in the output stream is undefined.

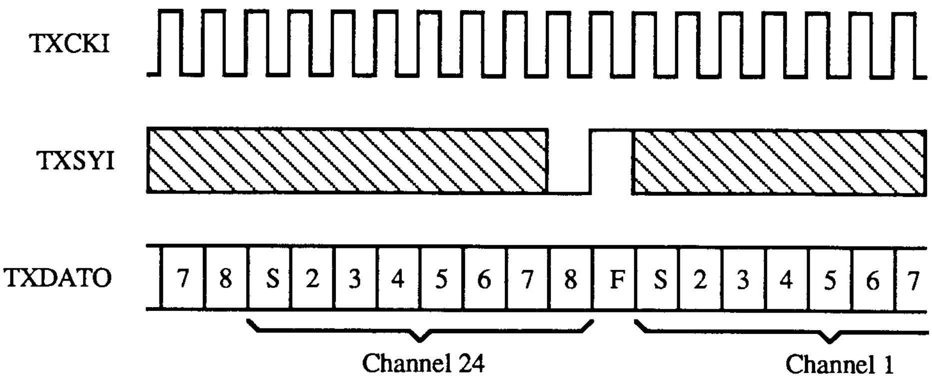


Figure 4.3. DS1 PLCP Transmit Timing

Figure 4.4 shows the transmit timing for the E1 PLCP. The clock signal TXCKI is 2.048 MHz. The synchronization signal TXSYI has a rising edge prior to the sampling of the first bit of time slot 0. This signal can be present every 2 ms. The data stream signal TXDATO is the output signal; it transitions in response to the rising edge of the TXCKI clock signal, and can be sampled on the following falling edge. This timing is compatible with the $Base_2$ Systems UGA-510 Primary-rate CEPT Framer. The content of time slot 0 and time slot 16 of the output is undefined.

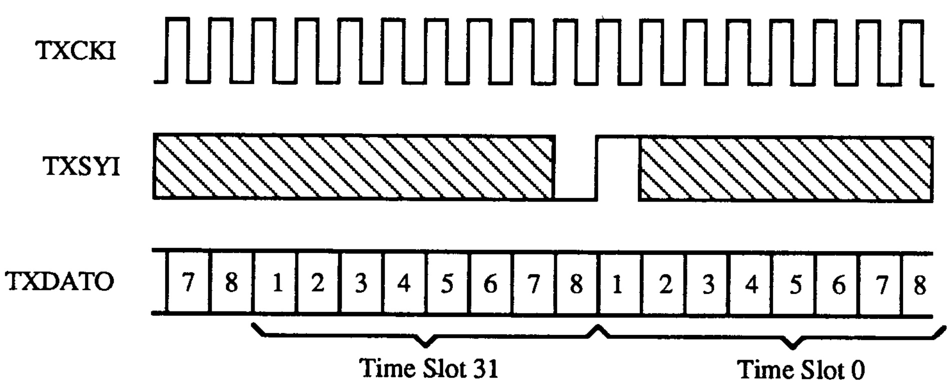


Figure 4.4. E1 PLCP Transmit Timing

Figure 4.5 shows the transmit timing for the DS3 PLCP. The clock signal TXCKI has a frequency of 44.736 MHz. The TXSYI input signal is sampled on falling clock transitions and the TXDATO output changes on falling clock edges. The synchronization signal TXSYI has a rising edge after the sampling of the frame bit (between subframes). The data stream signal TXDATO is the output signal; it transitions in response to the falling edge of the TXCKI clock signal, and can be sampled on the following falling edge. This timing is compatible with the $Base_2$ Systems UGA-330-2 DS3/E3 framer, using the TXOVH output of that circuit to synchronize the UGA-210 input. The content of the frame bit position is undefined.

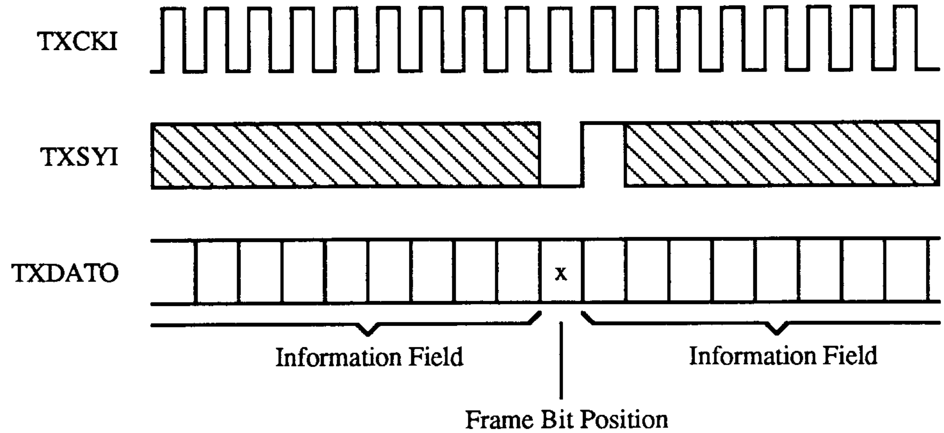


Figure 4.5. DS3 PLCP Transmit Timing

Figure 4.6 shows the transmit timing for the E3 PLCP. The clock signal TXCKI has a frequency of 34.368 MHz. The synchronization signal TXSYI has a rising edge after to the sampling of the last bit of the frame alignment signal. The data stream signal TXDATO is the output signal; it transitions in response to the falling edge of the TXCKI clock signal, and can be sampled on the following falling edge. This timing is compatible with the $Base_2$ Systems UGA-330-2 DS3/E3 framer. The frame alignment signal position is filled with the hex value CCCC; this value provides the four overhead bits required by ETSI T/NA(91)18 that follow the frame alignment signal defined by CCITT G.751.

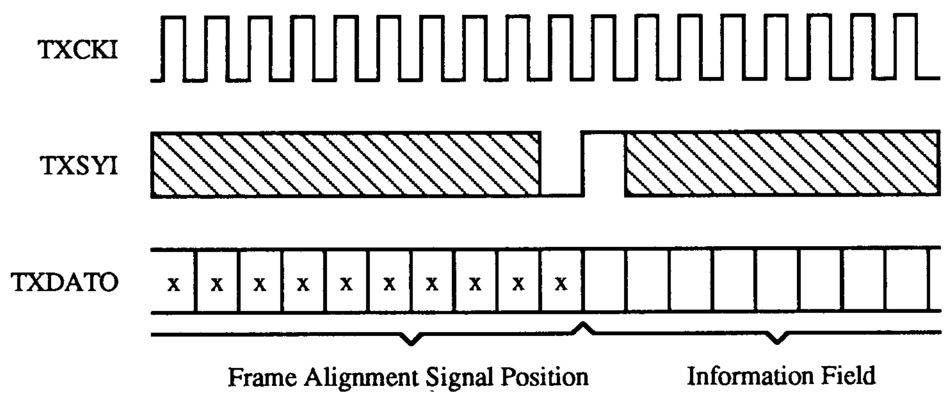


Figure 4.6. E3 PLCP Transmit Timing

The transmit PLCP provides a synchronization signal for the PLCP transmit frame on PLCPSYO. This signal is high for the first bit of each PLCP frame. This signal is used for synchronization of multiple SCARFs as described in section 4.11. A transmit PLCP slot synchronization signal is available on SLOTSYO. This signal is high for the first bit of each PLCP slot.

4.3. Framed PLCP Receive Interface

The PLCP receive inputs consist of the receive clock RXCKI, the receive synchronization RXSYI, and the receive data input RXDI.

The input timings are all similar; the inputs RXDI and RXSYI are sampled on the falling edge of the input clock, and the low-to-high transition of the synchronization signal occurs during the interval of the frame bit for DS1 and DS3, with the first bit of time-slot 0 for E1, and with the first bit of the frame-alignment signal for E3. For brevity, only the DS1 timing will be shown. Figure 4.7 shows this timing.

In all framed PLCPs, the content of the framing bit positions is ignored. The synchronization signal RXSYI does not need to be present every frame; it can be applied at any submultiple of the frame rate (e. g., once every DS1 ESF superframe for DS1).

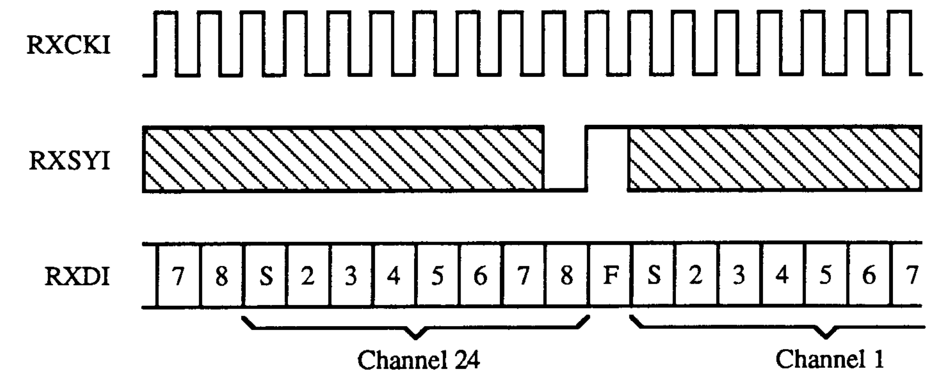


Figure 4.7. DS1 PLCP Receive Timing

4.4. Unframed PLCP Interface

The timing for the unframed interface consists of a clock input and a data output; the data is provided on TXDATO and a synchronization signal that is high on the first bit of each PLCP slot is provided at PLCPSYO. This provides a convenient reference for externally identifying the first octet of each slot for conversion of the framing octets required for SDS3 operation.

In unframed mode it is possible to provide L2_PDUs slots while ignoring PLCP overhead. This function is set by selecting E1 PLCP mode, which has no stuffing content. By setting Enable External PLCP Sync, Disable PLCP Framing, and Disable PLCP OOF, the external PLCP contents will be ignored by the receiver. The receiver is then synchronized by a signal that is high for the first eight bits of the PLCP slot. The functional timing requirement is shown in Figure 4.8.

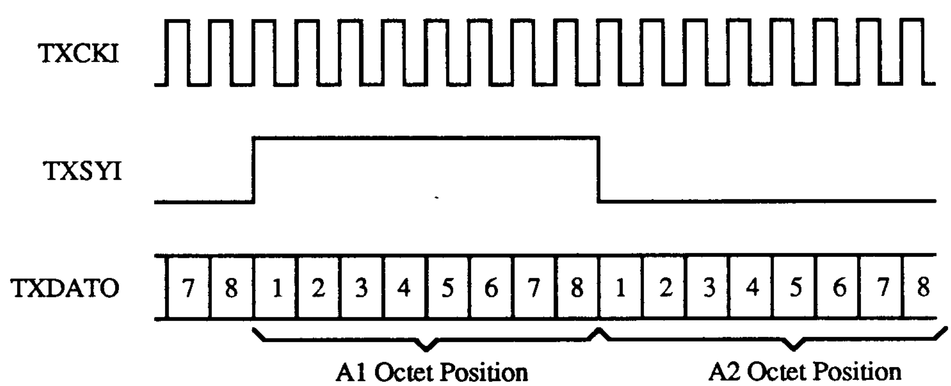


Figure 4.8. External PLCP Synchronization

The synchronization signal TXSYI must be high for the eight clock cycles during which the A1 octet bits are being clocked into the transmitter.

4.5. PLCP Overhead Generation

The PLCP overhead generation consists of the framing octets A1 and A2, the path-overhead identifier (POI) octets, and the path overhead octets. All of these are generated by the PLCP transmit circuitry, but can be selectively disabled if desired. These functions are also available in the segmentation bypass modes to control PLCP overhead generation.

The A1 and A2 octets are generated according to the sequence given in TR-TSV-000773. The POI octets are determined by the particular PLCP that is selected, but in each case consist of a slot count and one parity bit. The DS3 PLCP has twelve slots per frame, the DS1 and E1 PLCP have ten, and the E3 PLCP has nine. In each case the POI octets provide a backwards count of the PLCP slots in the frame, along with a parity bit.

All path overhead growth octets Zn and the path user channel F1 are forced to zero. The B1 octet is populated with a bit-interleaved parity code (BIP-8) that is calculated over each PLCP frame.

Figure 4.9 shows the individual bit functions of the Transmit BIP-8 Register TX_BIP8, located at address 02. This register controls insertion of BIP-8 errors in the generated PLCP. A non-zero value written to this register will invert the corresponding bits of the B1 octet from that calculated by the BIP-8 circuit in the following PLCP frame. This register will be cleared after each frame when the errors are inserted; the register can be read to determine if this has occurred, so that the local processor can insert BIP-8 errors as desired in each PLCP frame. This capability can be used to verify far-end FEBE operation.

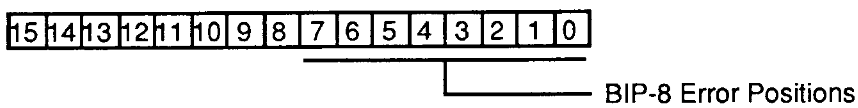


Figure 4.9. TX_BIP8 Register (address 02)

The G1 octet consists of three different fields. The first four bits of the field contain the FEBE code, which normally is derived from the BIP-8 error calculation, but which can be set to all-zeros, all-ones, or the received FEBE code by control bits in the RX_PLCP_CTRL register.

Figure 4.10 shows the individual bit functions of the M1 and M2 fields of Transmit PLCP Register M1_M2. This register is located at address 0B. This register specifies the M1 and M2 octets that are inserted in the transmitted PLCP.

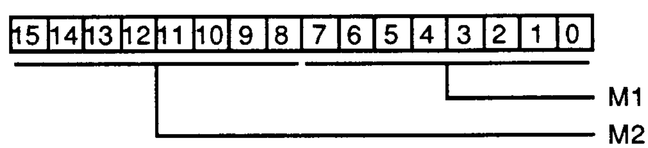


Figure 4.10. M1_M2 Register (address 0B)

4.6. PLCP Framing Operation

The PLCP receiver implements a framing state machine for the PLCP framing as described in TR-TSV-000773.

In framed mode, the PLCP receiver will process a serial stream to find PLCP framing, with octet synchronization provided externally in DS1, E1 and E3 modes and nibble synchronization in DS3 mode.

In unframed mode, PLCP framing is always done without an octet or nibble reference, and the framing counter output is not used.

Stuffing is provided according to the PLCP setting.

The PLCP framing state machine is given in Figure 12.4 of IEEE 802.6. Jam signal detection is not provided for this receiver, as there is no requirement for it in SMDS. Three states are present: in frame, out-of-frame, and loss of frame.

Valid framing is found when two consecutive valid path overhead octets in sequence are observed after the A1, A2 framing octets. Framing is "on line", as the framing content is very robust.

The out-of-frame (OOF) state is entered only from the in-frame state, when there are errors in both the A1 and A2 octets or when there are two consecutive Pn errors. This event is an "OOF event," and is counted. The loss-of-frame state (LOF) is entered after eight PLCP frames in the OOF state.

The PLCP_OOF output pin indicates that the receive PLCP is not in the in-frame state.

4.7. PLCP Frame Reference and Stuffing

In each PLCP mode, there is a transmit reference clock that is used to provide the implicit 8-kHz frame reference carried in the PLCP. In DS1 and E1 modes, this reference is simply carried in and determined from the frequency of the line clock.

In DS3 and E3 modes, the 8-kHz reference is derived from the average period of the PLCP frame. For the transmitter, this frame reference can be derived three ways: from the received PLCP frame, from an external 8-kHz reference that is obtained from pin 8KCKI, or from "default" stuffing, which effectively obtains the PLCP frame period from the line clock in a predictable manner.

The Force Default Stuffing in the PLCP_CTRL register will force the default stuffing function in either DS3 mode or DS1 mode. This stuffing technique for DS3 is described in IEEE 802.6, chapter 12; this results in a PLCP frame period of 124.995 µs for a DS3 clock rate of exactly 44.736 MHz. For E3, the technique used is described in ETSI standard T/NA(91)18; it will result in a frame period of exactly 125 µs for a line clock rate of 34.368 MHz.

The external frame reference is enabled by setting External 8-kHz Timing in the SYS_CONFIG control word. If this bit is not set, then the received PLCP will be used to establish the frame reference for the transmit PLCP.

The external 8-kHz reference applied to 8KCKI is used at the transmit PLCP for DS3 and E3 whenever the receive PLCP is in the LOF state or the Signaling Freeze input is high and it is enabled. While the received PLCP is OOF but not LOF (normally 1 msec) default stuffing will be provided.

4.8. PLCP Status Outputs

Status bit indications will be maintained for the following in PLCP_STATUS:

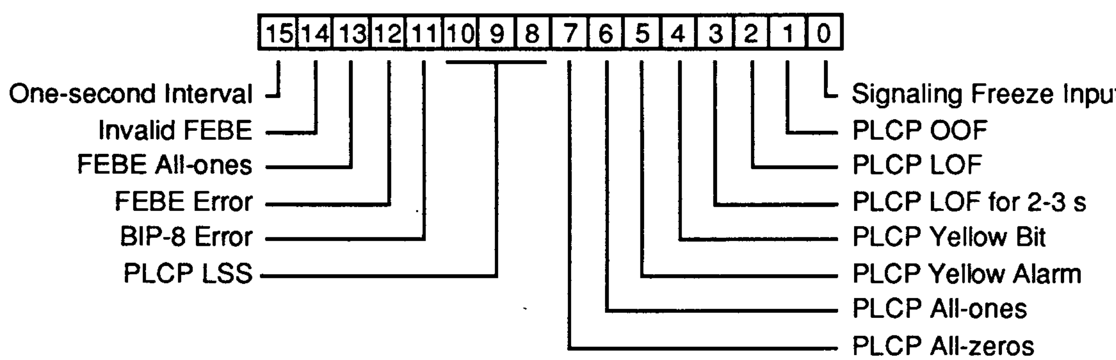


Figure 4.11. PLCP_STATUS Register (address 24)

There are two types of PLCP status indications. Conditions are reflected as a level indication. A positive condition will be latched until read, and then cleared unless it is still present. Events are latched until read and then always cleared. The only event indications in the PLCP_STATUS register are the error conditions BIP-8 Error, FEBE Error, FEBE All-ones, and Invalid FEBE, as well as the timing indication One-second Interval.

Signaling Freeze Input is the status of this input pin. The signaling freeze signal can be used to disable L2_PDU processing.

The PLCP framing state machine is defined in IEEE 802.6 Figure 12.4. PLCP OOF is set if the PLCP OOF state has been entered. It will be latched, and will continue to be read as one until valid PLCP framing is recovered. PLCP LOF is set when PLCP OOF is active for eight consecutive PLCP frames. PLCP LOF for 2-3 seconds is set if PLCP LOF is high for three consecutive one-second latching signals (rising edge on ONESECI). These are always reported as levels, describing the current state of the framer.

The PLCP Yellow Bit is updated with the value of the PLCP yellow alarm bit every PLCP frame. The PLCP Yellow Alarm status bit is set high after ten consecutive frames with a PLCP yellow alarm value of one and cleared after ten consecutive frames of a value of zero.

The PLCP LSS indication is based on the current state of the PLCP link status signal bits. If a bit in the PLCP link status bits has changed states, the corresponding bit in the PLCP LSS field is set. Each bit of the PLCP LSS field is treated like a separate status bit and is latched until read.

PLCP All-ones and PLCP All-zeros are set if two consecutive PLCP slots are all-zeros or are all-ones respectively. These indications can be used as AIS detection indications in E1, E3, and DS1 applications and as loss-of-signal detectors in all applications.

BIP-8 Error is set if there is an error in the BIP-8 code checking. FEBE Error is set if any valid non-zero FEBE value (values of 1 through 8) is returned. Invalid FEBE is set if any invalid FEBE value (9 through 15) is returned; a value of 15 will cause FEBE All-ones to be set. This value is used to indicate that the FEBE calculation is not supported at the far end of the circuit.

One-second Interval is set if the one-second timer input is detected. This input also latches the PLCP status counters and allows synchronization with the one-second timing function.

Each of these status bits is latched until read and then cleared if the condition is no longer present. If a status condition clears before the register is read, the status bit will still be held. Current status can be obtained by reading the register twice in succession.

4.9. PLCP Status and Counter Interrupts

The status interrupt pin STAT_INT can be programmed to provide an interrupt on any occurrence in the interrupt status register. Figure 4.12 shows the individual bit functions of the PLCP Status Interrupt Enable Register EN_PLCP_INT. This register is located at address 1E. This register enables interrupts on PLCP receiver status conditions.

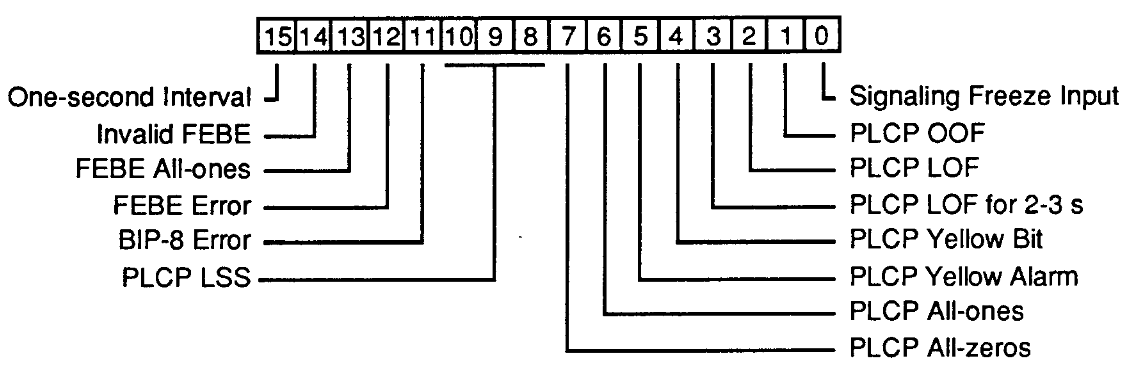


Figure 4.12. EN_PLCP_INT Register (address 1E)

Each of these signals will generate a receive status interrupt if the corresponding interrupt is enabled. The source of the interrupt can be determined by reading the INT_STATUS register at address 22; if bit 0 is set, an interrupt has occurred in the PLCP_STATUS register. Reading the PLCP_STATUS register clears the interrupt.

There are two types of interrupts provided. Alarm signals will provide an interrupt on change of state. Error signals will cause an interrupt on each occurrence of the error condition. The Error signals are BIP-8 Error, FEBE Error, and Invalid FEBE. The other signals are Alarm indications. The PLCP LSS bits enable an interrupt on a change of state in the corresponding PLCP link status signal bit.

Four counters are provided for PLCP error conditions; the addresses of these counters are given in Table 3. PLCP FERR is a count of errors in either the A1 octet or the A2 octet of each frame. PLCP OOF is a count of the out-of-frame events; these occur if either both the A1 and A2 octets are in error or if two successive path-overhead identifier octets are invalid and the previous state was in-frame. PLCP BIP and REM BIP are a count of the BIP-8 errors calculated and counted from the received FEBE bits, respectively.

Figure 4.13 shows the individual bit functions of the Counter Interrupt Enable Register EN_CNTR_INT. This register is located at address 1D. This register enables interrupts on error counter overflows. These counters are located at addresses 30-3F. All counters are sixteen bits. If a counter is set to interrupt, it will roll over to zero when it exceeds its maximum value. If a counter is not set to interrupt, it will saturate at its maximum value of 65535 and ignore further events.

To determine if an interrupt has been caused by a counter, the local processor first reads the INT_STATUS status register. If bit 1 of that register, Counter Overflow Interrupt, is set, then an interrupt is pending due to a counter overflow. The counter status register CNTR_STATUS at address 23 is then read to determine the source of the interrupt. The bit positions of the EN_CNTR_INT and CNTR_STATUS each refer to the same respective counters.

The interrupt is cleared when the CNTR_STATUS register is read. Note that the counter itself does not have to be read to determine its value, as the overflow that causes the interrupt resets the counter to zero.

If the interrupt for a particular counter is not set, the counter will saturate at a value of 65535 and will stay at that value until read. If Enable One-second Latching of PLCP Counters is set, then at each one-second interval defined by the input ONESECI, the current counter value will be latched for the following one-second interval and the counter will be cleared. If the counter is again read in that one-second interval, the current value of the counter will be read and the counter will be cleared.

The other counters shown in EN_CNTR_INT are associated with the reassembly operation and are described in section 7.11.

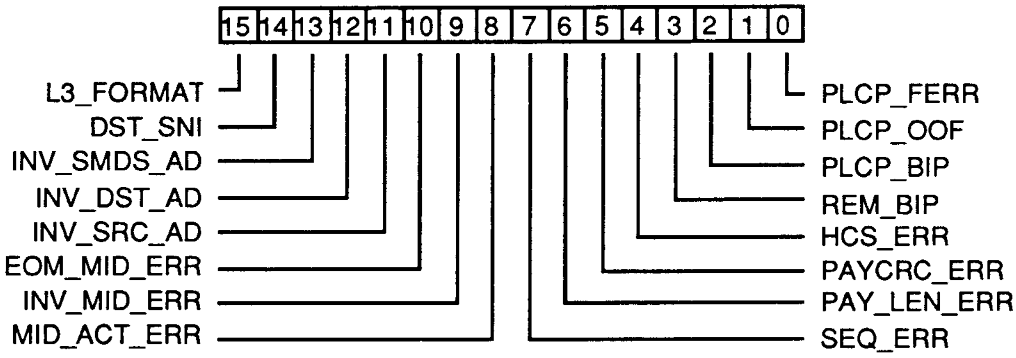


Figure 4.13. EN_CNTR_INT Register (address 1D)

4.10. PLCP Transmit/Receive Synchronization

The PLCP block must transmit segments at the same rate at which they are received. For DS1 and E1, long-term synchronization of the bit clock rates will establish this. For DS3 and E3 rates, the payload data rate is independent from the line rate, and a separate timing/synchronization mechanism is required.

The DS3 and E3 PLCPs both have a 125-µs frame. The reference clock for this frame is taken from the received signal, or alternatively from an external reference. In either case, the transmit circuit will generate one PLCP frame per reference frame.

4.11. Multiple PLCP Synchronization for SCARF Multiplexing

It is possible to configure two or more SCARFs together to provide synchronized PLCPs that can access a single framer, and thus multiplex different services or hosts to a single SMDS or other cell-based service access point. This mode is enabled by setting the Enable SCARF Synchronization bit in the SYS_CONFIG register. Examples of services that can be provided in this application are multiplexing of isochronous and connectionless data or multiplexing of connectionless data from multiple sources in "cluster" arrangements.

Figure 4.14 shows the required configuration of the inputs and outputs as well as the control circuitry. The receive signals from the framer are connected to all three SCARFs. Message selection or slot selection for selecting proper input signals can be accomplished with screening on slot type bits, virtual channel identifiers, or address screening. These features are described in sections 7 and 8.

In the transmit direction, the output signals are synchronized and combined using an exclusive-or circuit. This circuit allows the correct BIP-8 code to be calculated on the transmit stream for any PLCP. The control of the multiplexing is provided by the MUXPRIN and MUXPROUT multiplex priority signals. If the MUXPRIN signal to a SCARF is high, it sets MUXPROUT high if it has no traffic to send. If it does have traffic to send, it sends one L2_PDU and then sets MUXPROUT high on the next slot. By chaining the inputs and outputs of the multiplexed part as shown in Figure 4.13, alternate slots will be used by SCARF ICs with L2_PDUs to send. For isochronous data, the MUXPRIN input to the SCARF is set high each time a slot is required for isochronous traffic and the MUXPRIN to the SCARF carrying connectionless traffic is forced low at the same time. Other arrangements are possible with simple logic; no local processor intervention is required.

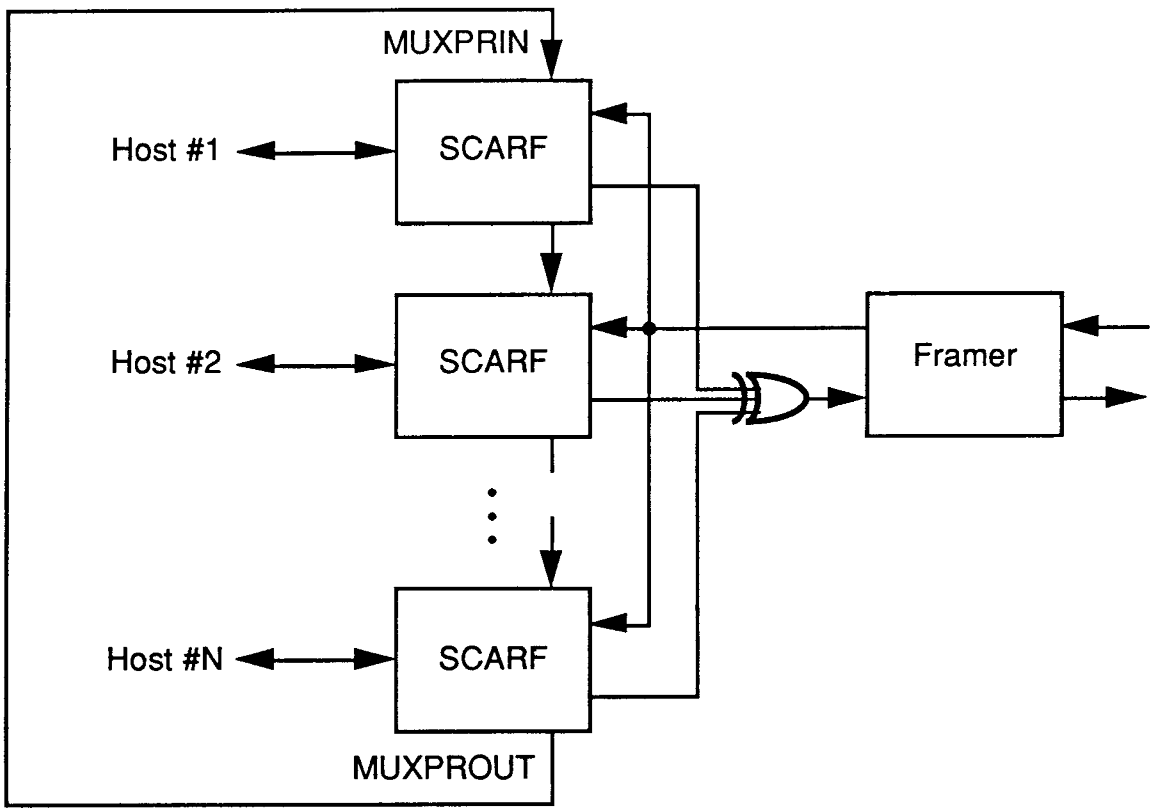


Figure 4.14. SCARF Multiplexing

The transmit PLCPs of all SCARFs must be synchronized as shown in Figure 4.15. The master SCARF provides a PLCP frame synchronization signal on the PLCPSYO pin. This synchronization signal is used by slave SCARFs by connecting it the CK8KI input and setting the External PLCP Transmit Sync bit in the PLCP_CTRL register on each slave SCARF.

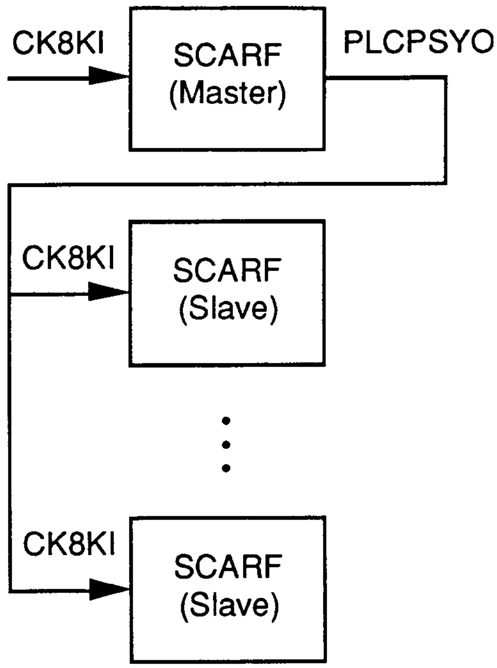


Figure 4.15. SCARF Multiplexing

5. HOST INTERFACE AND FUNCTIONS

The host interface controls the transfer of data to and from the SCARF. Multiple modes are provided for transfer of both L3_PDUs and L2_PDUs. Provision is made for connection to data buses, to clocked-octet interfaces, and to serial HDLC formats.

The host interface supports the transfer of L3_PDU messages with selected L3_PDU overhead, L2_PDU slots (without the HCS octet), or L2_PDU segments. A "dummy" HCS octet can be provided on output and the HCS octet can be ignored on input if required. Transfer of messages and validation of them is under the control of stack pointers. These functions are described in sections 6 and 7.

Figure 5.1 shows the individual bit functions of the Host Interface Control Register HOST_CTRL. This register is located at address 0A. This register controls the host interface type and disables L3_PDU overhead transfer.

Control bits 1 and 0 select the Host Mode. There are four modes that can be selected. Bus Interface mode selects a mode in which all data transfers to and from the host are unidirectional on a bus. The bus control is generally provided by an external adapter circuit. A maximum transfer rate of 33 Mbyte/s is supported. Message transfer is coordinated with control signals to the bus interface.

Octet Interface provides bidirectional transfer. Control signals are provided in optional modes to allow the expansion of the octet transfer to 16 or 32 bits. Message transfer is coordinated with enable and status signals on the control pins.

Serial HDLC mode provides a serial interface that provides the core functions of the CCITT Q.921 LAPD protocol, with optional CRC generation and checking. Zero-bit insertion is provided.

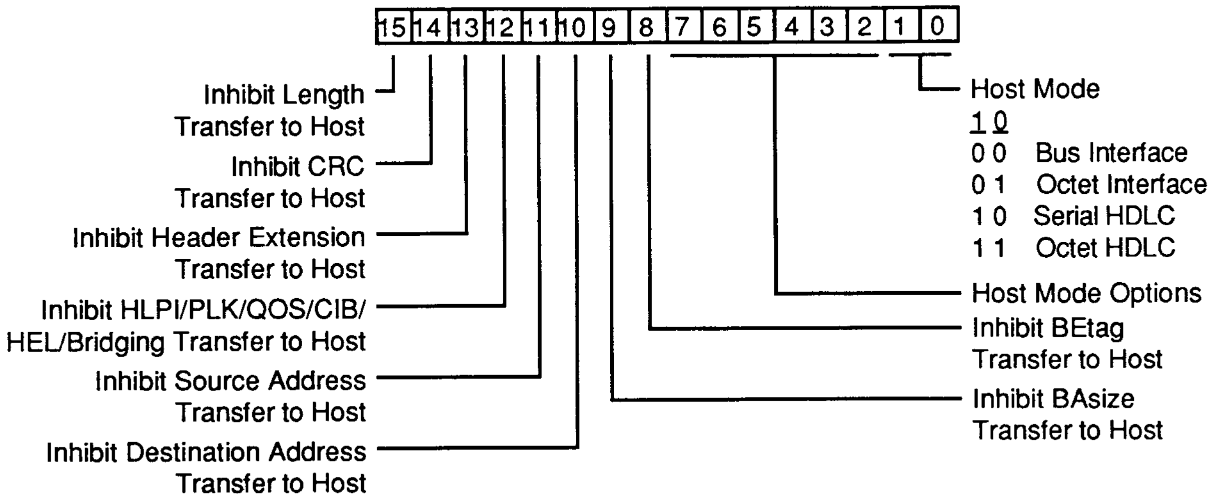


Figure 5.1. HOST_CTRL Register (address 0A)

Octet HDLC mode provides an octet-based HDLC link from the Base2 Systems UGA-330-2 DS3/E3 framer. This framer can be operated with or without framing overhead and provides zero-bit insertion for transparency and optional 16-bit or 32-bit CRC.

The Host Mode Options field provides control bits that are specific to the particular host mode selected. In Bus Interface mode, a host loopback function is provided.

Bits 8-15 selectively disable L3_PDU overhead transfer to the host.

5.1. Bus Interface Modes

Bus interface options are provided to allow transfer of messages across either an EISA bus or a VME bus. In each case the host interface connects directly to a part that implements a bus controller. The EISA bus interface is realized with the Intel 82355 Bus Master Interface Controller (BMIC). The VME bus interface uses the Cypress VIC068.

The control bits for the bus interface mode are as follows:

Bit #	Function
2	Host Loopback
3	EISA Bus
4	VME Bus Interface
5	Local Processor Host Mode
6	Read Reassembly Buffer
7	Load Segmentation Buffer

5.1.1 EISA Bus Interface

The Intel 82355 Bus Master Interface Controller can be used to connect SCARF to an EISA bus. In this mode, the SCARF will provide a maximum data rate of 33 Mbyte/s. The EISA bus clock should be used as the system clock for the SCARF in this mode.

The local processor for the SCARF will also operate as the local processor for the BMIC.

The 16 data pins of the BMIC are connected to HST_DAT15-0. The control pins that are used are as follows:

SCARF Input	BMIC Output	Function
HST_IN0	TLD#	Transfer Address Load
HST_IN1	TRQ#	Transfer Request
HST_IN2	TEOP#	Transfer End-of-Process
HST_IN3	TDIR	Transfer Direction

SCARF Output	BMIC Input	Function
HST_OUT0	TCLK	Transfer Clock
HST_OUT1	TACK#	Transfer Acknowledge
HST_OUT2	TDOE#	Data Output Enable

For transfer of data from the EISA bus to the host, the BMIC will transfer a message in a single message block. The host interface will respond to a transfer request by noting the direction of the transfer, providing acknowledgement, and reading the data as presented on each TCLK cycle. If the data overruns the segmentation buffer or maximum message length (9232 or 65,532 octets depending on the value of the Disable SMDS Length Limit bit in the TX_PROT register), the message transfer is aborted and the message is lost. For L3_PDU transfers, message length is variable. For pipeline modes, the message length must be 52 octets for L2_PDUs and 48 octets for segments.

For the transfer of reassembled messages, the transfer of a message from the SCARF to the EISA host must be done in a single message transfer. For this to occur the EISA host must know that a message is ready and the length of the message. The Reassembly Complete interrupt in the EN_STK_INT register indicates that a message is ready to be output. After a Reassembly Complete interrupt has been received, the message length may may read from the RSM_LNGTH register (address 26). This information can be passed on a message by message basis by the local processor through the "doorbell" and "mailbox" utility registers of the BMIC IC.

5.1.2. VMEbus Interface

A VMEbus interface to SCARF can be implemented with a Cypress VIC068 VMEbus Interface Controller chip. The 64-MHz clock required by the VIC068 may be divided by two to supply the SCARF system clock but this is not a requirement. The Local Processor to the SCARF will act as processor to the VIC068. The VIC068 is specifically designed to work with Motorola 680X0 processors but also may be used with other processors.

The sixteen data pins, HST_DAT15:0, may be connected to either the high or low 16 bits of the VMEbus through bidirectional latching transceivers. The data transferred to and from the SCARF need not flow through the VIC068. Required command input and output pins are as follows:

SCARF Input	VIC068 Output	System Output	Function
HST_IN0	BLT*	-	Block transfer mode
HST_IN1	DS*	-	Data Strobe
HST_IN2	R/W*	-	Read/Write select
HST_IN3	-	/CS	Chip Select
HST_IN4	-	ABORT	Optional Abort input

SCARF Output	VIC068 Input		Function
HST_OUT0	DSACK*		Data strobe acknowledge

Note: The /CS signal is active low and is a combination of PAS* and the address of the SCARF I/O port in the VME address space. ABORT is active high and can be used to kill a message which has been transferred wholly or in part to the SCARF due to VMEbus error etc. If ABORT is brought to a logic 1 before /CS is removed, the message just loaded will be aborted. In systems not requiring the abort feature, this input should be connected to ground.

Both single slave read/writes and block transfers of unlimited burst size in either direction are supported. Maximum block transfer rates are on the order of 16 MBytes/sec for 16-bit VMEbus transfers. Since the host interface is essentially a single-address port, there is no need to interrupt bursts on 256-byte boundaries on the local side.

5.1.2.1. VMEbus Message Reassembly

To read out a completely reassembled L3_PDU the Read Reassembly Buffer control bit 6 of HOST_CTRL is used. A typical control sequence is as follows:

1. Enable Reassembly Complete interrupt (bit 8) in the EN_STK_INT register.

2. When this interrupt occurs read the L3_PDU length from the RSM_LNGTH register. Set the Read Reassembly Buffer bit high.

3. Load the RSM_LNGTH value minus any header/trailer to be inhibited into the VIC068 Block Transfer length registers 0 & 1 ($db,$df).

4. Set up the block transfer address on the local side to decode a SCARF /CS and the proper VMEbus write address. Enable the VIC068 DMA Complete interrupt.

5. Program the VIC068 to do the block transfer.

6. When the transfer is complete, the VIC068 will generate an interrupt which the Local Processor will respond to by clearing the Read Reassembly Buffer bit in HOST_CTRL.

As an option, instead of using the predetermined length in block transfer mode, the VIC068 can read consecutive words until the HST_MSG_OUT bit 15 of STK_STATUS generates an interrupt to which the Local Processor can respond.

5.1.2.2. VMEbus Message Segmentation

To transfer an L3_PDU from VMEbus to the SCARF for segmentation, the Load Segmentation Buffer bit 7 of HOST_CTRL is used. A typical control sequence is as follows:

1. The Local Processor is notified of a pending message to be sent, along with its length and starting VMEbus address, and sets the Load Segmentation Buffer bit in HOST_CTRL.

2. The Local Processor loads the length of the L3_PDU to be transferred into the VIC068 block transfer length registers, sets up the local SCARF address, the VMEbus read address, and tells the VIC068 to start the transfer.

3. Once the transfer is complete, the Local Processor responds to the DMA finished interrupt generated by the VIC068 and clears the Load Segmentation Buffer bit of HOST_CTRL.

4. The Host Interface then starts segmentation of the L3_PDU automatically.

L2_PDUs or Segments can be transferred in a similar manner.

5.1.3 Local Processor Host Mode

The Local Processor Host mode is a Bus Interface mode that allows the local processor to function as the host. No host interface data pins are used in this mode. The local processor uses the host interface circuitry as a resource to simplify the transfer of data.

This configuration will support the "burst mode" operation of the Intel 80960-series of microprocessors to burst rates of 25.6 Mbyte/s. For this mode, the CLK2 input of the 80960SA or the CLKIN input of the 80960CA

(CLKMODE must be set to divide CLKIN by two to obtain PCLK) should also be connected to the SYSCKI input of the SCARF.

This mode can support transfer of L3_PDUs, L2_PDUs, or segments, using any of the segmentation or reassembly modes. Transfers in the reassembly direction are supported by interrupts.

To segment and transmit an L3_PDU the Load Segmentation Buffer control bit is used to delineate messages.

1. Set the control bit Load Segmentation Buffer. This primes the host interface to load an L3_PDU for segmentation.

2. Write the L3_PDU content as required to address 48. In burst mode, up to eight 16-bit words or 16 octets can be written in one burst. The L3_PDU content will be written to the required segmentation buffer locations.

3. Clear the Load Segmentation Buffer control bit. This will cause the Host Message Input status bit to be set and will cause an interrupt if this interrupt is enabled (it need not be). The segmentation block then initiates segmentation by loading the stack locations and incrementing the stack pointer as described in section 6 below.

When burst mode transfers are used, the low-order address bits of the address are ignored. Thus the write address for segmentation can be any address in the range 48 to 4F.

For segments or L2_PDUs, the proper length slot should be written while the Load Segmentation Buffer bit is high.

Transfer of reassembled L3_PDUs is controlled by interrupts. Each reassembled message results in an indication in the STK_STATUS Reassembly Complete status bit. This indication will not be provided until address screening and the L3_PDU 32-bit CRCs are completed.

The steps for providing message transfer are as follows:

1. Wait for a Reassembly Complete status indication on the STK_STATUS control word. This status bit can be enabled to provide interrupts.

2. Read the message length from the RSM_LNGTH register

3. Set the Read Reassembly Buffer control bit in the HOST_CTRL register.

4. Read the L3_PDU from address 48. Each read will provide two octets of the message; overhead fields can be inhibited by control bits in the HOST_CTRL register.

5. When the end of the L3_PDU is read, the Host Message Output status bit will be set. It may be enabled to cause an interrupt. If the concurrent 32-bit CRC check is enabled, the Concurrent L3_PDU CRC Failure status bit will give the status of the L3_PDU. Therefore, the STK_STATUS register should be read, which will clear both of these indications.

6. Clear the Read Reassembly Buffer control bit in the HOST_CTRL register

For L2_PDU reception, an interrupt is provided each time an L2_PDU is received.

5.1.4 Host Loopback

In this mode, the SCARF internally connects the reassembly process output to the segmentation input. Host Loopback can be used for testing or for configuring an arrangement to provide reassembly of messages in both directions. Only compatible segmentation and reassembly modes can be accommodated in this mode; the information transmitted must be in identical formats. No CRC or FCS functions are supported in Host Loopback mode.

5.2. Octet Interface Modes

The octet interface modes allow the connection of the SCARF directly to dual-port RAMs, FIFO RAMs, and other similar circuits.

The control bits for this mode are:

Bit #	Function
2	AMD TAXI™
3	Ignore ACK
4	Mark Last Word
5	Insert/Delete HCS Octet
6	Word Width (LSB)
7	Word Width (MSB)

The Insert/Delete HCS Octet mode is available to convert 53-octet L2_PDUs to 52-octet PDUs for RAM storage in L2_PDU pipeline mode. If this bit is enabled, the fifth octet of each received message is discarded. The SMDS HCS octet value of "22" is inserted in the fifth octet of each transmitted message, thus restoring the HCS octet to SMDS L2_PDUs.

5.2.1 TAXI Mode

If the TAXI control bit is set the SCARF will connect directly to AMD TAXI serial communications ICs; the Mark Last Word and Word Width control bits are ignored. The SCARF can be connected directly to the serial transmission link and supports payload data rates above 130 Mbit/s in both directions simultaneously; the interface is designed to allow straightforward multiplexing of multiple low-speed SCARF circuits to a single transmitter/receiver pair. This mode is useful for transmission to a remote host in both CPE and switching applications.

There are two clocking modes for the TAXI mode. For full-speed operation, the TAXI can be synchronized to the SCARF IC. In this mode, the system clock input to the SCARF must be twice the frequency of the TAXI byte clock. In this case control bit 3 should be set, so that the ACK signal from the TAXI receiver is ignored. In slower TAXI applications, control bit 3 should be cleared and the ACK input from the TAXI receiver connected as shown below.

The required inputs from and outputs to the TAXI Transmitter are:

SCARF Input	Function
HST_IN0	Output High-Z
HST_IN1	Acknowledge (ACK)

SCARF Output	Function
HST_DAT15-8	Transmit Data
HST_OUT0	Strobe (STRB)
HST_OUT1	End Message Marker (to Command Input or High-order Data Input)

The outputs to the TAXI transmitter are one byte of data, a strobe signal indicating data is present, and an End Message Marker which is high for at least one active strobe cycle at the end of a message. This signal allows the command channel of the TAXI connection to be used to delineate L2_PDU or L3_PDU messages.

The Acknowledge input is a "handshake" response from the transmitter indicating that it is ready to accept another byte of data. This can be useful in applications where the bandwidth of the TAXI chip is smaller than the peak bandwidth of the host interface, or where a multiplexed interface is not ready to accept data. The Output Hi-Z input will force the Transmit Data bus to high-impedance. This is also useful for multiplexing multiple SCARFs to a single serial link to a remote host.

The required inputs from the TAXI Receiver are:

SCARF Input	Function
HST_DAT7-0	Receive Data
HST_IN2	Data Strobe (DSTRB)
HST_IN3	Violation (VLTN)
HST_IN4	End Message Marker (from high-order data or Command bit and strobe)

The Data Strobe input indicates that data is present on the data bus. The Violation output indicates that the data word received was in error, and will result in an abort of the message being loaded to the host; the message will be ignored. The End Message Marker indicates that the octet just received was the last one in a message. This signal would normally be provided by decoding the command signal and the command strobe CSTRB. Consecutive End Message Markers (with no DSTRB inputs between them) will be ignored.

5.2.2 Octet Expansion Mode

In this mode, the SCARF provides a general octet-oriented interface to FIFOs and dual-port RAMs. This mode is useful to provide very-high speed bus interconnection to SCARF. Segmentation Data refers to data being transferred to the SCARF for segmentation and Reassembly Data refers to reassembled L3_PDUs transferred from the SCARF.

The host interface pin connections are:

SCARF Input	Function
HST_DAT7-0	Segmentation Data
HST_IN2	Segmentation Data Marker
HST_IN3	Reassembled Data FIFO Full
HST_IN4	Segmentation Data FIFO Empty

SCARF Output	Function
HST_DAT15-8	Reassembled Data
HST_OUT0	Segmentation Data Strobe
HST_OUT1	Reassembled Data Strobe
HST_OUT2	Reassembled Data Marker
HST_OUT3	Segmentation Data Select 0
HST_OUT4	Segmentation Data Select 1
HST_OUT5	Reassembled Data Select 0
HST_OUT6	Reassembled Data Select 1

Transfer of information in both directions is always clocked by the SCARF host interface using the data strobe signals. In the segmentation direction, the Segmentation FIFO Empty input will inhibit the Segmentation Data Strobe. In the receive direction, the Reassembly FIFO Full input will inhibit the Reassembly Data Strobe. These control bits can also be used to inhibit data transfers in dual-port RAM designs as well. The FIFO Full and FIFO Empty control bits and Data Strobes are all active low.

The Word Width control bits specify whether the interface is one, two, or four octets wide. The coding is both bits 6 and 7 cleared for one octet, bit 6 set for two octets, and bit 7 set for four octets. If the interface is set for one octet, the data select outputs can be ignored. If the interface is set for two octets, Data Select 0 will be low for the most significant octet and Data Select 1 will be low for the least significant octet. If the interface is set for four octets, the octet number being transferred is indicated by the two select pins with a value of 0 (Data Select 0 = 0, Data Select 1 = 0) for the most significant octet, a value of 1 (Data Select 0 = 1, Data Select 1 = 0) for the second octet, a value of 2 for the third octet, and a value of 3 for the least significant octet. The select outputs must be decoded externally with a dual 2-input-to-4-output demultiplexer.

The Mark Last Word control bit forces the Reassembled Data Marker signal high on the last octet of each segment, L2_PDU, or L3_PDU transferred. If this bit is not set, the Reassembled Data Marker bit is high on the first octet. Segmentation data must have the last word marked.

5.3. Serial HDLC Mode

This mode is provided to allow transfer of messages using HDLC formatting. The core functions of the CCITT Q.921 LAPD protocol are provided. The frame-check sequence (FCS) for reassembled messages must be generated in the reassembly buffer before transfer; this function is performed by the host interface circuitry according to the options set in the RX_CTRL register described in section 7.1.

FCS checking of messages for segmentation is provided as a part of the segmentation address screening function, as described in section 6.5.

The only HOST_CTRL bit used in Serial HDLC mode is bit 2 which causes abort sequences to be sent on the Reassembly Output Data pin until the control bit is cleared.

The required pin connections for serial HDLC transfer are:

SCARF Input	Function
HST_IN0	Clock for Segmentation Input Data
HST_IN1	Clock for Reassembly Output Data
HST_DAT0	Segmentation Input Data

SCARF Output	Function
HST_DAT8	Reassembly Output Data

Protocol errors such as non-integral number of octets and abort sequence detected are indicated by the External Host Error status bit in the INT_STATUS register.

Detailed timing requirements for this interface are given in section 9. This interface is recommended for operation at DS1 and E1 clock rates only, as the "off-line" calculation of CRC may substantially increase latency for message processing at higher transfer rates.

5.4. Octet HDLC Mode

This mode of operation allows the use of the Base2 Systems UGA-330-2 as an HDLC formatter for bidirectional transmission. This IC can be used with DS3 framing (M13 or C-bit parity formats), E3 framing according to G.751, and unframed. This circuit will operate to a clock rate of 52 MHz and can be connected to an HSSI interface.

The UGA-330-2 is connected to the same local processor that controls the SCARF IC. The UGA-330-2 can be optioned to generate a 16-bit or a 32-bit CRC.

No control bits are required to define options in this mode.

The control bits for the Octet HDLC mode are as follows:

Bit #	Function
2	Send Abort
3	Send FCS

The required pin connections are:

SCARF Input	UGA-330-2 Output	Function
HST_DAT7-0	RDAT7-0	Receive Data
HST_IN0	IDLE	Receive Link Idle
HST_IN1	VALFCS	Receive Message FCS Valid
HST_IN2	RXBCK	Receive Byte Clock
HST_IN3	TXBCK	Transmit Byte Clock

SCARF Output	UGA-330-2 Input	Function
HST_DAT15-8	TDAT7-0	Send Data
HST_OUT0	SNDMSG	Send Message Control
HST_OUT1	SNDFCS	Send FCS Control

The Send Abort control bit will command the UGA-330-2 to generate abort signals until the control bit is cleared. When the SCARF is in reassembly DXI mode (RX_CTRL bit 8), an FCS sequence is always generated by the UGA-330-2. If the SCARF is not in reassembly DXI mode, an FCS sequence is only generated by the UGA-330-2 when the Send FCS control bit is set.

Aborted messages, messages with a non-integral number of octets, or messages with invalid FCS are detected in the SCARF and generate a status signal on the External Host Error status bit. The message is discarded.

6. SEGMENTATION PROCESS

Segmentation refers to the subdividing of level 3 messages, or L3_PDUs, to segments that are transmitted within level 2 slots, or L2_PDUs. The SCARF provides modes that perform this segmentation function as well as modes that just pass L2_PDUs or segments.

There are six segmentation modes. Two test modes allow the generation of repeating PLCP frames or L2_PDUs from buffer RAM. Two pipeline modes allow either 52-octet L2_PDUs or 48-octet segments to be transferred from the host. The L2_PDU is transferred across the host interface with or without the header check sequence (HCS) overhead, and the HCS is calculated and inserted by the SCARF. The payload CRC can either be inserted or checked and transferred without modification. Both the HCS and the payload CRC can be optionally disabled or errored on a single-event basis. Two modes are provided for L3_PDU segmentation; the L3_PDUs can be segmented either after the complete L3_PDU arrives from the host or on a segment-by-segment basis, as the host transfers segments.

The segmentation process operates either autonomously or under control of the local processor. In autonomous mode, messages are forwarded automatically; local processor control allows them to be sent one by one. Local Processor control can allow per-message processing of message content or overhead by the local processor, as well as message insertion by the local processor.

The segmentation process provides formatting checks in two instances. It can provide an address screen function; this function is described in section 8. When the data exchange interface (DXI) mode is used at the host, the SCARF will also recognize management messages directed to the local processor and inhibit transmission of those messages.

6.1. L2_PDU Generation Control

Figure 6.1 shows the individual bit functions of the L2_PDU Transmission Control Register TX_L2_CTRL. This register is located at address 03. This register controls L2_PDU generation in the message segmentation section of the SCARF.

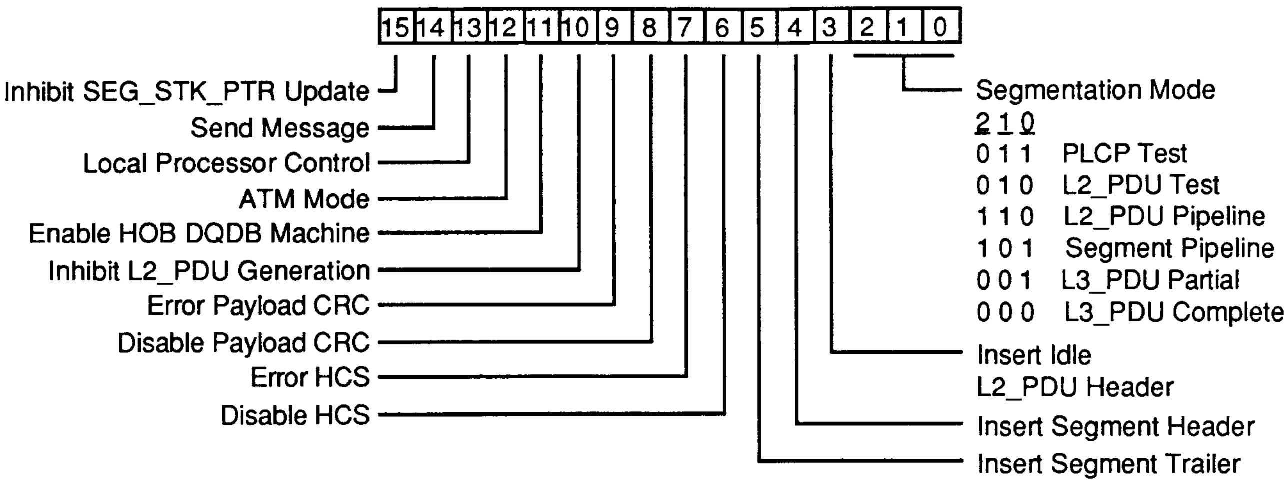


Figure 6.1 TX_L2_CTRL Register (address 03)

PLCP Test allows the generation of the entire message including the PLCP layer from buffer RAM. L2 PDU Test allows the same for 53-octet L2_PDUs. These modes allow the construction and generation of test signals to test the behavior of receivers to particular sequences. The messages are loaded from the local processor directly to RAM.

L2 PDU Pipeline mode forwards 52-octet slots from the host. In L2 PDU Pipeline mode, the L2_PDU overhead for active octets is provided from the host; only the HCS is provided by SCARF. The segmentation buffer runs from 2000 (hex) to one less than four times the value loaded in TX_L3_CTRL; normally this value would be the largest multiple of 13 that fits in the segmentation buffer allocation. When the buffer is full, it will "roll over" to 2000 (hex). In this mode, the L2_PDU overhead for active channels is provided as a part of the L2_PDUs that are transferred from the host. The HCS is calculated at the time the L2_PDU is transmitted and inserted in the L2_PDU according to the Disable HCS and Error HCS control bit settings described below.

Segment Pipeline mode (48-octet) operates like L2_PDU mode. The L2_PDU header overhead is taken from RAM addresses 98 and 99. Idle slot L2_PDU and segment overhead can be taken from RAM, depending on the setting of bits 3, 4, and 5 of the TX_L2_CTRL register. The host transfers 48-octets of information at a time, and the segmentation block inserts them as the final 48 octets of an L2_PDU.

There are two L3_PDU segmentation modes. In L3 PDU Partial mode, the segmentation process starts as soon as the host interface has started transferring the message to buffer RAM. In L3 PDU Complete mode, the entire message must be in RAM before the segmentation process is started. In partial message mode, only the first segment of the message must be in the buffer before transmission is initiated; the BAsize field is used to determine the length of the message for transmission and therefore must be present for this mode to be used. In both of these modes, message transmission is controlled by the segmentation stack process. The only functional difference in the two modes is that in partial mode the host block increments its pointer as soon as the first segment is loaded to the buffer and the segmentation block depends on the BAsize field to determine the length of the message for transmission.

Insert Idle L2 PDU Header allows the L2_PDU header for idle L2_PDUs to be inserted from RAM; if this bit is not set, the header of an idle L2_PDU is all-zeros. In L2 PDU Test and L2 PDU Pipeline modes, if this bit is set all overhead for idle L2_PDUs (which can be generated either because L2_PDU generation is inhibited or because the segmentation buffer is empty in Pipeline mode) is read from buffer RAM.

Similarly, Insert Segment Header and Insert Segment Trailer cause these fields to be read from RAM addresses that depend on whether the L2_PDU is active or not. If sent, the payload CRC field is either filled from RAM or generated by segmentation process, depending on the Payload CRC control bits. The MID field is always read from a location in RAM.

Disable HCS and Disable Payload CRC disable the field generation and allow the existing field to pass. Error HCS and Error Payload CRC forces an error in the generated field on the next busy slot after the control bit is set. The "Error" functions are cleared when the error is generated. This allows the local processor to easily generate a specific number of errors. Note that the header check sequence is contained in the fourth octet of the Network Control Information field.

Setting both Disable Payload CRC and Error Payload CRC in either Pipeline mode causes the existing payload CRC field in the L2_PDU to be checked for errors instead of generating a new field value. Any CRC errors are counted in the L3_PDUs-transmitted-counter L3_TX_CNT. This check capability is available only in L2 PDU Pipeline and Segment Pipeline modes and will be performed on all segments whether or not they are empty (an empty segment will contain all zeros which results in a valid CRC).

Inhibit L2 PDU Generation will stop the transmission of L2_PDUs. This function can be used for initialization of multiplexed SCARFs or can be used for test purposes.

Enable HOB DQDB State Machine enables the head-of-bus DQDB state machine that is described in TR-TSV-000772, section 4.2.2.2. This machine does not function in the Test modes, but can inhibit L2_PDU transmission in all other modes.

ATM Mode causes the HCS to be calculated on octets 1-4 of the L2_PDU header instead of octets 2-4. This feature is useful if the SCARF is being used to provide PLCP and level 2 functions in ATM networks.

Local Processor Control allows the local processor to control the transmission of L3_PDUs or L2_PDUs depending on segmentation mode on a message-by-message basis. In this mode, an interrupt will be generated each time a segment or L2_PDU is ready for transmission in Pipeline Mode or an L3_PDU is ready for transmission in L3_PDU mode. This interrupt is bit 6 of the STK_STATUS register, described in section 6.5.3. Setting Send Message, which is an unlatched control bit, will cause one pending message (L2_PDU in Pipeline modes or L3_PDU in L3_PDU modes) to be sent.

Inhibit SEG STK PTR Update has similar functions in both L3_PDU modes and in the pipeline modes. In either L3_PDU mode, it inhibits the incrementing of the segmentation stack pointer at the beginning of the transmission of an L3_PDU. This control bit can be used to allow a single message to be transmitted repeatedly and is used to control the transmission of a message that is loaded into the segmentation buffer from the local processor. In either pipeline mode, if Local Processor Control is enabled, this control bit can be used to allow a single segment transmission to be repeated each time that the Send Message bit is set. If Inhibit SEG STK PTR is set and Local Processor Control is not set, all of the segments that are in the segmentation buffer (the segmentation buffer is the address space between 2000 (hex) and the value in the TX_L3_CTRL register) will be transmitted repeatedly in sequence.

A separate control register is provided for the bandwidth balancing modulus BWB_MOD; a value one less than the desired bandwidth modulus is written to the register. This function is not required for SMDS service, but is a part of the IEEE 802.6 DQDB state machine; it is invoked when the Enable HOB DQDB Machine control bit is set. This register is shown in Figure 6.2 and is located at address 0F.

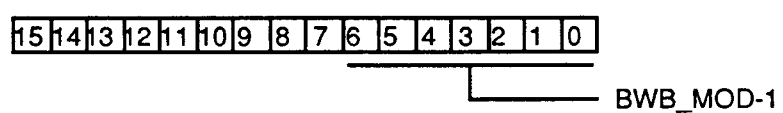


Figure 6.2 BWB_MOD Register (address 0F)

The transmission of L2_PDUs can be limited in rate to an access class. Access classes are defined in TR-TSV-000772, section 4.3. This feature is implemented for segmentation by setting both the Enable Access Class and Enable Segmentation control bits (bits 0 and 1 respectively) in the ACCESS register at address 12 (see figure 7.6). The operation of this function is described in section 6.5.2.

6.1.1. Segmentation Bypass Mode Control

This section describes the use of the TX_L2_CTRL bits in the Segmentation Bypass Modes that are defined in section 3.1.

In each of these modes, the payload CRC bits are generated and inserted if Disable Payload CRC is not set. If this bit is set, the bits in this field that are input on the host pins are transmitted. If Disable Payload CRC is not set, the Error Payload CRC control bit can be used to force errors in the payload CRC under local processor control.

The header check sequence is under control of the Disable HCS, Error HCS, and ATM Mode control bits. If Disable HCS is not set, the header check sequence is generated by the circuit and inserted in the output. In this mode the coverage of the HCS is determined by the setting of the ATM Mode control bit and the HCS can be errored by setting Error HCS. If Disable HCS is set in PCLP Insertion Mode or L2_PDU Insertion Mode, the external input bits are inserted in the HCS field. If Disable HCS is set in Segment Insertion mode, the field is set to all-zeros.

6.2. Test Mode Operation

When PLCP Test mode is enabled, all 57 octets of each PLCP slot are read from memory. PLCP frames are sent continually, starting over from the beginning of the segmentation buffer when the end of the buffer area has been reached.

Each PLCP frame is written into an even number of 16-bit words. DS1 and E1 PLCP frames are written into 288-word memory segments. DS3 PLCP frames are written into 344-word memory segments. E3 PLCP frame pairs, consisting of 2 PLCP frames or 18 PLCP slots, are written into 516-word memory segments. In each case, each segment is filled continuously from the first word of the PLCP frame or frame pair.

The register TX_L3_CTRL, which is not used for L3_PDU control functions in the test modes, is set to one-fourth (right shift of two bits) of the first word of the first unused memory segment in the segmentation buffer. The segmentation buffer starts at 2000 hex.

For instance, to write three DS1 PCLP frames, the first frame is written into the 285 words starting at 2000 hex, the second frame is written into the first 285 words starting at 2120 hex (288 decimal = 120 hex), and the third PLCP frame is written into 285 words starting at 2240 hex. The TX_L3_CTRL register is set to 08D8 hex (2360 » 2).

In order to allow the external generation of PLCP overhead in the correct position relative to stuffing when the entire PLCP slot is being read from the buffer, message generation will only start on the first PLCP slot of a PLCP frame. PLCP overhead is provided as described in section 4.5.

In L2 PDU Test mode, a sequence of 53-octet L2_PDU pairs is written to the segmentation buffer as consecutive slots; the first 53 words of each 56-word segment of memory is loaded. The starting address is the initial address of the segmentation buffer, and the TX_L3_CTRL register is set with the address of the first unused 56-word slot, right-shifted by two bits as above. PLCP overhead is provided normally. An even number of L2_PDUs must be in the memory space (in order to have an integral number of 16 bit words with 53 octet PDUs). L2_PDUs are sent consecutively, unless Inhibit L2 PDU is enabled. If this control bit is enabled, idle L2_PDUs are transmitted.

If Insert Idle L2 PDU Header is set, overhead for idle L2_PDUs in this mode must be written to two different addresses in the buffer RAM (this is required for proper RAM processing of odd and even 53-octet L2_PDUs in RAM). The table below shows the required addresses for the the Access Control Field (ACF) and the four octets of the Network Control Information field (NCI-1 to NCI-4):

Octet	Location #1	Location #2
ACF	90 (upper byte)	93 (lower byte; upper byte = 0)
NCI-1	90 (lower byte)	94 (upper byte)
NCI-2	91 (upper byte)	94 (lower byte)
NCI-3	91 (lower byte)	95 (upper byte)
NCI-4	92 (upper byte; lower byte = 0)	95 (lower byte)

Local Processor Control and Send Message are ignored in PLCP Test Mode. In L2_PDU Test mode, these bits can be used to control the transmission of individual L2_PDUs.

In both test modes, the header check sequence is under control of the Disable HCS, Error HCS, and ATM Mode control bits. If Disable HCS is not set, the header check sequence is generated by the circuit and inserted in the output. In this mode the coverage of the HCS is determined by the setting of the ATM Mode control bit and the HCS can be errored by setting Error HCS. If Disable HCS is set, the external input bits are inserted in the HCS field.

In each of the test modes, the payload CRC bits are generated and inserted if Disable Payload CRC is not set. If this bit is set, the bits in the input field are transmitted. If Disable Payload CRC is not set, the Error Payload CRC control bit can be used to force errors in the payload CRC under local processor control. Setting both Disable Payload CRC and Error Payload CRC in either test mode causes the payload CRC field in the segment to be checked for errors.

6.3. Pipeline Operation

The pipeline modes are intended for ATM applications and for switching applications where no level 3 processing is required.

In L2_PDU Pipeline mode, the host transfers 52 octets of the L2_PDU to the segmentation buffer; the HCS is forced to all-zeros by the segmentation block and can be overwritten by the HCS circuit (The host interface can be programmed to transfer this octet, but the segmentation process will ignore this octet and regenerate it).

Segment Pipeline mode transfers 48-octet segments. In this mode, all fields of each segment are transferred by the host. Each segment that is transferred is provided with an L2_PDU header that can programmed in buffer memory. This header consists of the ACF, NCI-1, NCI-2, and NCI-3 octets, and must be written to RAM addresses 98 and 99.

In either of these modes, the upper boundary of the segmentation buffer must be set by the local processor. This value is written to the TX_L3_CTRL register, and must provide an integral number of L2_PDUs or segments that fall on a quad word boundary.

All TX_L2_CTRL control bits are active in either pipeline mode. If Insert Idle L2_PDU Header is set, the header must be written to RAM addresses 90 and 91 as shown in the above table as Location #1. The NCI-4 or HCS octet is always set to 0; the HCS will be calculated unless Disable HCS is set and can be errored if Error HCS is set. The HCS calculation is determined by the setting of ATM Mode. If Insert Segment Header is set, the desired segment header value for idle L2_PDUs must be written to RAM address 92. If Insert Segment Trailer is set, the desired segment trailer value for idle L2_PDUs must be written to RAM address 93.

Payload CRC calculation and checking operates just as in the test modes.

6.4. L2_PDU Transmission Control

In both pipeline and segmentation modes, when there is a message queued, the following conditions have to be met for L2_PDUs to be transmitted:

Inhibit L2_PDU Generation must not be set.

If Local Processor Mode is set, Send Message must have been set to one at the beginning of L3_PDU transmission.

If Enable HOB DQDB Machine is set, this state machine must be in a state that allows transmission of an L2_PDU. If this bit is set, the bandwidth balancing modulus must also be set in the BWB_MOD register. A BWB_MOD value of 0 disables the bandwidth-balancing function, as is required for SMDS service.

If Enable SCARF Synchronization (in the SYS_CONFIG control) is set to 1, the multiplex priority input pin (MUXPRIN) must be high for the current L2_PDU time.

If there are no messages to send or if L2_PDU transmission is inhibited, all-zeros are sent to the Transmit PLCP block for all L2_PDU content.

In normal operation, the overhead fields of active L2_PDUs are taken from the following locations or set to the indicated values:

Overhead Field	Source
L2_PDU Header	Buffer RAM (addresses 98-99)
Header Check Sequence	HCS Generation Circuit
Segment Type	L3_PDU Generator
Sequence Count	L3_PDU Generator
MID	Buffer RAM (address 9C for SSM, 9A for other)
Length Field	L3_PDU Generator
Payload CRC	Payload CRC Generation Circuit

If Enable SCARF Synchronization is set, the MUXPRIN input is sampled before each L2_PDU interval; if there is an L2_PDU ready for transmission and the input is high it is transmitted; otherwise an idle L2_PDU is generated. This allows external control of L2_PDU transmission, which can be used for multiplexing SCARFs to send L3_PDUs from multiple sources or to mix L3_PDUs and isochronous traffic. The MUXPRIN input must be set high if the HOB DQDB machine is enabled.

The MUXPROUT output is low if either the MUXPRIN input is low or an L2_PDU is going to be transmitted; otherwise it is high.

The DQDB state machine implementation for head-of-bus provides control of the queuing for head-of-bus operation. The state machine is described in TR-TSV-000772, section 4.2.2.2.

The input to the state machine is the current state of the transmit "queue" (whether there is a message to be sent or not) and the value of the request bits in the ACF field of each received L2_PDU. The output is a flag that enables transmission of L2_PDUs.

Note that the required inputs to this function from the reassembly block are the request bits REQ-0, REQ-1 and REQ-2. These bits are contained in the ACF field of L2_PDUs.

6.5. L3_PDU Segmentation

There are two modes available for the segmentation of L3_PDUs. In L3 PDU Partial mode, message segmentation starts as soon as the first segment of an L3_PDU is available. This allows the segmentation to proceed with minimum delay, but it requires that the entire L3_PDU be formatted before entry to the SCARF. In L3 PDU Complete mode, entire messages are transmitted through the host interface before they are segmented by the segmentation block. Control of the segmentation process is done via the stack processing functions.

If address screening and CRC checks are required, these are controlled by an additional stack pointer ADR_SEG_PTR. In the case that either of these checks is being performed, the value of this stack pointer should be used to determine whether a message is ready for transmission. If a message is invalidated by a check operation, the segmentation block will discard it.

If a CRC check is required, the entire message must be in the segmentation buffer before the check can be completed, so the L3 PDU Complete mode must be used. Address screens can be run in either partial or complete mode.

All TX_L2_CTRL control bits are active in both L3_PDU modes. If Insert Idle L2 PDU Header is set, the header must be written to RAM addresses 90 and 91. The NCI-4 or HCS octet is always set to 0; the HCS will be calculated unless Disable HCS is set and can be errored if Error HCS is set. The HCS calculation is determined by the setting of ATM Mode. If Insert Segment Header is set, the desired segment header value for idle L2_PDUs must be written to RAM address 92 and the desired segment header value for active L2_PDUs (except for MID) must be written to RAM address 9A. The MID field is always read from RAM address 9C for SSM segments and from RAM address 9A for other segment types. If Insert Segment Trailer is set, the desired segment trailer value for idle

L2_PDUs must be written to RAM address 93 and the desired segment trailer value for active L2_PDUs to RAM address 9B Note that the payload CRC field will be overwritten unless payload CRC generation is inhibited.

6.5.1. L3_PDU Format Control

Figure 6.3 shows the individual bit functions of the L3_PDU Format Control Register TX_L3_CTRL. This register is located at address 04. This register controls L3_PDU overhead generation in the message segmentation section of the SCARF. Each of the indicated overhead fields can be either read from the segmentation buffer or generated internally by the SCARF and inserted as a part of the message content loaded from the host.

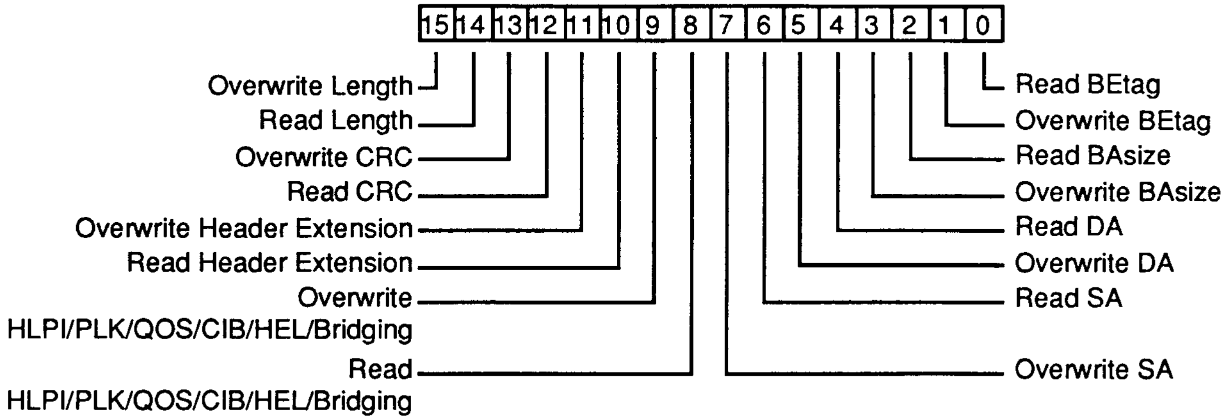


Figure 6.3. TX_L3_CTRL Register (address 04)

All control bits except the CRC bits operate in the following way. If the "Read" control bit is set, the overhead field is read from the segmentation buffer and inserted into the transmitted message. If the "Overwrite" bit is set, the field exists in segmentation buffer, but is generated internally for transmission. (Setting both bits has the same effect as setting the Read bit only). If neither bit is set, the field does not exist in the segmentation buffer and is generated internally for transmission. This register is active only in L3_PDU Complete and L3_PDU Partial modes; in the pipeline modes, it is used to set the upper boundary of the segmentation buffer.

The fields that have internal generation capability other than being read from the buffer RAM message space are the BAsize and Length fields, the BEtag fields, the CIB and PL bits, and the CRC-32 field. The BAsize and Length are calculated from the message length in the segmentation buffer. The BEtag value is taken from a dedicated register, and the CRC-32, and CIB bit are calculated as a part of the segmentation process. The PL bit is calculated as a part of the segmentation process and OR'd with the input field, whether from RAM memory or provided from the host. The reason for this is to allow the PAD field to be provided externally. Note that when the PAD field is provided externally, the PL bits must be set to the required values.

The memory space for the L3_PDU overhead (starting with the destination address) is in buffer RAM locations A2-B1. The overhead fields appear in this space just as they would for a L3_PDU that had a zero-length information field, requiring 44 octets. Note that Read BEtag will cause both the beginning and end tags to be read from memory. Also, if either the BEtag, the Length, or the CRC fields are read from memory, the information field must be padded to be four-octet aligned.

The sources of the fields that can be inserted by SCARF are summarized as:

Reserved/BEtag (beginning)	BEtag Register
BAsize	(calculated from L3_PDU length)
Destination Address	Buffer RAM Address A2-A5
Source Address	Buffer RAM Address A6-A9
HLPI/QOS/HEL	Address AA
CIB Bit	(calculated from control bits)
PL Field	(calculated from L3_PDU Length)
Bridging Field	Buffer RAM Address AB

Header Extension	Buffer RAM Addresses AC-B1
CRC32 Field	CRC Generator
PAD Field	Internally generated as required

CRC generation is determined by the Read CRC and Overwrite CRC bits. The CRC-32 circuit monitors the value of Read CRC and Overwrite CRC to determine whether or not to insert the CRC. If neither bit is set, the CIB bit is overwritten to 0 and no CRC is included in the L3_PDU. If either bit is set, the CIB bit is forced to one and the L3_PDU will include the CRC field. If the Read CRC control bit is set, the CRC field is generated from the contents of the segmentation buffer rather than the internal circuit. If the Overwrite CRC bit is set, the CRC field in the segmentation buffer is overwritten by the CRC circuit. If both Read CRC and Overwrite CRC control bits are set, the CRC is inserted by the CRC circuit and the CRC field is not present in the segmentation buffer.

In L3_PDU Partial mode, the BAsize field and all other L3_PDU overhead must be present in the message as it is loaded from the host. In addition, the BAsize field must be consistent with the presence of the CIB bit and the CRC-32 field in the L3_PDU. In this mode, if the CIB bit is 0, then no CRC-32 field will be inserted regardless of the setting of the Read CRC and Overwrite CRC control bits. If both Read CRC and Overwrite CRC are set and the CIB bit is 1, the CRC field cannot be present in the message, but the BAsize field contents and the Length field contents must be set as if it were. In any mode that causes the CRC-32 to be generated or read, the CIB bit is forced to 1. The PL field is not generated in this mode, and must be set correctly in the message loaded from the host.

Figure 6.4 shows the individual bit functions of the Transmit BEtag Field Register. This register is located at address 20. This register holds the value which is inserted into the BEtag fields in L3_PDUs by the segmentation process. This value is incremented after each use and may be reset to a zero value with the Clear BEtag Register bit in the TX_PROT register. It can be read by the local processor but will not be cleared when read and cannot be written.

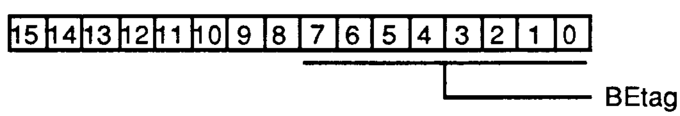


Figure 6.4. BEtag Register (address 20)

6.5.2. L3_PDU Transmission Control

The transmission of L3_PDUs is under control of a set of stack pointers. There are three pointers defined, each of which points to one of 128 entries in a segmentation control stack. Each entry in the stack consists of a sixteen-bit address pointer and a sixteen-bit length field. The segmentation control stack is located at addresses 100-1FF of buffer RAM. Both segmentation and reassembly stack processes are monitored through a single stack interrupt status register.

Other options for segmentation formatting and control are in the transmission protocol control register TX_PROT, located at address 05, shown in Figure 6.5. This register controls the addition of headers to L3_PDUs in the message segmentation section of the SCARF, as well as segmentation initialization.

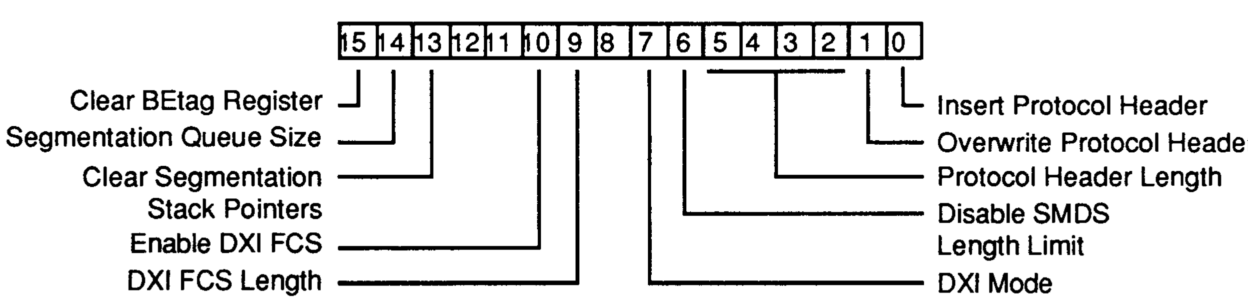


Figure 6.5. TX_PROT Register (address 05)

Insert Protocol Header causes a header to be read from RAM addresses C0-CF and inserted at the beginning of the INFO field of the L3_PDU before it is segmented. If this field is to overwrite information delivered from the host, Overwrite Protocol Header is set instead of Insert Protocol Header. The protocol header length in double-octets is specified by bits 5-2, so it can be up to 32 octets long. The field contains a value of one less than the desired number of double-octets.

Disable SMDS Length Limit disables the length limit of 9232 octets for L3_PDUs. If this bit is set, the maximum length is 65532.

DXI Mode causes the SCARF to terminate the frame format of the SMDS Data Exchange Interface (DXI) for segmentation. The FCS field in L3_PDUs transferred from the host is checked and the message content (L3_PDU or local management PDU) is determined. The MSB of the length field entry on the segmentation stack is used to indicate a management message in this mode. For an L3_PDU message, the four-octet DXI Header and Trailer (FCS field) of the message that is passed from the host is not segmented or transmitted. If a management message is recognized, the DXI LM Message status bit is set in the STK_STATUS register, which will generate an interrupt. The local processor can then read the contents of the segmentation address screen pointer and the segmentation stack contents to determine the location and length of the message, which can then be read from buffer memory.

Enable DXI FCS allows the address screening block to check the frame-check sequence (FCS) on each message received from the host in SMDS DXI mode. DXI FCS Length selects the FCS field length with logic-zero indicating a 16-bit FCS and logic-one indicating a 32-bit FCS.

Clear Segmentation Stack Pointers sets the three pointers that operate on the segmentation stack and resets all of the message control circuitry for segmentation. This effectively resets the segmentation process. This control bit is not latched and will be read as zero.

The Segmentation Queue Size field sets the number of messages that can be queued in the segmentation RAM. If this field is set to zero, the limit is set to 127, which is one less than the number of messages that can be held in the Segmentation Stack memory. If this field is set to 1, a maximum of 16 messages may be queued at once.

Clear BEtag Register clears the counter that generates the BEtag field. This control bit is not latched and will be read as zero.

A further control on L3_PDU transmission can be provided by the access class credit manager. This provides a limitation on average transmission rate for segmentation; the underlying algorithm is described in TR-TSV-000772, section 4.3 A single credit manager is provided by SCARF and can be assigned to either the segmentation process or the reassembly process. The access class manager is described in section 7.7.3.

When the access class credit manager is programmed to operate as a part of the segmentation function, it will inhibit segmentation of an L3_PDU until enough credit has accumulated to allow the L3_PDU. This would normally be used as a CPE function to ensure, for instance, that a multiport router did not transfer enough messages to an SMDS service to violate a selected access class.

6.5.3. Segmentation Stack Functions

Control of the segmentation process is through a set of stack functions. The "stack" as defined here is really a circulating store; however, the segmentation store and the stack are protected against "roll-over", so that the functions are more like a stack operation.

The segmentation stack buffer consists of 256 memory locations that are organized as an address field and a length field in consecutive addresses for each L3_PDU that is to be transmitted; the buffer capacity is thus 128 messages. These values are written to the memory locations by the host interface as each message is queued for segmentation. There are three pointers to these stack locations. The host segmentation pointer HST_SEG_PTR is maintained by the host interface and is incremented to point to the locations identifying a message after that message has been loaded into the segmentation buffer. The address screen pointer ADR_SEG_PTR is maintained by the segmentation address screen circuit; this circuit also performs DXI FCS checks when required in SMDS DXI mode. Finally, the segmentation process maintains the segmentation stack pointer. This pointer is used to maintain the segmentation process.

There are conditions that can be programmed to cause interrupts at each stage of the segmentation process. If a particular event is programmed to cause an interrupt, it will also latch the value of the corresponding pointer when the interrupt occurred. By reading the pointer value twice in succession when such an interrupt is processed, the range of pointer values for which this condition could have occurred is established. This allows the investigation or logging of these conditions as required.

The host interface segmentation pointer HST_SEG_PTR is incremented each time a message is ready for segmentation. In L3_PDU Complete mode, each time a complete message is transferred to the segmentation buffer, the address pointer to the first octet of the message and the length of the message in octets is written to the segmentation stack. The pointer is then incremented. In L3_PDU Partial mode, the pointer to the first address and the BAsize field from the L3_PDU are written to the stack, and the pointer is incremented after the first segment is written to the segmentation buffer.

The address screening function maintains a pointer, ADR_SEG_PTR, that points to a message that is being screened. The operation of this function is described in section 8. This block will also check the FCS on an L3_PDU that is transferred from the host in SMDS DXI mode; this check is required when using the serial HDLC interface, and is recommended for DS1 and E1 operation only.

The segmentation block maintains the SEG_STK_PTR and compares its value to ADR_SEG_PTR. This indicates when a message should be sent.

Pointer status is available in a stack interrupt status register STK_STATUS, located at address 25. Figure 6.6 shows its individual bit definitions. The status bits in this register indicate events associated with the segmentation and reassembly stacks, address screening, segmentation failures, and the host interface. Each of the bits in the STK_STATUS register can be programmed to generate an interrupt at the STK_INT pin by setting the corresponding bit of the STK_STATUS Interrupt Enable Register EN_STK_INT at address 1F. The interrupt will be cleared when the STK_STATUS register is read, which clears the status bit. If an interrupt is not enabled and the event occurs, the appropriate status bit is still set, even though the interrupt does not occur.

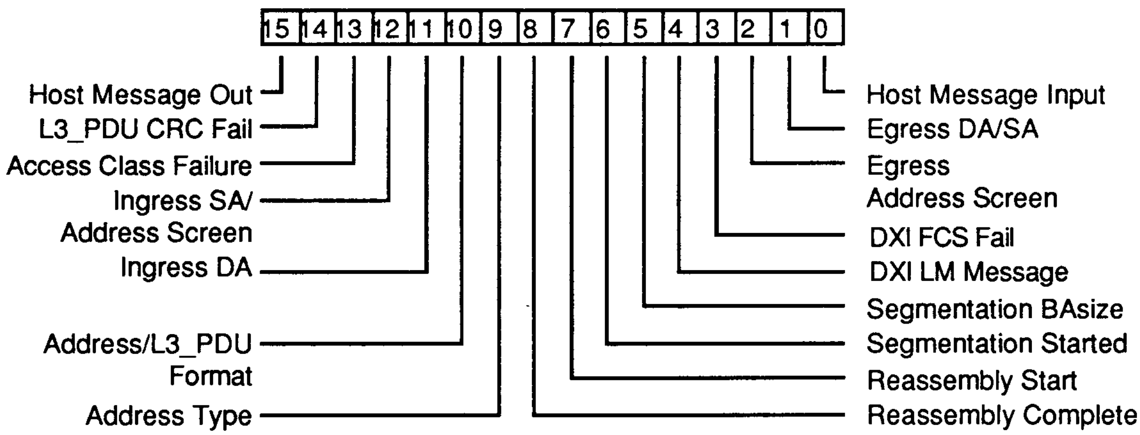


Figure 6.6. STK_STATUS Register (address 25)
EN_STK_INT Register (address 1F)

Host Message Input indicates the host has placed a message on the segmentation stack. If this status bit is programmed to enable an interrupt, when it is set, the value of HST_SEG_PTR is latched until read. Reading the pointer value twice will give the value of the pointer when the interrupt occurred and the current value, allowing the determination of the number of messages that have been input since the interrupt was last processed.

Segmentation BAsize indicates that segmentation of an L3_PDU has been inhibited because it would have exceeded the BAsize limit specified for SMDS service (or 65532 if Disable SMDS Limit is set). Segmentation Started indicates segmentation of an L3_PDU has begun; if Local Processor Mode in TX_L2_CTRL is set, this bit indicates that a message is ready for segmentation. Enabling either of these bits to interrupt will latch the value of SEG_STK_PTR.

Egress DA/SA indicates that either the destination address of the message is not in the SNI address list or that the individual source address is. Egress Address Screen indicates that the source address screen failed. Either of these conditions will latch the value of the address screen pointer ADR_SEG_PTR if programmed to enable interrupts.

DXI FCS Fail indicates that the frame-check sequence has failed on completion of the transfer of an L3_PDU from the host in SMDS DXI mode. DXI LM Message indicates that the message transferred from the host is a local management message and should be read by the local processor. In either case the message will be ignored by the segmentation block. Either of these events when enabling interrupts will latch the value of the ADR_SEG_PTR.

Address violations or address screen failures and DXI status bits can be read from the length field of the segmentation stack. DXI FCS failures are indicated by setting the most significant bit of this field to 1 and the rest of the bits 0. Local management messages are indicated by setting the most significant bit to 1; the rest of the bits indicate the length of the message. Note that this limits valid SMDS DXI messages to less than 32768 octets even if Disable SMDS Length Limit is set. A length field value of 4 or less indicates an address screen failure (see Section 8).

If the access class credit manager is enabled for segmentation, it will set the Access Class Failure status bit each time the access class credit is exceeded. The access class manger will inhibit segmentation until sufficient credit is available. If this bit is set to enable an interrupt, it will latch SEG_STK_PTR.

The reassembly address screen status bits are described in section 8.

The other interrupt conditions in the register are set by the reassembly process and are described in section 7.

6.6. Status and Status Interrupts

There are several event counts and status functions that are maintained for segmentation. These appear in the INT_STATUS register, which is shown in Figure 6.7. These status bits each can be enabled to cause an interrupt on the STAT_INT pin by enabling the corresponding bit of the EN_INT register, which is illustrated in Figure 2.4.

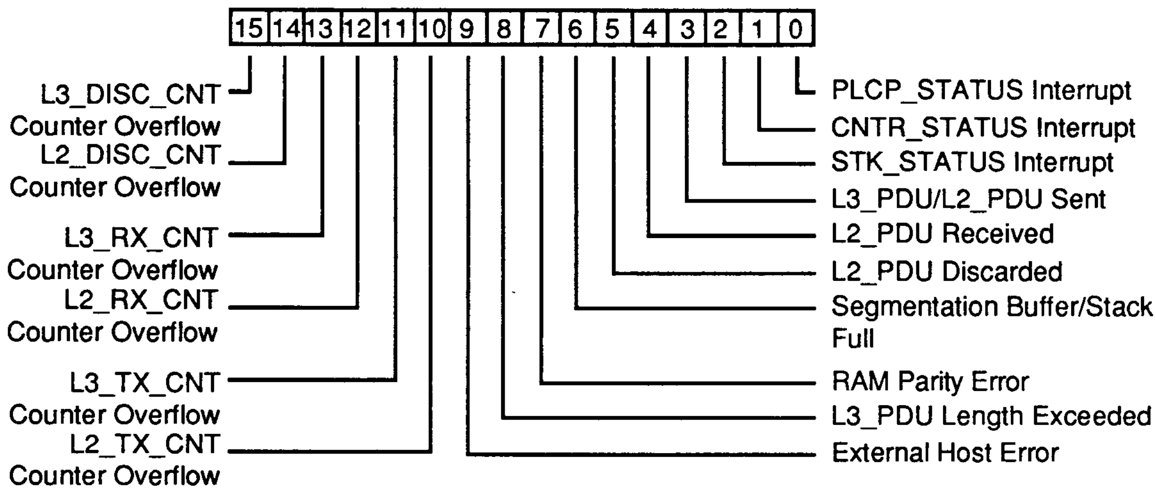


Figure 6.7. INT_STATUS Register (address 22)

L3 PDU/L2 PDU Sent has different functions in each of the modes. In L3_PDU Complete and L3_PDU Partial mode, it is set each time an L3_PDU has completed segmentation and has been transmitted; if segmentation is being controlled by the local processor (Local Processor Control enabled), the interrupt is set when the segmentation process becomes idle. In L2_PDU Pipeline and Segment Pipeline modes, it is set each time an L2_PDU is transmitted. In L2_PDU Test mode, it is set each time two L2_PDUs are transmitted. In DS1, E1, and DS3 PLCP Test modes, it is set each time a PLCP Frame is transmitted; in E3 Test mode, it is set once every other PLCP frame. This bit is cleared when the INT_STATUS register is read.

There are three status bits in the INT_STATUS register that are set by the host interface to indicate problems in processing inputs for segmentation. These status bits are required because the maximum host transfer rate far exceeds the capacity of the PLCP. These bits can be programmed to provide interrupts on STAT_INT by setting the corresponding bit in the EN_INT register.

Segmentation Buffer/Stack Full indicates the host interface does not have sufficient segmentation buffer space to write an incoming message or that the capacity of the circular buffer to stack message data (address in RAM and length) has been exceeded. This can occur if 128 or more short messages are loaded before they can be transmitted by the PLCP. In either case a message is discarded.

L3 PDU Length Exceeded indicates a message received by the host interface exceeds the maximum length of an SMDS L3_PDU (or 65532 octets if Disable SMDS Length Limit is set in the TX_PROT register) and has been discarded. External Host Error indicates a failure in the protocol between the host interface and the host. These three status bits are cleared when the INT_STATUS register is read.

Counts are maintained of L2_PDUs and L3_PDUs transmitted in counters L2_TX_CNT and L3_TX_CNT respectively. These counters can be programmed to cause interrupts in INT_STATUS by setting bits 10 and 11 of the EN_INT register (Figures 2.3 and 2.4). If the counter interrupts are not enabled, the counters will stop at their maximum value of 65,535; if interrupts are enabled, the counters will interrupt on "roll over" and continue counting. The counters and their interrupt status bits clear when read.

In the pipeline modes, the TX_L3_CNT counter will count payload CRC errors on incoming segments if that option is enabled.

6.7. L3_PDU Insertion by the Local Processor

The local processor is able to insert L3_PDUs into the buffer memory by manipulating the message stack. This function is distinct from the use of the local processor as the host, as described in section 5.3. The capability described here allows the local processor to insert an L3_PDU in the message queue in any host mode. This capability is useful for implementing loopbacks and other SMDS-level maintenance and diagnostic functions.

This operation is done by inserting the L3_PDU at the bottom of the unused space in the segmentation buffer, and then overwriting the current values of the message stack and then forcing the message to be resent.

This procedure ensures that the L3_PDU sent by the local processor will not overwrite an L3_PDU currently being loaded to the segmentation buffer by the host.

The detailed procedure is as follows:

1. Read the current value of the segmentation stack pointer SEG_STK_PTR.
2. Read the address of the message from the memory location in the SEG_STK_PTR pointer.
3. Write the L3_PDU into the segmentation buffer so that it ends at the location just before the address of the beginning of the L3_PDU currently being transmitted.
4. Set Local Processor Control bit in the TX_L2_CTRL register.
5. Read the INT_STATUS register to clear it and enable the L3 PDU/L2 PDU Sent and the Segmentation Started interrupts. In this mode, L3 PDU/L2 PDU Sent is set when the segmentation process is idle.
6. Wait for an interrupt on L3 PDU/L2 PDU Sent.
7. Set Inhibit SEG STK PTR Update.
8. Read SEG_STK_PTR and write the beginning address to the buffer memory location that is indicated by SEG_STK_PTR and the length of the L3_PDU in octets to be transmitted to the following buffer memory location.

9. Set TX_L3_CTRL for the desired functions.

10. Toggle Send Message. This will cause the L3_PDU that was loaded into the buffer memory to be transmitted. Wait for an interrupt on L3 PDU/L2 PDU Sent to indicate that segmentation is completed and the segmentation process is idle.

11. Restore TX_L3_CTRL and clear Local Processor Control and Inhibit SEG STK PTR Update. This will restore normal L3_PDU operation of the segmentation block.

The only other processing to be done is to ensure that the host processor does not overwrite the buffer space when the buffer pointer is "backed up" to allow the transmission of the L3_PDU inserted by the local processor. This can be done by monitoring the value of the HST_SEG_PTR or by disabling host message transfer if required.

7. REASSEMBLY PROCESS

Reassembly refers to the concatenation of received L2_PDU payloads to reconstitute an L3_PDU. SCARF provides modes both that reassemble messages and that deliver L2_PDU slots or segments.

There are six modes available for reassembly. Two test modes are provided that write entire PLCP slots or entire L2_PDUs directly to memory. Two pipeline modes are available; one delivers entire L2_PDUs and the other delivers 48-octet segments to the host, after any specified level 2 checks are completed. Two modes provide reassembly of L3_PDUs. One does logical reassembly only; it delivers to the host 48-octets that are accepted as a part of a message with segment overhead intact. The other reassembles complete L3_PDUs in memory; the L3_PDUs are transferred to the host in the order that they complete the reassembly process.

This section describes the function of the reassembly process and state machines. The process consists of the identification of new messages from L2_PDUs, updating of the message status, and loading the message payload to the reassembly buffer.

Messages (L3_PDUs) are tracked by associating message status using a MID pointer to RAM. In this way up to 128 L3_PDUs can be reassembled simultaneously, assuming the reassembly buffer has adequate physical storage space. A "stack" process similar to the segmentation stack is used to provide status on the reassembly process. One pair of pointers tracks the start of messages and one pair tracks the completion of messages, including transfer to the host.

Message validation checks are performed for both L2_PDUs and L3_PDUs. These checks may be individually disabled.

7.1. Reassembly Control

There are six modes of reassembly. Two test modes are provided that allow the local processor to read long test messages either of entire PLCP slots or of entire L2_PDUs. In these two modes, level 2 message validation checks are executed but all segments are forwarded unchanged.

An L2_PDU "pipeline" mode that forwards 52 octet segments is provided for extracting all fields except the header check sequence from each L2_PDU. Only L2_PDUs with a valid header check sequence will be forwarded, unless that check is disabled.

A segment mode that forwards 48-octet segments is provided to allow processing of all SMDS SIP Level 2 checks without reference to the SIP Level 3 processes.

A segment mode that performs logical reassembly of L3_PDUs while forwarding 48 octet segments in the order received is provided to allow pipelining of the reassembly process. In some applications this can minimize processing delay and reduce buffer storage requirements.

Finally, one mode provides for the complete reassembly of L3_PDUs. Each L3_PDU is reassembled in the reassembly buffer and transferred to the host in the order that the L3_PDUs complete reassembly.

The reassembly process operates either autonomously or under control of the local processor. In autonomous mode, messages are forwarded automatically; local processor control allows them to be sent one by one. This mode can allow per-message processing of message content or overhead by the local processor.

The Reassembly process is controlled by the RX_CTRL word as shown in Figure 7.1.

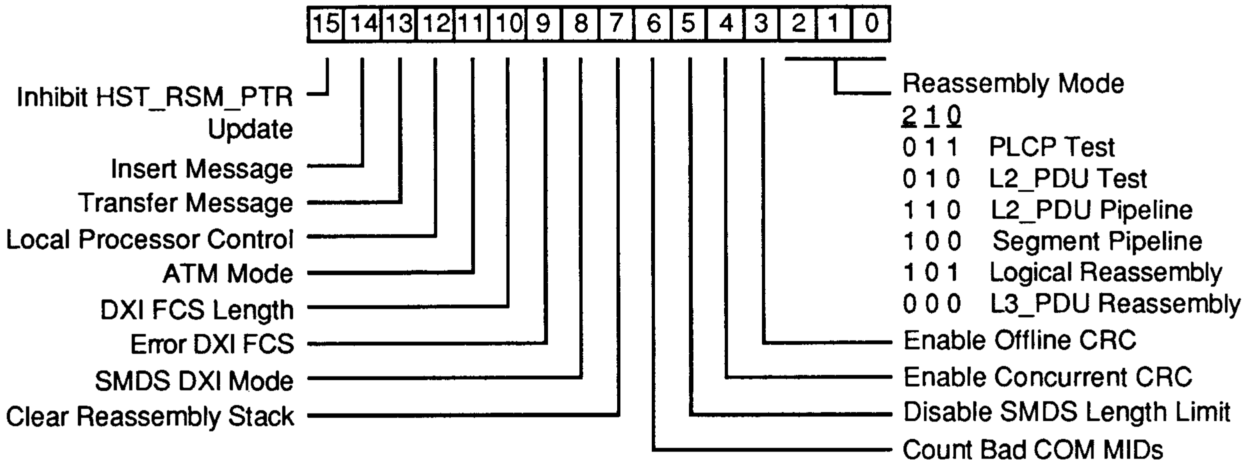


Figure 7.1. RX_CTRL Register (address 07)

PLCP Test Mode allows the capture of entire PLCP slots in buffer RAM. L2_PDU Test Mode allows the same for 53-octet L2_PDUs. These modes allow testing of the receive-PLCP block output. The messages are loaded directly to RAM where they may be read by the local processor. Error counters are active in this mode, so that errors can be detected. However, all information is loaded to RAM whether or not it contains protocol errors.

In L2_PDU Pipeline mode, the reassembly block receives 53 octet L2_PDUs from the receive PLCP. The HCS check is the only processing that is performed, and the HCS is stripped out before the segment is written to the reassembly buffer (only 52 octets are written). Other error counters are active.

Segment Pipeline mode receives 53 octet L2_PDUs from the receive PLCP and forwards 48 octet segments to the host in the order received. No level 3 functions are provided.

Logical Reassembly provides for the reassembly of L3_PDUs but transfers successive segments to the host in the order received. If an L3_PDU fails to reassemble (bad sequence number or segment count limit exceeded) any additional segments of the L3_PDU are discarded.

L3_PDU Reassembly mode provides complete reassembly of L3_PDUs. The entire L3_PDU is received and validated before the message is passed to the host interface. A reassembly-quit stack process is used to communicate between the reassembly process and the host interface, and can be monitored by the local processor.

Disable SMDS Length Limit allows the BAsize and Length fields of a message to be as large as 65532 octets.

Enable Offline CRC enables an off-line check of the 32-bit CRC when present in an L3_PDU. Enable Concurrent CRC enables a CRC check of reassembled messages concurrently with transfer to the host. These checks are described in detail in section 7.7.5.

Count Bad COM MIDs enables the Invalid message ID counter EOM_MID_ERR to count this condition on COMs as well as EOMs.

Clear Reassembly Stack sets the four pointers (RSM_STRT, RSM_QUIT, ADR_RSM_PTR, and HST_RSM_PTR) that operate on the reassembly stacks to zero and resets all of the message control circuitry for reassembly. This is used to initialize the reassembly process, as described in section 7.7.6. This control bit is not latched and will always be read as 0.

SMDS DXI Mode causes the SCARF to handle the frame format of the SMDS Data Exchange Interface (DXI). The DXI Header and FCS field are added to reassembled messages before they are passed out of the host interface. The header is read from the Receive Protocol Space in buffer RAM at address E0.

DXI FCS Length selects the FCS field length with "zero" indicating a 16-bit FCS and "one" indicating a 32-bit FCS. Error DXI FCS errors one bit of the FCS before transmission. This bit is latched and cleared once the error has been generated for a single message. This function can be used as a diagnostic test of FCS functions.

ATM Mode causes the HCS to be calculated on octets 1-4 of the L2_PDU header instead of header octets 2-4.

Local Processor Control allows the local processor to control the transfer of L3_PDUs or L2_PDUs to the host. In this mode, an interrupt will be generated each time an L2_PDU is ready for transmission in Pipeline Mode or an L3_PDU is ready for transmission in 44-octet Reassembly mode. Setting Transfer Message, which is an unlatched control bit, will cause one pending message (L2_PDU or L3_PDU) to be sent. Transfer Message is also used to initiate storage of received data into the reassembly buffer RAM in the test modes.

Insert Message causes the host interface to output a message inserted by the local processor. See Section 7.11 for details. This is an unlatched control bit and will be read as 0.

Inhibit HST RSM PTR Update inhibits the host from incrementing the host reassembly stack pointer after an L3_PDU has been sent out of the host interface in L3_PDU Reassembly mode. This control bit can be used to allow a single message to be sent out of the host interface repeatedly.

The level 2 and level 3 validation checks performed by the reassembly process can be individually disabled with the control bits in the Receiver L2_PDU and L3_PDU Validation Register RX_CHECK. The RX_CHECK bit functions are shown in Figure 7.2.

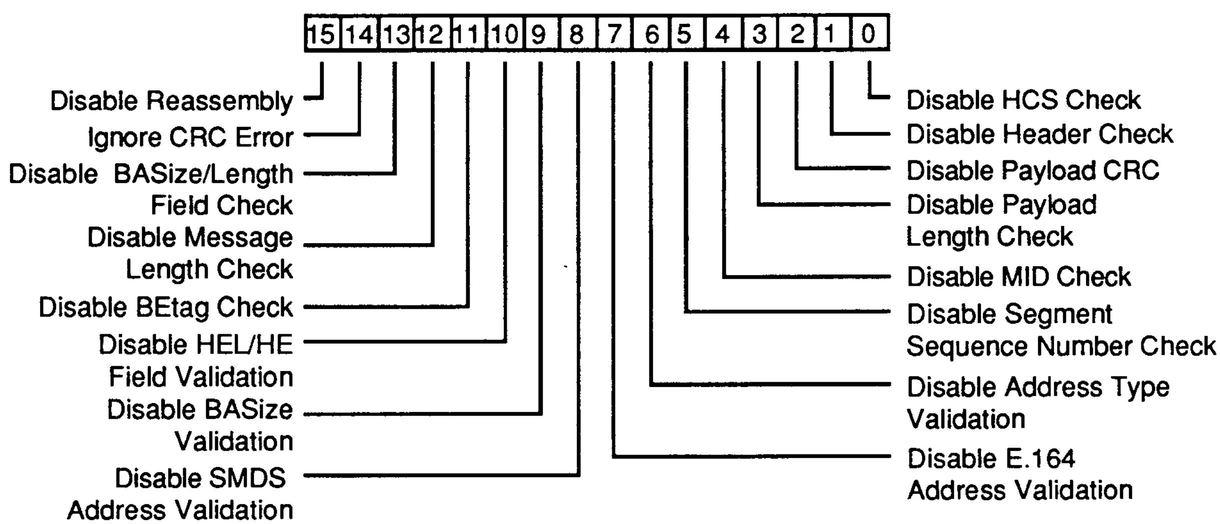


Figure 7.2. RX_CHECK Register (address 08)

Bits 0 through 4 disable L2_PDU validity checks; bits 5 through 13 disable level 3 validity checks. Disable HCS Check disables the check of the header check sequence, which for the value of the network control field has a hex value of 22. Disable Header Check disables the check that the first two octets of the network control field have the hex value FF FF and the third octet has the value specified in the NCI field of the RX_HDR register. Disable Payload CRC Check disables the check of the Payload CRC. Disable Payload Length Check disables the check for consistency between the segment type field and the length field. Disable MID Check disables the check for a zero

MID for SSM segments and a non-zero MID for BOM, COM and EOM segments. This bit does not function in Logical Reassembly or L3_PDU Reassembly mode.

Whenever a segment is received with an invalid field and the check of that field is disabled, the segment is accepted and not counted as discarded. However, the error count associated with the condition is incremented. When L3_PDU format checks are disabled, they may not be indicated as there is no way to provide them as status bits without stopping reassembly.

Disable Segment Sequence Number Check causes the reassembly process to ignore the sequence field when doing reassembly. When this condition is detected, the error will always be counted, but if this control bit is set reassembly will continue. No status bit will be set for the condition.

Disable Address Type Validation disables the check of the source and destination address type fields against valid 802.6 address types. Disable E.164 Address Validation disables the check that the source address type is an individual 60-bit public address, that the destination address is a group or individual 60-bit public address, and that the source and destination address fields are valid international addresses according to CCITT recommendation E.164; such an address consists of BCD-coded decimal digits and all-1s pad for unused characters. Disable SMDS Address Validation disables the check that if the source or destination addresses is a U.S. National number (first digit of the address equals 1), then the rest of the address is formatted correctly ten BDC digits followed by FFFF).

Counters are provided for non-802.6 source and destination address types and for non-SMDS (non 60-bit public) address types; the counters are described in section 7.8. At most one counter will be incremented for any given L3_PDU; if the destination address type is not an 802.6 address type, the source address type will not be checked. The counted events are not affected by the setting of the control bits in the RX_CHECK register.

Disable BASize Validation causes the reassembly process to accept any length in the BAsize field. Disable HEL/HE Field Validation causes the reassembly process to ignore the HEL and HE fields; this will mask the L3_PDU status bit when errors in these fields occur. No status bit will be provided for either of these conditions if the corresponding disable control bit is set.

Disable BEtag Check causes the receiver to ignore the beginning and ending BEtag values in doing reassembly. Disable Message Length Field Check disables the check of the length field against the received message length. Disable BAsize/Length Check disables the check of the length field of an EOM or SSM for consistency with the BAsize field. If any of these three conditions are detected, the corresponding status bits will be set in the reassembly-quit status word (see section 7.2 below) regardless of the setting of the control bits.

Ignore CRC Error allows the transfer to the host of a reassembled message even though the 32-bit CRC field defined in IEEE 802.6 is in error. This is described in section 7.7.5.

Disable Reassembly inhibits all reassembly functions; it is used for initialization of the SCARF reassembly functions as described in section 7.7.6.

7.2. Reassembly Stack Functions

The Logical Reassembly mode and the L3_PDU Reassembly mode use two stacks located in buffer memory, a reassembly-start stack (addresses 200-2FF) and a reassembly-quit stack (addresses 300-3FF). There are two pointers to each of these stacks.

The reassembly-start entries are two words: the address of the first octet pair of an incoming L3_PDU and a L3_PDU MID/status word as shown in Figure 7.3. The reassembly process places an entry on the reassembly-start stack at the location of the reassembly-start pointer RSM_STRT when an SSM or BOM segment is received. Reassembly address screens (see Section 8) are performed on messages on the reassembly start stack by tracking the RSM_STRT pointer with a second stack pointer ADR_RSM_PTR. The reassembly-start stack can be used by the local processor to time messages as they are reassembled to enforce the MRI (Message Receive Interval). The reassembly-start pointer RSM_STRT can be read by the local processor when an interrupt is received to determine what addresses should be read.

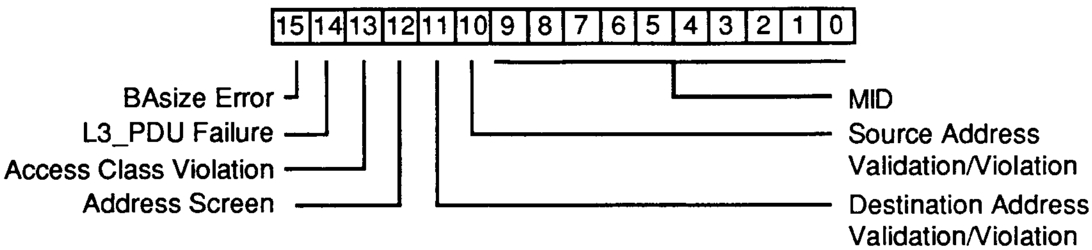


Figure 7.3. Reassembly-start Stack Status

MID is the message identifier for the message. Source Address Validation/Violation, Destination Address Validation/Violation, and Address Screen indicate that the message failed an address check; these functions are described in section 8. Access Class Violation indicates an L3_PDU would exceed the allowed message traffic as defined by Section 4.3 in TR-TSV-000772. L3_PDU Failure indicates that the L3_PDU was discarded due to a level 3 failure in the BOM or SSM, and a message timer should not be started by the local processor. The specific level 3 error for the message will be indicated in the reassembly-quit stack entry for the message (see below). If this bit is not set, the L3_PDU will be reassembled normally by SCARF and will eventually be entered on the reassembly-quit stack. However, if there is an address screen failure or access class violation, the L3_PDU will not be transferred to the host.

BAsize Error indicates that there was an error in the BAsize field.

The reassembly-quit stack is written at the address given by the RSM_QUIT pointer whenever a message completes reassembly or is terminated due to an error condition. The host interface outputs messages from the stack using the HST_RSM_PTR which tracks the RSM_QUIT. The reassembly-quit stack entries consist of two words: the address of the first octet pair of the L3_PDU and L3_PDU Status (error bits). The L3_PDU Status encoding is shown in Fig. 7.4.

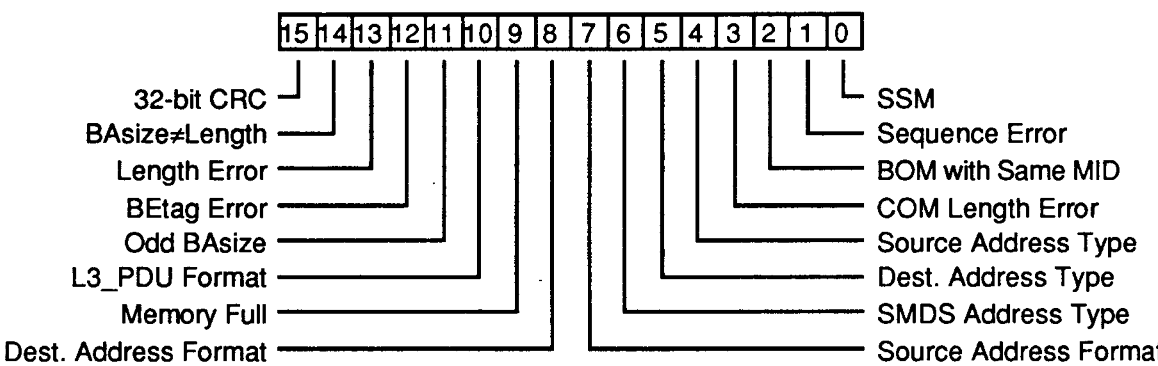


Figure 7.4. Reassembly-quit Stack Status

If none of the bits in the second word are set, the message successfully completed reassembly. If any bit other than the SSM bit is set, an error has occurred and the L3_PDU is discarded by the reassembly process. SSM indicates that the message is a Single Segment Message. Sequence Error indicates that an L2_PDU was received with the wrong sequence number. BOM with Same MID indicates a BOM with the same MID as the discarded L3_PDU was received before the discarded L3_PDU completed reassembly. In this case, the reassembly process terminates processing on the old message and begins reassembling the new message. COM Length Error indicates a COM segment was received which caused the message length to exceed the BAsize.

Source Address Type indicates that the source address type was not an allowed 802.6 address type. Destination Address Type indicates that the destination address type was not an allowed 802.6 address type. SMDS Address Type indicates that the source or destination address type was not an allowed SMDS address type. Source Address Format indicates that the source address field did not conform to the SMDS address field format. Destination Address Format indicates that the destination address field did not conform to the SMDS address field format. Memory Full indicates that reassembly failed due to the exhaustion of the reassembly buffer.

L3_PDU Format indicates one of the following errors in the L3_PDU: invalid BASize, invalid Header Extension Length, or invalid Header Extension. Odd BAsize indicates that the BAsize was not 0 mod 4.

BEtag Error indicates that the beginning and ending BEtag fields did not match. Length Error indicates the message length did not match the length field. BAsize ≠ Length indicates the BAsize and Length fields of the L3_PDU do not match. 32-bit CRC indicates an error in the L3_PDU CRC-32 field.

The local processor can read RSM_QUIT when interrupted in order to read the address and error condition entries from the reassembly-quit stack for logging errors. The payload of the first L2_PDU of the message is stored contiguously in the reassembly buffer, starting at the address given in the first word on the reassembly-quit stack.

7.3. Test Mode Operations

When PLCP Test mode is enabled, entire PLCP slots including PLCP overhead are written into memory from the receive PLCP framing circuit. The starting buffer address is set by the segmentation/reassembly buffer boundary and the total number of PLCP slots to write is written into the RX_CHECK register which is used as a count in applications when L3_PDU operations are not required. The memory is written at the start of the next PLCP slot after the Transfer Message bit in RX_CTRL is set. Once the memory is filled (as defined by RX_CHECK), a reassembly complete interrupt (STK_STATUS bit 8) is issued and the reassembly block halts until the Transfer Message bit is set again. No reassembly of segments is performed, but the following status counters are updated: HCS check errors, Payload CRC errors, Payload length errors, Invalid Source Address Type, Invalid Destination Address Type, Invalid SMDS Address, and L3 Format Error.

L2_PDU Test mode operates the same as PLCP Test mode except that only the 53 octet L2_PDU from each slot is written to memory and RX_CHECK indicates the number of L2_PDUs to write.

The maximum value that can be written in the RX_CHECK register for each possible reassembly buffer option is given in Table 4.

7.4. End of Reassembly Buffer

The End of Reassembly Buffer register RSM_BUF_END is located at address 09 and is used to indicate the end of the reassembly buffer for L2_PDU Pipeline, Segment Pipeline, and L3_PDU Reassembly modes. The reassembly processor interprets the 16 bits of RSM_BUF_END as the 16 MSBs of the 18 bit address of the top of the reassembly buffer. The reassembly process will reset to the beginning of the reassembly buffer when it reaches this address. The reassembly buffer must be an integral number of segments (26 words for L2_PDU Pipeline and 24 words for Segment Pipeline and L3_PDU Reassembly). This register ensures that the reassembly process and host interface remain segment-aligned in these modes.

The values of the RSM_BUF_END register that are required for the different options on reassembly buffer size are given in Table 5. The first three columns are the beginning address, end address (plus 1), and size of the reassembly buffer. The next two columns are the number of segments that can fit in the given space and the contents of the RSM_BUF_END register for Segment Pipeline, Logical Reassembly, and L3_PDU Reassembly modes. The last two columns are the number of L2_PDUs and the RSM_BUF_END register value for L2_PDU Pipeline mode.

7.5. L2_PDU Pipeline Operation

In L2_PDU Pipeline mode, L2_PDUs are transferred from the receive PLCP to the host interface in the order received. The only processing is to perform HCS checks according to the ATM Mode bit and the Disable HCS check bit. If the check is enabled and the HCS is invalid, the L2_PDU is not sent out of the host interface. The HCS field is stripped out before the message is passed out of the host interface (only 52 octets are passed).

The End of Reassembly Buffer Register RSM_BUF_END (address 09) sets the upper limit of the reassembly buffer. This register is a 16-bit register used to indicate the 16 MSBs of the 18-bit address, and the address is the last word in the buffer. In this mode, the address must be set so that the buffer contains an integral number of 52-octet

L2_PDUs. Table 5 shows the setting for RSM_BUF_END for the options on reassembly buffer size for both L2_PDUs in pipeline mode and segments in both pipeline and reassembly modes.

7.6. Segment Pipeline Operation

In Segment Pipeline mode, 48-octet segments are extracted from L2_PDUs and transferred to the host interface in the order received. There are three levels of validation that can be performed. If only the five-octet L2_PDU header is validated, then all segments with valid headers will be transferred to the host. If all header and SMDS L2_PDU validation is performed, then all valid SMDS segments will be transferred, regardless if they are part of a valid L3_PDU. Finally, "logical reassembly" of L3_PDUs can be performed. This function is described in section 7.9, after the description of the L3_PDU reassembly process below.

The End of Reassembly Buffer Register RSM_BUF_END (address 09) sets the upper limit of the reassembly buffer. This register is a 16-bit register used to indicate the 16 MSBs of the 18-bit address, and the address is the last word in the buffer. In this mode, the address must be set so that the buffer contains an integral number of 48-octet segments; settings for the register are shown in Table 4.

7.7. L3_PDU Reassembly Operations

In L3_PDU Reassembly mode, the reassembly of the level 3 messages or protocol data units (L3_PDUs) from L2_PDUs is performed. Multiple L3_PDUs can be received simultaneously. The reassembly buffer is used to buffer the L2_PDU payloads for each MID until all L2_PDUs for a single MID have been received.

7.7.1. Reassembly Tables

The reassembly process uses three 2 KByte tables of reserved memory at addresses 400-FFF to keep track of the state of a message. Each table has 1024 16-bit entries indexed by MID values. The first table (addresses 400-7FF) contains the address of the first segment for a message . The second table (addresses 800-BFF) contains the segment count (bits 5-15), the sequence number (bits 1-4) and an MID active bit (bit 0). The MID active bits in this table must be initialized to inactive (zero) before reassembly is initiated. The third table (addresses C00-FFF) is reserved for internal use.

7.7.2. L2_PDU Validation

Before the reassembly process does any processing based on the L2_PDU type, it validates the L2_PDU. Control of the L2_PDU header checks is provided by the RX_CHECK register and by the RX_HDR register, which is shown in Figure 7.5.

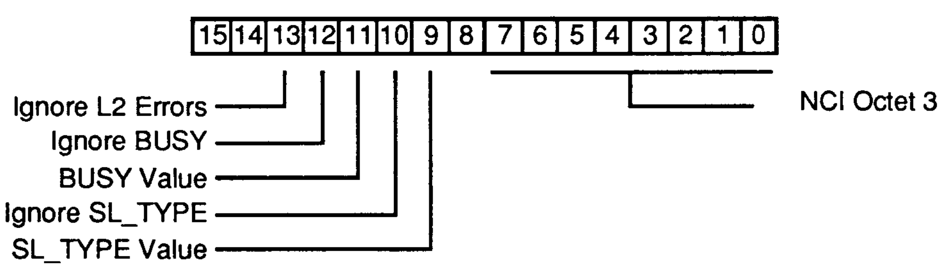


Figure 7.5. RX_HDR Register (address 0C)

These control bits enable the SCARF to be programmed to accept only certain slot types or all slots whether busy or not.

The following checks are performed:

1. The BUSY bit of the ACF is checked, unless Ignore Busy is set. The BUSY bit must be the same as the BUSY Value control bit. Signals reflecting the value of the requests bits in the ACF are generated for the HOB A DQDB state machine in the segmentation block.

2. The SL_TYPE bit is checked unless the Ignore SL TYPE control bit is set. The SL TYPE bit must be the same as the SL TYPE Value control bit.

3. The HCS must be valid, unless Disable HCS Check is set in the RX_CHECK register.

4. Unless Disable Header Check is set in the RX_CHECK register, the first two octets of the Network Control Field must be FFFF, and the third octet of the Network Control Field must be as specified in the NCI field of the Header Validation Field Register RX_HDR.

5. The payload CRC must be valid, unless Disable Payload CRC is set.

6. The payload length must be 0 modulo 4 and be 44 for a BOM or COM, 28-44 for a SSM, and 4-44 for an EOM, unless Disable Payload Length Check is set.

7. The MID must be zero for a SSM, and non-zero for a BOM, COM or EOM, unless Disable MID Check is set.

The checks will be made in the sequence listed above, and only one error will be counted for any L2_PDU, unless checks are disabled; then all disabled checks up to the first enabled check will be counted.

Ignore L2 Errors is a control bit that is effective in Logical Reassembly and Segment Pipeline modes only. It allows all segments to pass to the host regardless of whether or not errors have occurred in the L2_PDU SIP processing. All reassembly status indications will be unaffected, but all segments will pass to the host in the order received.

7.7.3. L3_PDU Validation

Once an L2_PDU has been validated, level 3 checks are performed based on segment type. If the segment is an SSM or BOM, the access class credit manager will also be checked and updated based on the BA-size field of the L3_PDU. This section describes the validation steps, including access class validation in section 7.7.3.5.

7.7.3.1. Single Segment Message

When a SSM segment is received, the following checks occur:

1. Check destination address type valid per IEEE 802.6, section 6.5.1.2.1.

2. Check source address type valid per IEEE 802.6, section 6.5.1.2.1.

3. Check source and destination address type valid per SMDS SIP. See TA-TSY-000774 Issue 3, Section 5.5.1.1.

4. Check destination address SMDS format. See TA-TSY-000774 Issue 3, Section 5.5.1.1.

5. Check source address SMDS format. See TA-TSY-000774 Issue 3, Section 5.5.1.1.

6. Check access-class credit as described in 7.7.3.5.

7. Check BAsize field. The BAsize value must be 0 modulo 4 and be in the range 32 to 9224 (or 65332 if Disable SMDS Length Limit is set in the RX_CTRL register) inclusive.

8. Check HEL field equal to 3.

9. Check for a valid HE field. The requirements for this are given in TR-TSV-000772, section 4.2.1.1.1.

10. Check BEtags. The beginning and end BEtags must match.

11. Check length. The length field must give the length of the message as calculated from the segment count and the payload length field.

12. Check Length field. The length field must match the BAsize field.

7.7.3.2. Beginning of Message

When a BOM segment is received, the following checks occur:

1. Check MID active. If yes, terminate old message with BOM with same MID error and start new reassembly process for current message.

2. Check destination address type valid per IEEE 802.6, section 6.5.1.2.1.

3. Check source address type valid per IEEE 802.6, section 6.5.1.2.1.

4. Check source and destination address type valid per SMDS SIP. See TA-TSY-000774 Issue 3, Section 5.5.1.1.

5. Check destination address SMDS format. See TA-TSY-000774 Issue 3, Section 5.5.1.1.

6. Check source address SMDS format. See TA-TSY-000774 Issue 3, Section 5.5.1.1.

7. Check credit as described in 7.7.3.5.

8. Check BAsize field. The BAsize value must be 0 modulo 4 and be in the range 32 to 9224 (or 65332 if Disable SMDS Length Limit is set in the RX_CTRL register) inclusive.

9. Check HEL field equal to 3.

10. Check for a valid HE field. The requirements for this are given in TR-TSV-000772, section 4.2.1.1.1.

7.7.3.3. Continuation of Message

When a COM segment is received, the following checks occur:

1. Check MID active.

2. Check correct sequence number.

3. Check number of received segments does not exceed BAsize.

7.7.3.4. End of Message

When a EOM segment is received, the following checks occur:

1. Check MID active.

2. Check correct sequence number.

3. Check BEtag check. The beginning and end BEtags must match.

4. Check length. The length field must give the length of the message as calculated from the number of segments received and the payload length field.

5. Check Length field. The length field must match the BAsize field.

7.7.3.5 Access Class Credit Manager

The access class credit manager is used to limit the information rate of L3_PDU messages at DS3 and E3 rates. The algorithm for enforcing the access class on ingress at Switching Systems is given in section 4.3 of TR-TSV-000772. The control of this function is provided by the ACCESS register, shown in Figure 7.6.

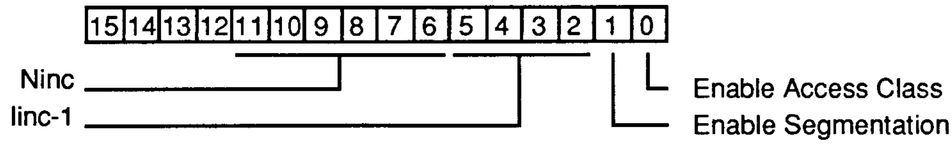


Figure 7.6. ACCESS Register (address 12)

Enable Access Class enables the operation of the access class credit manager. If Enable Segmentation is not set, the access class manager will discard L3_PDUs at reassembly that exceed the access class that is programmed by the parameters Ninc and Iinc-1; the value entered in bits 5-2 of the register is one less than the desired value of Iinc. If Enable Segmentation is set, segmentation of a message will be inhibited until the credit manager has sufficient credit to allow the L3_PDU to be sent.

7.7.4. Memory Full

If a busy L2_PDU arrives when the reassembly buffer is full, the corresponding L3_PDU reassembly process will be terminated and placed on the reassembly-quit stack with the Memory Full bit set to indicate a memory full error. The local processor can read the status entry on the reassembly-quit stack when interrupted to determine the memory full condition.

7.7.5. CRC Checking

Reassembled message queueing for off-line CRC checks is done with the reassembly-quit stack using the host reassembly stack pointer HST_RSM_PTR. When a message has reassembled and the off-line CRC check is enabled, the CRC is checked before transfer to the host, according to the position of the pointer. The off-line CRC is recommended only for DS1 and E1 modes, as it can cause substantial delay in the higher-speed modes.

The concurrent CRC check is done concurrently with transfer to the host. The SCARF can be programmed to interrupt the local processor if the check fails and will inhibit further transfers of reassembled messages to the host until the interrupt is cleared. This allows notification of the errored L3_PDU to the host by the local processor.

7.7.6. Reassembly Initialization

In order for the reassembly process to operate correctly, the buffer area, stack processes, and other reassembly resources must be properly initialized. The following steps are required:

1. Set Disable Reassembly in the RX_CHECK register. This will keep the receiver from trying to enter segments during the reassembly process.
2. Set the buffer size parameters in SYS_CONFIG and the RSM_BUF_END register value as given in Table 5.
3. Set RX_CTRL, RX_CHECK, RX_HDR, and ACCESS to the desired mode for reassembly.
4. Set Clear Reassembly Stack Pointers in the RX_CTRL register. This will reset the reassembly control stack pointers and memory counters, and initialize the reassembly buffer control circuitry to point to the first location in the reassembly buffer.
5. Write hex 0014 to addresses 401-7FF and hex 0000 to addresses 400, 800-FFF and 50-51.
6. Initialize the address screening tables if required (see section 8.2).
7. Read all L3 status registers and error counters in order to initialize them. Enable desired interrupts.

8. Clear the Disable Reassembly control bit. This will allow reassembly operation to start.

7.8. Interrupts and Status Counters

Eleven of the 16-bit status counters listed in Table 3 provide level 2 and level 3 status counts. In addition four counters provide counts of traffic. The address of each counter is given in Table 3. In addition individual interrupts can be set for non-idle L2_PDUs that are received and L2_PDUs that are discarded.

Fig. 7.7 shows the interrupt status register INT_STATUS. Bits 3, 4, and 11-15 relate to the reassembly process.

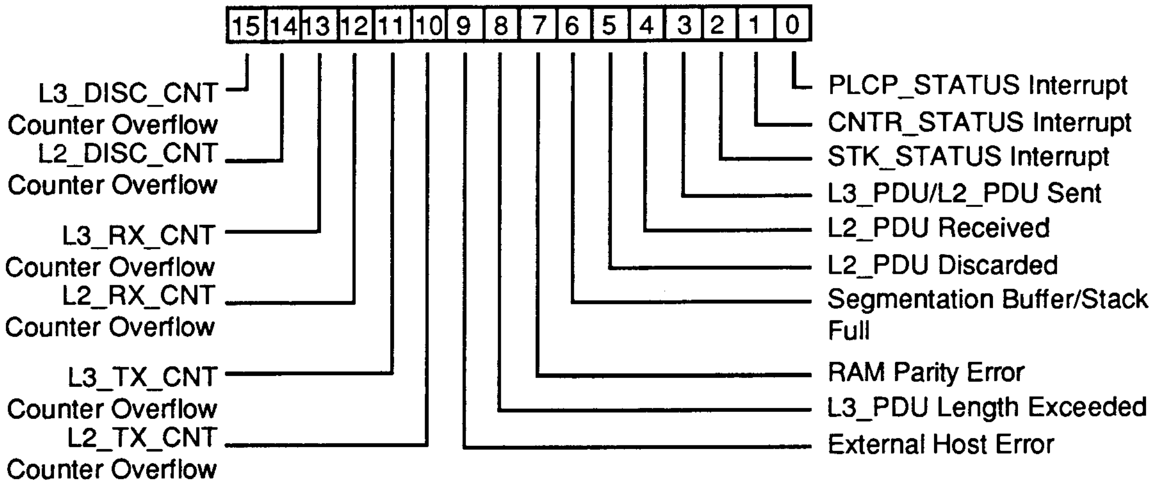


Figure 7.7. INT_STATUS Register (address 22)

There are two interrupts in the INT_STATUS register that related to reassembly of L2_PDUs. These interrupts may be enabled in the EN_INT register with corresponding status bits in the INT_STATUS register. L2 PDU Received indicates the receiver has received a complete active L2_PDU. L2 PDU Discarded indicates an L2_PDU has been discarded due to a format error. These two interrupts are cleared when the INT_STATUS register is read. The possible status errors are counted.

L2_RX_CNT provides a count of all L2_PDUs that are accepted for processing. This count is based on the BUSY and SL_TYPE bits being tested as specified by the RX_HDR register. This count includes discarded L2_PDUs. L2_DISC_CNT is a count of discarded L2_PDUs. This count is incremented when an L2_PDU fails a level 2 check. This count does not include L2_PDUs that are discarded because a sequence count error is detected in the reassembly process.

L3_RX_CNT is a count of all L3_PDUs that are transferred to the host through the host interface. L3_DISC_CNT is a count of all L3_PDUs that either fail to reassemble correctly or are inhibited from transfer to the host because of a CRC failure or an address screening failure (see section 8).

If the corresponding bits of the EN_INT register are set, these four counters will cause interrupts when they overflow. Otherwise the status bit will be set when the counter is full (hex FFFF) and will remain at this value until read.

Figure 7.8 shows the bits of the CNTR_STATUS register and the EN_CNTR_INT register. Bits 4-15 relate to the reassembly process. Each bit is identified by the name of a 16-bit counter that can be read from the addresses given in Table 3; the address of each counter is 3b (hex), where "b" is the bit number in the CNTR_STATUS register.

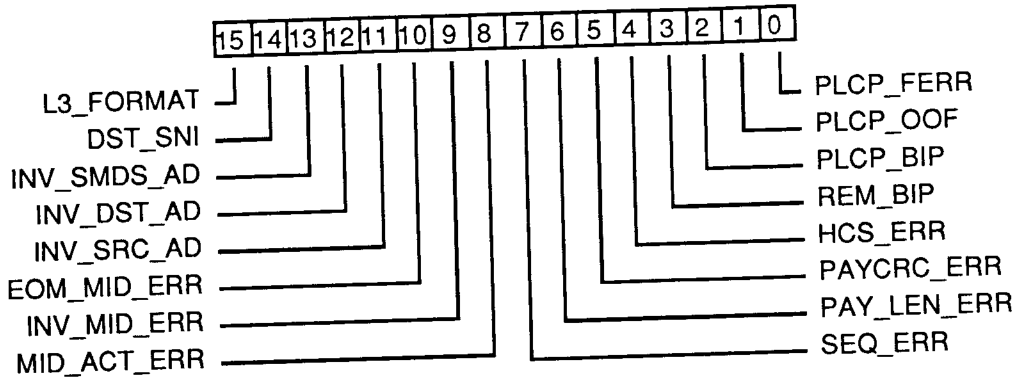


**Figure 7.8. CNTR_STATUS Register (address 23)
EN_CNTR_INT Register (address 1D)**

L2_PDU error counts are provided for header check sequence errors (HCS_ERR), payload CRC errors (PAYCRC_ERR), payload length field errors (PAY_LEN_ERR), and sequence count errors (SEQ_ERR). No more than one of these counters will be incremented on a given L2_PDU, and the checks are performed in the order given here. Errors are counted even if the RX_CHECK register is set to ignore the errors in the processing of L2_PDUs.

For a given L2_PDU with all error checks enabled only one error condition will be recorded. The "precedence" of errors is given in TA-TSY-000774 Issue 3, Section 8. If some error checks are disabled, they will be counted if the check fails, and the first enabled check that fails will be the last error counted.

L3_PDU status counters are provided for BOMs with MIDs that have an active reassembly process (MID_ACT_ERR), L2_PDUs with invalid MID values (INV_MID_ERR), and other L3_PDU format errors (L3_FORMAT). L3_FORMAT errors include invalid BAsize or Length fields, disagreement in these fields, BEtag errors, L3_PDU BAsize exceeded by a COM, address format errors, and HE or HEL field format errors.

Normally no more than one L3_PDU Format error will be counted for a given L3_PDU; if L3_PDU format checks that are normally made in a BOM are disabled, corresponding errors if detected will be counted and a further error in the continuing reassembly process (e.g. BEtag check failure) may also be counted.

There are three counters that provide information about address types. INV_SRC_AD and INV_DST_AD are counts of source and destination addresses respectively that are not valid IEEE 802.6 address types. If both addresses in an L3_PDU have invalid types, only the destination address counter is incremented. INV_SMDS_AD is incremented if the source address type is not an individual 60-bit public address or destination address type is not a 60-bit public address. No more that one count will occur for this counter for a given L3_PDU.

Overflow interrupts may be individually enabled. If a counter is set to interrupt, it will roll over to zero when it reaches its maximum value. If a counter is not set to interrupt, it will saturate when it reaches its maximum value and then will be cleared when read. The interrupt enable bits for the counters at addresses 2A-2E are found in the EN_INT register, with the corresponding interrupt status in the INT_STATUS register. These interrupts are cleared when INT_STATUS is read. The interrupt enable bits for the counters at addresses 30-3F are found in the Counter Interrupt Enable Register EN_CNTR_INT, with the corresponding interrupt status in the CNTR_STATUS register. Figure 7.8 shows the individual bit functions of EN_CNTR_INT. This register is located at address 1D. If one of these interrupts occurs, the Counter Overflow Interrupt bit in the INT_STATUS register will be set. The CNTR_STATUS register can then be read to determine which counter or counters overflowed. These interrupts are cleared when CNTR_STATUS is read.

The remaining reassembly process interrupts can be enabled in the STK_STATUS Interrupt Enable Register EN_STK_INT at address 1F with the corresponding status bits in the status register STK_STATUS at address 25. Figure 7.9 shows the individual bit functions of the STK_STATUS and EN_STK_INT register. If one of these interrupts occurs, the STK_STATUS Interrupt bit in the INT_STATUS register will be set. The STK_STATUS register can then be read to determine the exact interrupt source. The status bits of this register that are used in the reassembly process are described below.

Reassembly Start indicates an SSM or BOM L2_PDU has arrived and reassembly has started. If this bit enables an interrupt, the value of the RSM_START pointer will be latched until it is read. By reading the pointer value twice, the range of pointer values that locate new messages since the last interrupt occurred can be determined.

Reassembly Complete indicates message reassembly and any programmed address screens, off-line CRC check or FCS check have completed for a message. In pipeline or logical reassembly modes, it indicates a segment is ready for output. Address Type indicates that the source or destination address had an address type value which is inconsistent with IEEE 802.6. Address Format/L3 PDU Format indicates that either the address format was not consistent with SMDS service or that an error was detected in the L3_PDU format; the details of the status can be read from the reassembly-quit stack status word. L3 format errors include HE and HEL format errors, BAsize format error, BEtag mismatch, length error, BAsize length mismatch, BAsize exceeded on a COM, and sequence error. Each of these three events will latch the value of the RSM_QUIT pointer if the corresponding interrupt is enabled.

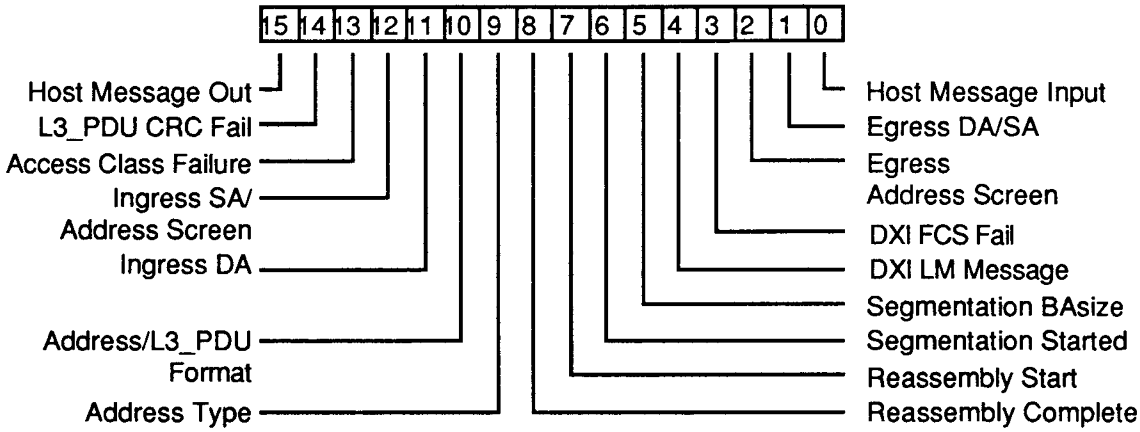


Figure 7.9. STK_STATUS Register (address 25)
EN_STK_INT Register (address 1F)

Ingress DA and Ingress SA/Address Screen indicate address violations or screening failures. The address screening operation is described in section 8. below.

L3 PDU CRC Fail indicates a CRC error on a reassembled L3_PDU; this error will occur only if a CRC check is enabled. Host Message Out indicates that an L3_PDU was transferred to the host. Either of these events will latch the value of HST_RSM_PTR until it is read, and this pointer will identify the specific message affected.

All register contents of STK_STATUS are cleared when the register is read.

7.9. Logical Reassembly Operation

"Logical Reassembly" refers to the application of the reassembly process in analyzing segment content to determine the status of each message that is being reassembled, while forwarding segments in the order received, after they are processed through the L3_PDU validation steps that are a part of the reassembly process. To do this the reassembly mode is set to Logical Reassembly.

The reassembly process functions the same way in Logical Reassembly mode as it does in L3 PDU Reassembly mode. COM and EOM segments are checked for correct sequence numbers and all L3_PDU protocol checks are performed unless disabled in the RX_CHECK register. L3_PDU 32-bit CRC checking is not available in Logical Reassembly mode.

L3_PDU status is still obtained through interaction with the four reassembly pointers. The same status bits are provided as for the case of complete reassembly.

7.10. Local Processor Message Kill

The local processor can halt reassembly of an L3_PDU by writing its address and MID value to locations 400 and 800 respectively. These values are present in the reassembly-start stack. When reassembly is terminated by SCARF, the L3_PDU address and status will be entered on the reassembly-quit stack, with the SSM and Sequence Error status bits both set. Also, location 800 will be written by SCARF to a value of 0.

The Message Kill function can be used by the local processor software to discontinue reassembly of a message that has taken longer than a specified interval to reassemble; this condition is normally caused by the loss of an EOM segment.

7.11 Message Insertion by the Local Processor

The local processor is able to insert a message into the segmentation buffer to be sent out of the host interface. This allows management messages to be sent from the SCARF to the host. This operation is done by inserting the message at the bottom of the unused space in the segmentation buffer and then forcing the message to be sent. This operation uses the Local Processor Message Address Register MESS_ADDR and the Local Processor Message Length Register MESS_LNGTH.

MESS_ADDR is located at address 0D and gives the 16 MSBs of the 18-bit address in buffer RAM of a message to be sent out of the host interface. The message is sent out when the Insert Message bit in the RX_CTRL register is written. The memory for the message must be allocated by the local processor.

MESS_LNGTH is located at address 0E and gives the number of words in a message to be sent out of the host interface. If SMDS DXI mode is enabled in the RX_CTRL register, this length does not include the FCS field at the end of the message. The local processor must allocate space for the FCS field at the end of the message. If SMDS DXI mode is enabled, the FCS field will be added to the message before it is sent out of the host interface. The message header required for the DXI mode is not provided by the SCARF and must be inserted by the local processor as a part of the message generation.

The detailed procedure is as follows:

1. Read the current value of the segmentation stack pointer SEG_STK_PTR.
2. Read the address of the message to which SEG_STK_PTR points.
3. Write the message into the segmentation buffer so that it ends at the location just before the address of the beginning of the L3_PDU currently being transmitted.
4. Set MESS_ADDR and MESS_LNGTH to the appropriate values.
5. Set Insert Message in RX_CTRL. This will cause the message to be transferred to the host.

The only other processing to be done is to ensure that the host processor does not overwrite the buffer space when the buffer pointer is "backed up" to allow the transmission of the L3_PDU inserted by the local processor. This can be done by monitoring the value of the HST_SEG_PTR or by disabling host message transfer if required.

8. ADDRESS SCREENING

Address screening is included to provide the Switching System (SS) features in section 3 of TR-TSV-000772 Issue 1. These features are also useful for CPE in identifying specified "loopback" codes, for separating reassembled messages when SCARF multiplexing is used, and for test applications.

There are six address screening functions that are implemented in the SCARF, three for egress messages and three for ingress messages. (Ingress messages have been reassembled and egress messages are for segmentation.) For egress the functions are:

1. Source Address Violation: The source address is checked against the list of individual addresses assigned to the SNI. A match results in a source address violation, and the L3_PDU is discarded. This is part of requirement 3-13 of TR-TSV-000772 Issue 1 (Section 3.2.5.2).

2. Destination Address Validation: An individual destination address is checked against the list of individual addresses assigned to the SNI. A group destination address is checked against the list of group addresses which identify the SNI. The destination address validation fails if a match is not found, and the L3_PDU is discarded. A match also yields the individual screen number (1 of up to 4) to be used in screening the source address. This is requirement 3-1 of TR-TSV-000772 Issue 1 (Section 3.2.1).

3. Source Address Screen: The source address is checked against the addresses in the individual screen determined by the screen number from function 2. Each screen can be set for allowed or disallowed operation. If allowed, the screen fails if the source address does not match any members of the screen. If disallowed, the screen fails if the source address matches any member of the screen. IF the screen fails the message is discarded. This is requirement 3-27 of TR-TSV-000772 Issue 1 (Section 3.2.6.5).

The ingress functions are:

1. Destination Address Violation: An individual destination address is checked against the list of individual addresses assigned to the SNI. A match results in a destination address violation. This is requirement 3-3 of TR-TSV-000772 Issue 1 (Section 3.2.2).

2. Source Address Validation: The source address is checked against the list of individual addresses assigned to the SNI. The source address validation fails if a match is not found. A match also yields the individual screen number (1 of up to 4 for a individual group destination address) or the group screen number (1 of up to 4 for a group destination address) to be used in screening the destination address. This is requirement 3-8 of TR-TSV-000772 Issue 1 (Section 3.2.4).

3. Destination Address Screen: An individual destination address is checked against the individual addresses in the screen determined by the screen number from function 2. A group destination address is checked against the group addresses in the screen determined by the screen number from function 2. Each screen can be set for allowed or disallowed operation. If allowed, the screen fails if the destination address does not match any members of the screen. If disallowed, the screen fails if the source address matches any member of the screen. This is requirements 3-24, 3-25, and 3-26 of TR-TSV-000772 Issue 1 (Section 3.2.6.4).

There are two address lists in the address screening area of buffer RAM: a list of up to 128 SNI addresses (individual addresses assigned to the SNI and group addresses which identify the SNI) at 1800-19FF hex and a list of up to 128 addresses (group and individual) which are members of an address screen (1A00-1BFF hex).

Each address entry is stored in four words (eight octets) and includes the entire 64-bit address including the address type subfield. The first word of the entry contains the two least significant octets of the address (bits 0-15 where 0 is least significant bit) with the SMDS transmission octet ordering preserved (more significant octet in most significant bits of word). The second word of the entry contains bits 16-31 of address, the third word contains bits 32-47 of the address, and the fourth word contains bits 48-63 of the address.

8.1. Control

Reassembled message queueing for address screening is done with the reassembly-start stack using the address screen stack pointer ADR_RSM_PTR. Segmentation message queueing for address screening and SMDS DXI FCS checks is done with the segmentation stack using the address screen stack pointer ADR_SEG_PTR.

The control of the address screening functions is in the Address Screen Control Register ADR_SCR. Figure 8.1 shows the individual bit functions of ADR_SCR. This register is located at address 11.

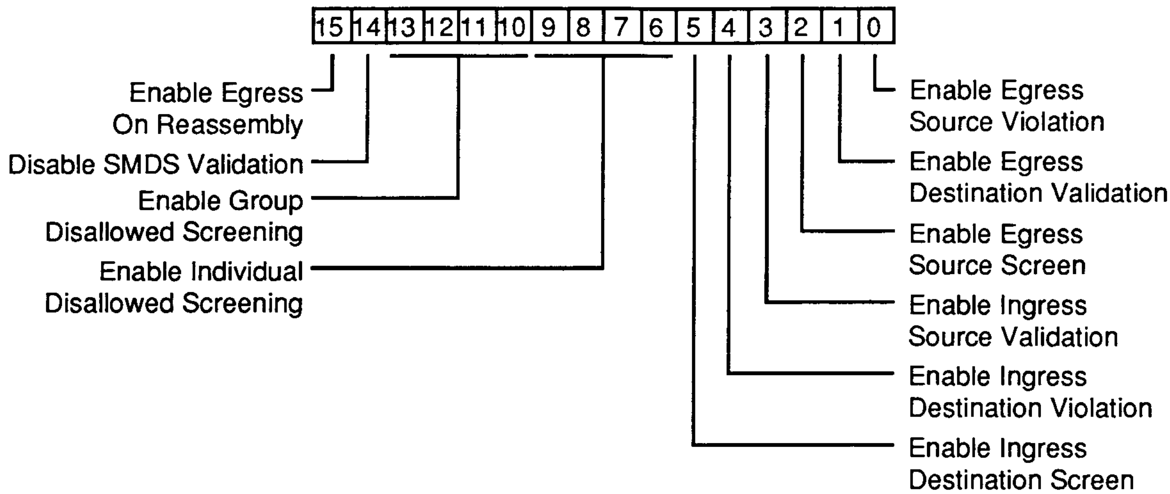


Figure 8.1. ADR_SCR Register (address 11)

Enable Egress Source Violation causes egress L3_PDUs to be discarded when the source address matches one of the individual addresses assigned to SNI.

Enable Egress Destination Validation causes egress L3_PDUs to be discarded when the destination address does not match one of the individual addresses assigned to SNI.

Enable Egress Source Screen enables the source address screen for egress L3_PDUs.

Enable Ingress Source Validation causes ingress L3_PDUs to be discarded when the source address does not match one of the individual addresses assigned to the SNI.

Enable Ingress Destination Violation causes ingress L3_PDUs to be discarded when the destination address matches one of the individual addresses assigned to SNI .

Enable Ingress Destination Screen enables the destination address screen for ingress messages.

Enable Individual Disallowed Screening causes messages whose addresses are found in the screen to be disallowed. Otherwise only messages whose address are found in the screen are allowed. These bits set the disallowed/allowed state for each individual screen (bit 6 for screen number 1 through bit 9 for screen number 4).

Enable Group Disallowed Screening causes messages whose addresses are found in the screen to be disallowed. Otherwise only messages whose address are found in the screen are allowed. These bits set the disallowed/allowed state for each group screen (bit 10 for screen number 1 through bit 13 for screen number 4).

Disable SMDS Validation causes the address screen to be run on the entire eight-octet address rather than just on the six octets (three most significant words) that correspond to a valid SMDS address. This will allow the screening of non-US addresses.

Enable Egress on Reassembly causes egress address screening functions to be run on reassembled messages and the ingress address screening functions to be run on messages to be segmented. This function is useful in test equipment applications. Otherwise, egress functions are run on messages to be segmented and ingress functions are run on reassembled messages. Note that this mode changes the stack locations that must be referenced to determine the status of the screen of a particular message.

If the egress destination validation or the egress source-address screen are run, then the egress source screen will be run as well (whether the control bit is set or not) in order to find the proper group on which to run these screens. If there is a source violation, the address screen will not be run. Similarly, the ingress source validation screen will be run if the ingress destination violation or ingress destination screen is requested. If the source validation fails, the destination screen will not be run.

8.2. Initialization

Address screening in the SCARF is done with open hashing tables. There are two tables: one used for SNI address validation and violations (1000-13FF hex), and one used for address screens (1400-17FF hex). Each table has 1024 16-bit entries. In addition, there is a chain entry of 16 bits for every address list entry. These chaining entries are located at (1C00-1C7F hex) for the SNI addresses, and (1C80-1CFF) for the screen addresses. Each 16-bit entry in the hash tables and chain lists contains four unused MSB's (bits 12-15), a four bit screen number field (bits 8-11), a entry valid bit (bit 7) and an address number (bits 0-6). Each address list entry is assigned an address number of 0-127 according to its position in either the SNI or the screen list.

The screen number field is used to associate each address with screen numbers. For entries in the SNI hash table and chain, bits 8 and 9 give the individual screen number (0-3) to be used for individual screens and bits 10 and 11 give the group screen number (0-3) to be used for group screens when the associated address (indicated by the address number field) is the source address on ingress messages or the destination address on egress messages. For entries in the address screen hash table and chain, bit 8 indicates the entry is a member of screen number 0, bit 9 a member of screen number 1, bit 10 a member of screen number 2 and bit 11 a member of screen number 3.

The hashing function used consists of two steps. First, each word of the address (16 bits) is added (with bit 17 carry ignored) to the 16-bit value of the HASH_CONST register at memory address 10 (hex). The value of HASH_CONST may be adjusted so that few addresses have the same hash function value. The four resultant words are then processed by the L2_PDU payload CRC function in the normal SMDS transmission order to yield a 10-bit hash value. If Disable SMDS Validation is not set, this process is run only on the first six octets of the address; otherwise it is run on all eight octets.

The initialization steps required are:

1. Store the address list members.

2. Initialize the entry-valid bit for all hash table and chain entries to 0.

3. For each member of the SNI address lists (1800-19FF) with address number b:
   Compute Hash value h
   Read h^{th} entry of SNI hash table (1000-13FF) to get valid bit and address num n
   If entry-valid bit not set
      Set screen number, valid bit and address number b in h^{th} entry of SNI hash table
   Else While entry valid bit set
         Read n^{th} entry of SNI chain (1C00-1C7F) to get valid bit and address num n
      End While
      Set screen number, valid bit and address number b in n^{th} entry of SNI chain
   End If

4. For each member of the screen address list (1A00-1BFF) with address number b:
   Compute Hash value h
   Read h^{th} entry of screen hash table (1400-17FF) to get valid bit and address num n
   If entry-valid bit not set
      Set screen number, valid bit and address number b in h^{th} entry of screen hash table
   Else While entry valid bit set
         Read n^{th} entry of screen chain (1C80-1CFF) to get valid bit and address num n
      End While
      Set screen number, valid bit and address number b in n^{th} entry of screen chain
   End If

8.3 Interrupts and Status

Address screening interrupts can be enabled in the STK_STATUS Interrupt Enable Register EN_STK_INT at address 1F with the corresponding status bits in the Stack Interrupt Status Register STK_STATUS at address 25. Figure 8.2 shows the individual bit functions of the STK_STATUS register and the EN_STK_INT register. Each bit of the EN_STK_INT enables the corresponding status bit to interrupt the local processor.

If one of these interrupts occurs, the STK_STATUS Interrupt bit in the INT_STATUS register will be set. The STK_STATUS register can then be read to determine the exact interrupt source. The status bits of this register that are used in the address screening are described below.

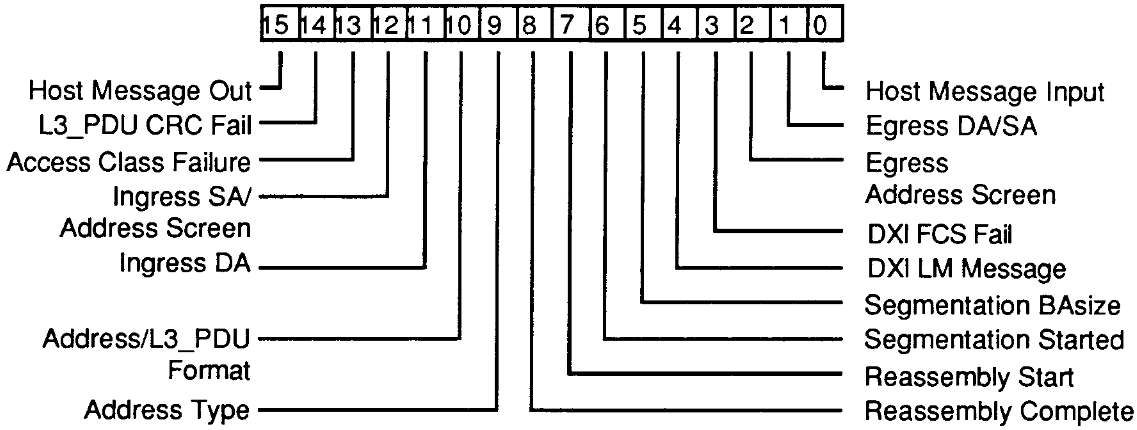


Figure 8.2. STK_STATUS Register (address 25)
EN_STK_INT Register (address 1F)

Egress DA/SA indicates that either the source address of the L3_PDU is in the SNI Source Address list or that the Destination Address is not in the SNI individual or group addresses. Egress Address Screen indicates that the egress address screen has failed. If the interrupt for one of these status bits is enabled, the value of the ADR_SEG_PTR will be latched unless Enable Egress On Reassembly is set, in which case ADR_RSM_PTR will be latched.

Ingress DA indicates that the destination address of an ingress message is assigned to the source. This indicates "local traffic" that should not be forwarded. This condition is also counted. Ingress SA/Address Screen indicates that either the source address is not in the SNI list or that the ingress address screen has failed. If the interrupt for one of these status bits is enabled, the value of the ADR_RSM_PTR will be latched unless Enable Egress On Reassembly is set, in which case ADR_SEG_PTR will be latched.

Note that both the ingress and egress STK_STATUS bits are arranged so that interrupts can be generated only on those events that are to be "logged" according to TA-TSV-000774.

All STK_STATUS register contents are cleared when the register is read.

One counter is provided for address screening status, as shown in Table 3. DST_SNI provides a count of ingress destination addresses that are individual addresses listed in the source address table. This counter is located at address 3E.

In the segmentation direction, messages in the segmentation buffer that failed an address screen can be located by the ADR_SEG_PTR value. If an address screening failure (or a SMDS DXI FCS failure) occurs, the status is written to the segmentation stack message length location. At the time this is done, the value of the ADR_SEG_PTR is latched if the corresponding STK_STATUS bit is programmed to enable an interrupt. To determine which message failed the screen, the value of this pointer can be read, and the message length value read from the buffer RAM. If the length is less than eight, an address screen failure occurred. If length is 32768, an SMDS DXI FCS failure occurred. Length 4 indicates a screen failure, length 2 indicates a destination validation/violation failure, length 1 indicates a source validation/violation failure. Once the status has been obtained, the pointer value can be read again to determine the current pointer location. Any intermediate message status words should also be checked to see if any other screening failures have occurred while the local processor was processing the initial interrupt.

The status word (see Figure 7.3) of the reassembly-start stack gives the address screening failures in the reassembly direction on a per message basis. Note that even though the message failed the address screen, in L3 PDU Reassembly mode it will complete reassembly with the rest of the status indications provided. Transfer to the host will always be inhibited, however.

9. ELECTRICAL CHARACTERISTICS

9.1. Pinout Description

Figure 9.1 is a package pinout diagram for the SMDS Control and Reassembly Formatter. The package is a 160-pin plastic quad flat pack (PQFP). The pin names and functions are shown in the following table: A list of the physical pinouts is also given in Table 6 for reference.

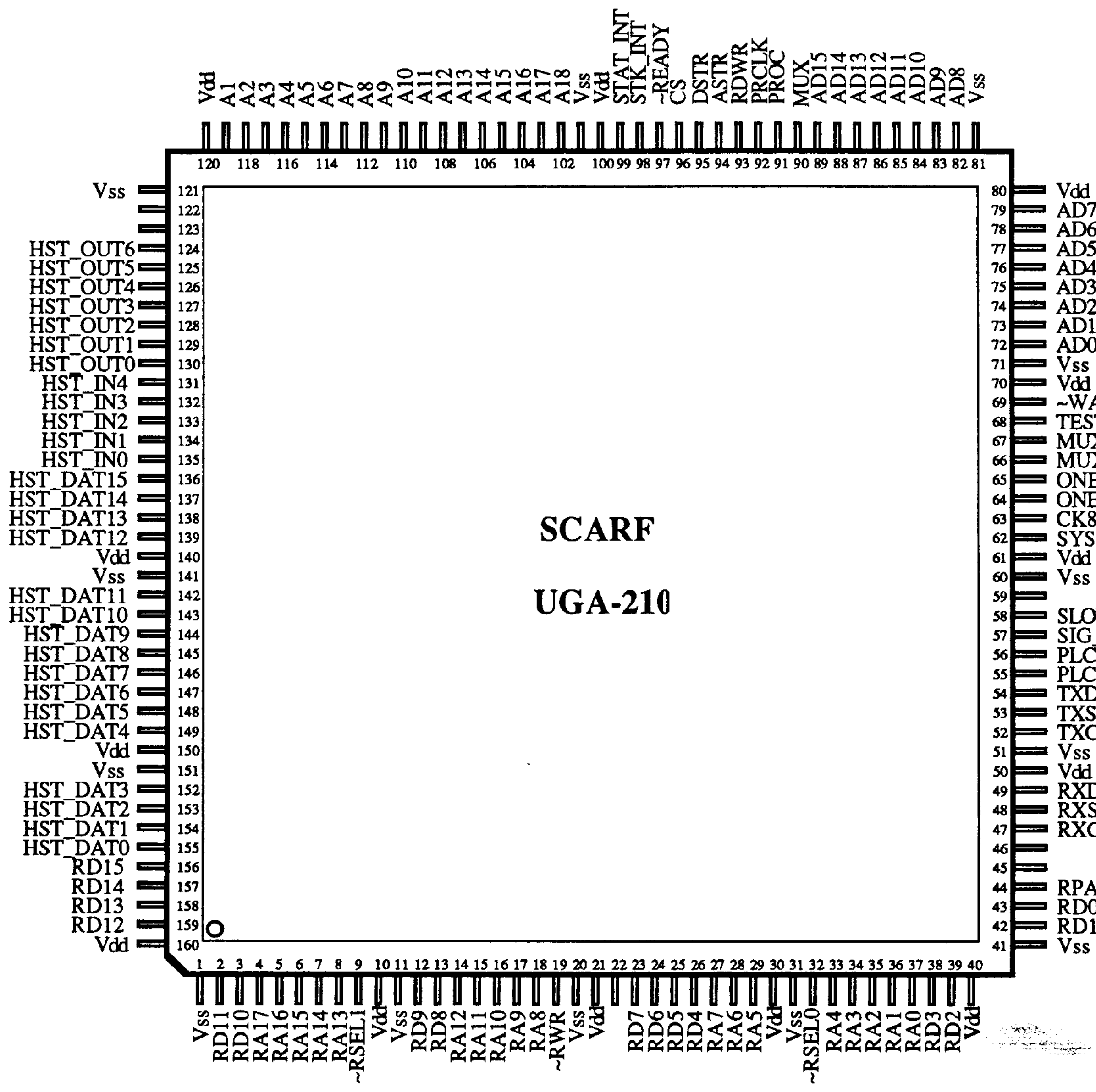


Figure 9.1. SCARF Pinout Diagram

Name	Type	Function	Reference
MUX	Input	Selects multiplexed address/data on pins AD15-AD0 when high.	2.1
PROC	Input	Processor Select.	2.1
PRCLK	Input	Processor Clock.	2.1
CS	Input	Chip select; must be logic high.	2.1
RDWR	Input	Read/Write Control.	2.1
ASTR	Input	Address Strobe or Address Latch Enable.	2.1
DSTR	Input	Data Strobe.	2.1
A18-A1	Input	Address input bus.	2.1
AD15-AD0	Bidirect	Multiplexed address/data bus.	2.1
STK_INT	Output; OD w/ pullup	Stack-function interrupt for either segmentation or reassembly.	2.2
STAT_INT	Output; OD w/ pullup	Status interrupt for either alarm conditions, error events, or counter overflows.	2.2
SYSCKI	Input	System clock; used to clock buffer RAM.	3.1
8KCKI	Input	8-kHz reference clock. Can be used to synchronized transmit PLCP and to provide reference for one-second counter.	3.1
SIG_FRZ	Input	When enabled and high, disables all L2_PDU and L3_PDU reassembly functions.	4.1
ONESECI	Input	One-second counter synchronization input. To synchronize one-second status counters of multiple SCARFs and framers, all one-second inputs should be tied to the same clock source.	3.1, 4.1
ONESECO	Output	One-second output derived from count of current 8-kHz frame reference (receive PLCP or 8KCKI).	3.1
MUXPRIN	Input	Multiplex priority input; if enabled high signal allows transmission of an L2_PDU	4.11
MUXPROUT	Output	Multiplex priority output; high if MUXPRIN is high and no L2_PDU is queued or if L2_PDU was sent in the previous slot.	4.11
TEST0	Input	Test input; connect to ground for normal operation.	1.5
~WAIT	Input	External ~READY input	2.1
HST_DAT15-HST_DAT0	Bidirect	Host interface data bus.	5.1
HST_IN4-HST_IN0	Input	Host interface clock and control inputs.	5.1
HST_OUT6-HST_OUT0	Output	Host interface clock and control outputs.	5.1
~RSEL0	Output	RAM select-bar signal; low to enable a RAM operation.	3.2
~RSEL1	Output	RAM select-bar signal; low to enable a RAM operation.	3.2
~RWR	Output	RAM write-bar signal; low to enable a write operation, high to enable a read operation.	3.2
RA17-RA0	Output	RAM address bus.	3.2
RD15-RD0	Bidirect	RAM data bus.	3.2
RXCKI	Input	PLCP receive clock input	4.2
RXSYI	Input	PLCP receive sync input.	4.2
RXDATI	Input	PLCP receive clock input.	4.2
TXCKI	Input	PLCP transmit clock input.	4.2
TXSYI	Input	PLCP transmit sync input.	4.2
TXDATO	Output	PLCP transmit data output.	4.2
PLCPSYO	Output	PLCP frame synchronization output.	4.2
SLOTSYO	Output	PLCP slot synchronization output.	4.2
PLCP_OOF	Output	PLCP out-of-frame indication.	4.6

9.2. Power Requirements and Temperature Range

The SCARF will meet all specifications over a temperature range of 0°C to 70°C and input voltage range of 4.75 to 5.25 Volts. The maximum current required for the circuit in operation is [TBD].

9.3. DC Characteristics

All input and bidirectional pins have input thresholds compatible with TTL drive levels. Leakage current for each pin is less than 10 µA in any state.

All output and bidirectional pins have drive current I_{OL} = 4 mA at 0.4 Volts and I_{OH} = -4 mA at 2.4 Volts except the interrupt pins which are open drain and require an external pullup resistor. All output and bidirectional pins have CMOS drive levels and can be used with CMOS or TTL logic.

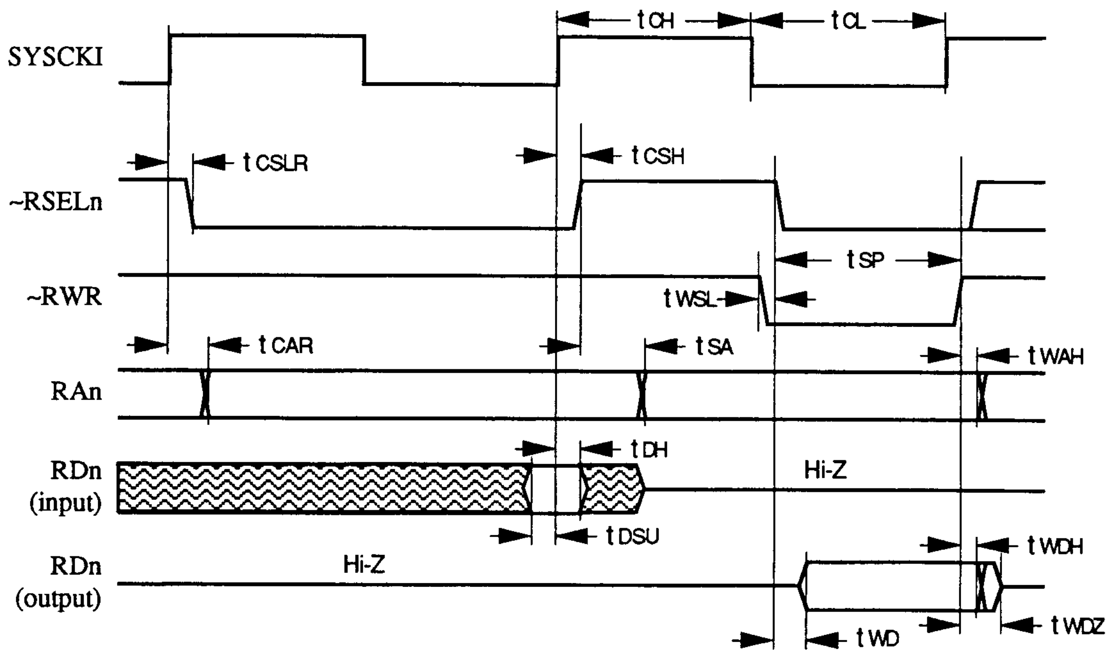
9.4. AC Characteristics

9.5. RAM Interface Timing Specification

The RAM interface is designed to connect directly to common families of high-speed static RAM, in configurations of 32Kx8, 64Kx4, 128Kx8, and 256Kx4. These RAMs are available with read access times as low as 12 ns.

The timing specifications for the RAM interface are given in Figure 9.2. The system clock frequency is basically at the option of the designer. It must be at least 0.44 times the peak line frequency of the PLCP clock rate for the circuit to operate properly and can be no higher that 33 MHz.

The critical RAM timing parameters are the read access time and the write pulse width. The RAM access time must be 15 ns less than the system clock period. The write pulse width must not be greater than the low period of the system clock.



Symbol	Parameter	Min	Max	Units
t_{CL}	Clock Pulse Width Low	15.0	-	ns
t_{CH}	Clock Pulse Width High	15.0	-	ns
t_{CSLR}	Delay from SYSCKI to RAM-select lead low (Read Operation)	2.0	8.5	ns
t_{CAR}	Delay from SYSCKI to Address (Read Operation)	3.5	15.0	ns
t_{DSU}	Data Setup time to SYSCKI high required.	0.	-	ns
t_{DH}	Data Hold time from SYSCKI high required.	-	3.	ns
t_{SA}	Delay from Select-bar High to Address (Write Operation)	2.5	9.0	ns
t_{CSH}	Delay from SYSCKI to RAM-select lead high (Write Operation)	2.0	8.0	ns
t_{WSL}	Delay from Write-bar low to RAM-select low	0.0	-	ns
t_{WD}	Delay from Write-bar low to Write Data Lo-Z, Valid	1.0	3.5	ns
t_{SP}	Select Pulse Width (Write Operation) (Logic OR of ~RSELn, ~RWR)	t_{CL}	t_{CL}+1	ns
t_{WAH}	Address Hold from Write-bar High	1.0	-	ns
t_{WDH}	Data Hold from Write-bar High	1.0	-	ns
t_{WDZ}	Data Hi-Z from Write-bar High	2.0	6.5	ns

Figure 9.2 RAM Timing Specification

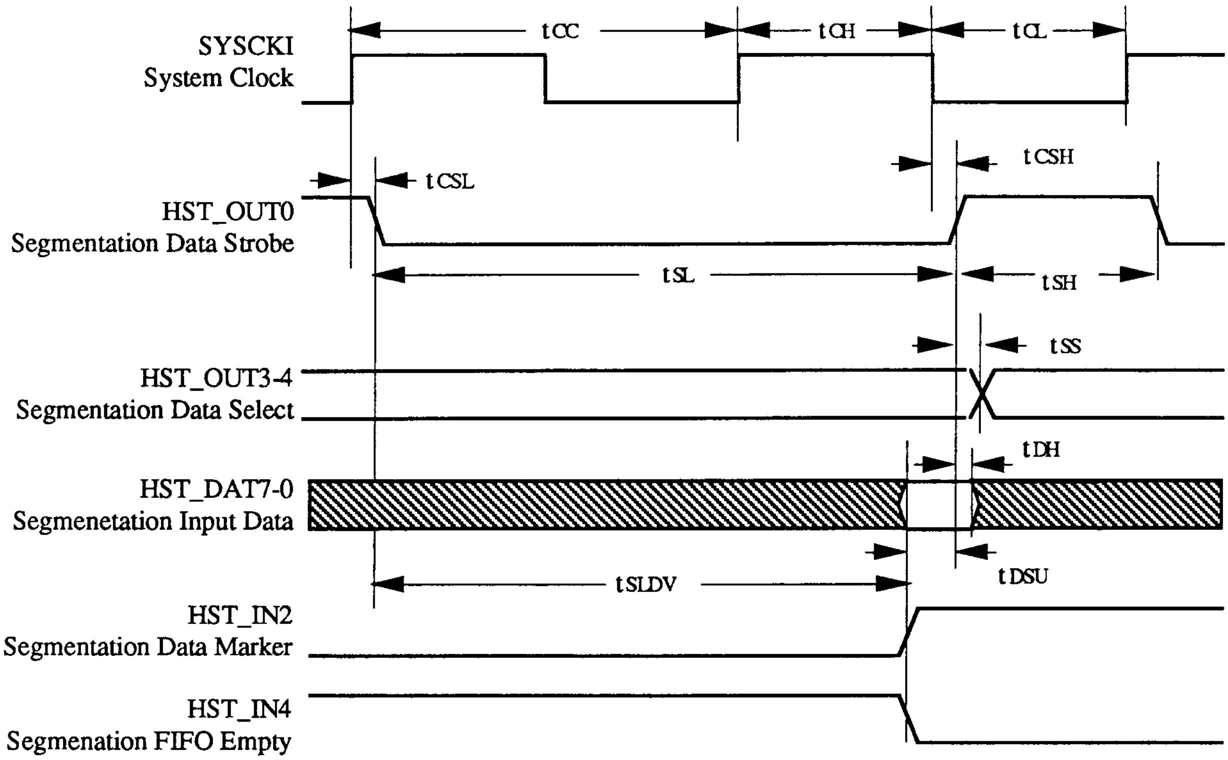
9.6. Host Interface Timing

The host interface operates in multiple modes, each with its own timing specification. The timing information for each mode is given below:

9.6.1 Octet Expansion Mode Timing

The octet expansion mode is provided to allow direct interfaces to catalog FIFOs and dual-port RAMs. Octets are transferred in both the reassembly and segmentation directions.

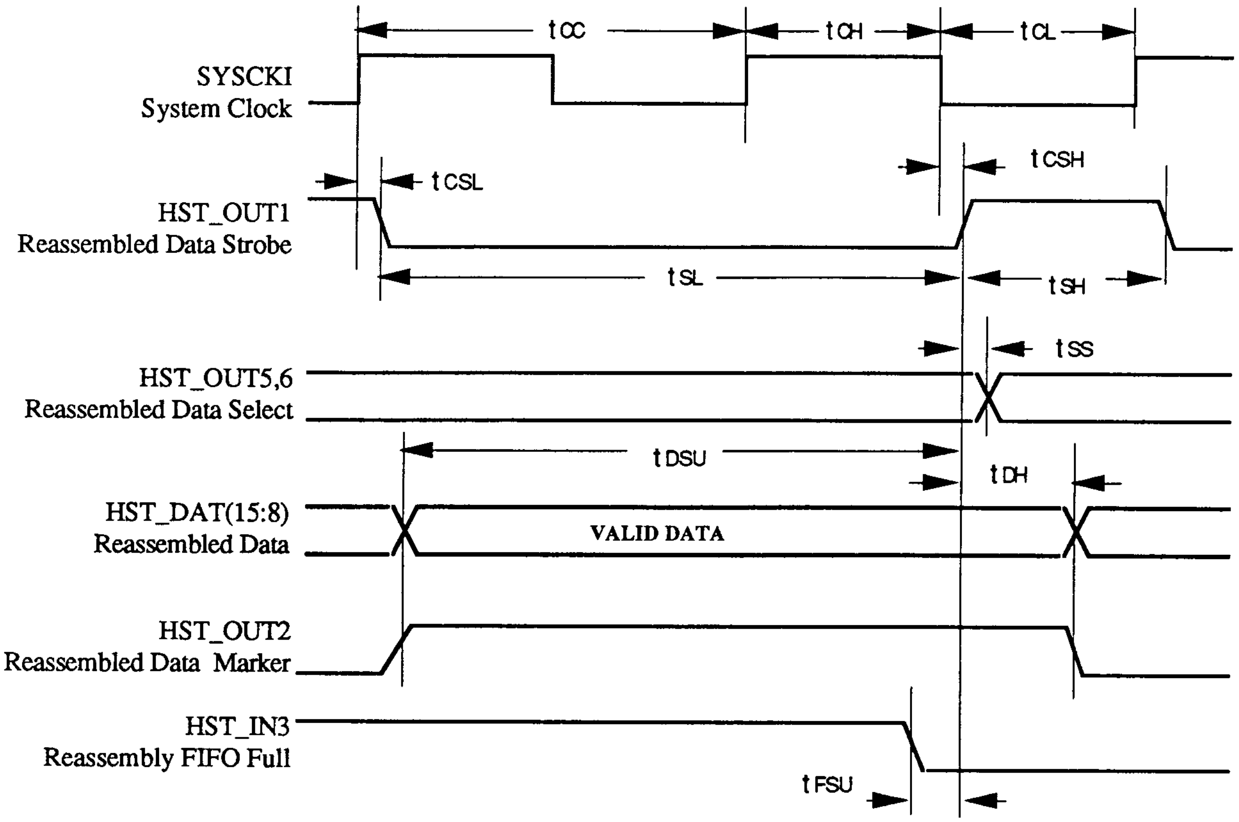
Figure 9.3 gives the timing specifications for the segmentation direction.



Symbol	Parameter	Min	Max	Units
t_{CL}	Clock Pulse Width Low	15.0	-	ns
t_{CH}	Clock Pulse Width High	15.0	-	ns
t_{CC}	Clock cycle time	30.0	-	ns
t_{CSL}	Delay from SYSCKI rising to STROBE low	3	13	ns
t_{CSH}	Delay from SYSCKI falling to STROBE high	3	13	ns
t_{SL}	STROBE low width	0.75 x t_{SC}	-	ns
t_{SH}	STROBE high width	0.25 x t_{SC}	-	ns
t_{SS}	Delay from STROBE high to SEL(1:0) valid	3	6	ns
t_{DH}	Data hold time from STROBE rising	0.0	-	ns
t_{DSU}	Data setup time to STROBE rising	10	-	ns
t_{SLDV}	STROBE low to data valid delay (t_{ACC} of fifo)	-	35	ns
t_{SC}	STROBE cycle time	2 x t_{CC}	-	ns

Figure 9.3 Octet Segmentation Timing Specification

Figure 9.4 gives the timing diagram for the reassembly direction. In this case, data is being transferred to the host. Note that in each case the data strobes are provided by the SCARF output.



Symbol	Parameter	Min	Max	Units
t_{CL}	Clock Pulse Width Low	14.0	-	ns
t_{CH}	Clock Pulse Width High	14.0	-	ns
t_{CC}	Clock cycle time	30.0	-	ns
t_{CSL}	Delay from SYSCKI rising to STROBE low	3	13	ns
t_{CSH}	Delay from SYSCKI falling to STROBE high	3	13	ns
t_{SL}	STROBE low width	0.75 x t_{SC}	-	ns
t_{SH}	STROBE high width	0.25 x t_{SC}	-	ns
t_{SS}	Hold from STROBE high to SEL(1:0) change	3	6	ns
t_{DH}	Data hold time from STROBE rising	17	-	ns
t_{DSU}	Data setup time to STROBE rising	30	-	ns
t_{SC}	STROBE cycle time	2 x t_{CC}	-	ns
t_{FSU}	/FF setup time to STROBE rising (/FF active on write of last location)	20	-	ns

Figure 9.4. Octet Reassembly Timing Specification

TABLE 1.

SMDS CONTROL AND REASSEMBLY FORMATTER

LOCAL PROCESSOR ADDRESS MAP

Control and Status Registers			
Address (hex)	Name	Allowed Operations	Reference
00-12	Control Registers	Read and Write	Table 2
13-1B	(unused)		
1C-1F	Interrupt Enable Control Registers	Read and Write	Table 2
20-25	Status Registers	Read Only	Table 3
26-29	(unused)		
2A-2F	L2_PDU and L3_PDU Counters	Read Only	Table 3
31-34	PLCP Error Counters	Read Only	Table 3
35-3F	Reassembly Error Counters	Read Only	Table 3
40-46	Stack Pointers	Read Only	Table 3
48	Local Processor Host Mode	Read and Write	5.1.3
Buffer RAM			
Address (hex)	Name	Allowed Operations	
50-8F	(unused)		
90-9F	Level 2 Overhead Generation	Read and Write	6.1 - 6.5
A0-BF	Level 3 Overhead Generation	Read and Write	6.5.1, Fig. 6.3
C0-DF	Transmit Protocol Header Generation	Read and Write	6.5.2
E0-FF	Receive Protocol Header Generation	Read and Write	7.1
100-1FF	Segmentation Stack	Read and Write	6.5.3, Fig. 6.6
200-2FF	Reassembly-start Stack	Read and Write	7.2
300-3FF	Reassembly-quit Stack	Read and Write	7.2
400-FFF	Reassembly Tables	Read and Write	7.7.1
1000-1FFF	Address Screening	Read and Write	8.2
2000-3FFFF	Segmentation and Reassembly Buffers	Read and Write	3.1

TABLE 2.

SMDS CONTROL AND REASSEMBLY FORMATTER

LOCAL PROCESSOR CONTROL REGISTERS

Address	Name	Function	Reference
00	SYS_CONFIG	System Configuration	3.1, Fig. 3.1
01	PLCP_CTRL	PLCP Mode and Control	4.1, Fig. 4.1
02	TX_BIP8	Transmit BIP-8 Error Insertion	4.5, Fig. 4.9
03	TX_L2_CTRL	L2_PDU Transmission Control	6.1, Fig 6.1
04	TX_L3_CTRL	L3_PDU Format Control	6.5.1, Fig. 6.3
05	TX_PROT	Protocol Control	6.5.2, Fig. 6.5
06	RX_PLCP_CTRL	PLCP Receiver Control	4.1, Fig. 4.2
07	RX_CTRL	L2_PDU and L3_PDU Receiver Control	7.1, Fig. 7.1
08	RX_CHECK	Receiver L2_PDU and L3_PDU Validation	7.1, Fig. 7.2
09	RSM_BUF_END	End of Reassembly Buffer	7.4
0A	HOST_CTRL	Host Interface Control	5., Fig. 5.1
0B	M1_M2	M1 and M2 fields of Transmit PLCP	4.5, Fig. 4.10
0C	RX_HDR	Receive Header Validation Field	7.7.2, Fig. 7.5
0D	MESS_ADDR	Local Processor Message Address	7.11
0E	MESS_LNGTH	Local Processor Message Length	7.11
0F	BWB_MOD	Bandwidth-balancing Modulus	6.1, Figure 6.2
10	HASH_CONST	Hashing Function Randomizer	8.2
11	ADR_SCR	Address Screen Control	8.1, Fig. 8.1
12	ACCESS	Access Class Credit Manager Control	7.7.3.5, Fig. 7.6
1C	EN_INT	Interrupt Enable Register	2.6 Fig. 2.4
1D	EN_CNTR_INT	Counter Interrupt Enable Register	4.9, Fig. 4.13, Fig 7.8
1E	EN_PLCP_INT	PLCP Status Interrupt Enable Register	4.8, Fig. 4.11
1F	EN_STK_INT	STK_STATUS Interrupt Enable Register	6.5.3, 7.8, Fig. 7.9, 8.2

TABLE 3.

SMDS CONTROL AND REASSEMBLY FORMATTER

STATUS REGISTERS AND COUNTERS

Address	Name	Function	Reference
20	BEtag	Transmit BEtag Field	6.5.1, Fig. 6.4
21	VERSION	Part Number/Version Number	2.5, Fig. 2.2
22	INT_STATUS	Interrupt Status	2.6 Fig. 2.3
23	CNTR_STATUS	Counter Interrupt Status	2.6, 4.9
24	PLCP_STATUS	Framer/PLCP Interrupt Status	4.8, Fig. 4.11
25	STK_STATUS	Stack Interrupt Status	6.5.3, Fig. 6.6, 7.9, 8.2
26	RSM_LNGTH	Length of Reassembled Message	5.1
2A	L2_RX_CNT	Count of L2_PDUs with BUSY = Busy Value	7.8
2B	L2_DISC_CNT	Count of Discarded L2_PDUs with BUSY = BUSY Value	7.8
2C	L2_TX_CNT	Count of Transmitted L2_PDUs	6.6
2D	L3_RX_CNT	Count of Reassembled L3_PDUs	7.8
2E	L3_DISC_CNT	Count of Discarded L3_PDUs	7.8
2F	L3_TX_CNT	Count of Transmitted L3_PDUs	6.6
30	PLCP_FERR	Count of PLCP Frame Errors	4.9
31	PLCP_OOF	Count of PLCP OOF Events	4.9
32	PLCP_BIP	Count of PLCP BIP-8 Errors	4.9
33	REM_BIP	Count of Remote BIP-8 Errors	4.9
34	HCS_ERR	Count of HCS Error Violations	7.8
35	PAYCRC_ERR	Count of Payload CRC Errors	7.8
36	PAY_LEN_ERR	Count of Payload Length Errors	7.8
37	SEQ_ERR	Count of Payload Sequence Number Errors	7.8
38	MID_ACT_ERR	Count of BOMs Received for Active MID	7.8
39	INV_MID_ERR	Count of Invalid MID Errors	7.8
3A	EOM_MID_ERR	Count of EOMs for Inactive MID	7.8
3B	INV_SRC_AD	Count of SA not valid 802.6 address	7.8
3C	INV_DST_AD	Count of DA not valid 802.6 address	7.8
3D	INV_SMDS_AD	Count of SA or DA type not SMDS	7.8
3E	DST_SNI	Count of DA In SNI Source Table	8.3
3F	L3_FORMAT	Count of L3 Format Errors	7.8
40	HST_SEG_PTR	Host Segmentation Stack Pointer	6.5.3
41	SEG_STK_PTR	Segmentation Block Stack Pointer	6.5.3
42	ADR_SEG_PTR	Address Screen Segmentation Stack Pointer	6.5.3
43	RSM_STRT	Reassembly-start Stack Pointer	7.2
44	HST_RSM_PTR	Host Reassembly Stack Pointer	7.2
45	RSM_QUIT	Reassembly-quit Stack Pointer	7.2
46	ADR_RSM_PTR	Address Screen Reassembly Stack Pointer	7.2

TABLE 4.

SMDS CONTROL AND REASSEMBLY FORMATTER

RX_CHECK VALUES - TEST MODES

Buffer Start	Buffer End	Buffer Size	Number of L2 PDUs	Register Value	Number of PLCP Slots	Register Value
16K	32K	16K	618	026A	574	023E
24K	32K	8K	308	0134	286	011E
16K	64K	48K	1854	073E	1724	06BC
24K	64K	40K	1544	0608	1436	059C
32K	64K	32K	1236	04D4	1148	047C
16K	128K	112K	4326	10E6	4024	0FB8
24K	128K	104K	4018	0FB2	3736	0E98
32K	128K	96K	3708	0E7C	3448	0D78
64K	128K	64K	2472	09A8	2298	08FA
96K	128K	32K	1236	04D4	1148	047C
16K	256K	240K	9272	2438	8622	21AE
24K	256K	232K	8964	2304	8334	208E
32K	256K	224K	8654	21CE	8048	1F70
64K	256K	192K	7418	1CFA	6898	1AF2
96K	256K	160K	6182	1826	5748	1674
128K	256K	128K	4946	1352	4598	11F6
160K	256K	96K	3708	0E7C	3448	0D78
192K	256K	64K	2472	09A8	2298	08FA

TABLE 5.

SMDS CONTROL AND REASSEMBLY FORMATTER

RSM_BUF_END VALUES

Buffer Start	Buffer End	Buffer Size	Number of Segments	Register Value	Number of L2 PDUs	Register Value
16K	32K	16K	682	1FFB	630	1FFE
24K	32K	8K	341	1FFD	315	1FFF
16K	64K	48K	2048	3FFF	1890	3FFC
24K	64K	40K	1706	3FFB	1575	3FFD
32K	64K	32K	1365	3FFD	1260	3FFD
16K	128K	112K	4778	7FFB	4411	7FFF
24K	128K	104K	4437	7FFD	4096	7FFF
32K	128K	96K	4096	7FFF	3780	7FF9
64K	128K	64K	2730	7FFB	2520	7FFB
96K	128K	32K	1365	7FFD	1260	7FFD
16K	256K	240K	10240	FFFF	9452	FFFD
24K	256K	232K	9898	FFFB	9137	FFFE
32K	256K	224K	9557	FFFD	8822	FFFE
64K	256K	192K	8192	FFFF	7561	FFFA
96K	256K	160K	6826	FFFB	6301	FFFC
128K	256K	128K	5461	FFFD	5041	FFFE
160K	256K	96K	4096	FFFF	3780	FFF9
192K	256K	64K	2730	FFFB	2520	FFFB

TABLE 6.

SMDS CONTROL AND REASSEMBLY FORMATTER

PIN FUNCTIONS

Pin #	Function	Pin Name	Description
1	Ground		Ground
2-3	Bidirect	RD11-RD10	RAM Data
4-8	Output	RA17-RA13	RAM Address
9	Bidirect	~RSEL1	RAM Select
10	Power		Supply Voltage
11	Ground		Ground
12-13	Bidirect	RD9-RD8	RAM Data
14-18	Output	RA12-RA8	RAM Address
19	Bidirect	~RWR	Write Control
20	Ground		Ground
21	Power		Supply Voltage
22			(no-connect)
23-26	Bidirect	RD7-RD4	RAM Data
27-29	Output	RA7-RA5	RAM Address
30	Power		Supply Voltage
31	Ground		Ground
32	Bidirect	~RSEL0	RAM Select
33-37	Output	RA4-RA0	RAM Address
38-39	Bidirect	RD3-RD2	RAM Data
40	Power		Supply Voltage
41	Ground		Ground
42-43	Bidirect	RD1-RD0	RAM Data
44	Bidirect	RPARD	RAM Odd Parity
45-46			(no-connect)
47	Input	RXCKI	PLCP Receive Input Clock
48	Input	RXSYI	PLCP Receive Input Sync
49	Input	RXDATI	PLCP Receive Input Data
50	Power		Supply Voltage
51	Ground		Ground

52	Input	TXCKI	PLCP Transmit Input Clock
53	Input	TXSYI	PLCP Transmit Input Sync
54	Output	TXDATO	Transmit Data
55	Output	PLCPSYO	PLCPSYO
56	Output	PLCP_OOF	PLCP Out of Frame
57	Input	SIG_FRZ	Signaling Freeze
58	Output	SLOTSYO	PLCP Slot Sync Output
59			(no-connect)
60	Ground		Ground
61	Power		Supply Voltage
62	Input	SYSCKI	System Clock
63	Input	8KCKI	8-kHz Reference
64	Output	ONESECO	One-second Out
65	Input	ONESECI	One-second In
66	Input	MUXPRIN	Mux Priority In
67	Output	MUXPROUT	Mux Priority Out
68	Input	TEST0	Test Input
69	Input	~READY	~READY In
70	Power		Supply Voltage
71	Ground		Ground
72-79	Bidirect	AD0-AD7	µP Address/Data
80	Power		Supply Voltage
81	Ground		Ground
82-89	Bidirect	AD8-AD15	µP Address/Data
90	Input	MUX	Multiplex Select
91	Input	PROC	Processor Select
92	Input	PRCLK	Processor Clock
93	Input	RDWR	Read/Write Control
94	Input	ASTR	Address Strobe
95	Input	DSTR	Data Strobe
96	Input	CS	Chip Select
97	Output/OD	~READY	Ready Control
98	Output/OD	STK_INT	Stack Interrupt
99	Output/OD	STAT_INT	Status Interrupt

100	Power		Supply Voltage
101	Ground		Ground
102-119	Input	A18-A0	µP Address Bus
120	Power		Supply Voltage
121	Ground		Ground
122-123			(no-connect)
124-130	Output	HST_OUT6-HST_OUT0	Host Interface Output
131-135	Input	HST_IN4-HST_IN0	Host Interface Input
136-139	Bidirect	HST_DAT15-HST_DAT12	Host Interface Data
140	Power		Supply Voltage
141	Ground		Ground
142-149	Bidirect	HST_DAT11-HST_DAT4	Host Interface Data
150	Power		Supply Voltage
151	Ground		Ground
152-155	Bidirect	HST_DAT3-HST_DAT0	Host Interface Data
156-159	Bidirect	RD15-RD12	RAM Data
160	Power		Supply Voltage

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