LG Semicon Co.,Ltd.

GM76FV8256/ GM76FU8256/ GM76FS8256
GM76FR8256

262,144WORDS x 8 BIT
CMOS STATIC RAM

Description

The GM76FV8256/ GM76FU8256/ GM76FS8256/ GM76FR8256 is a 2,097,152 bits static random access memory organized as 262,144 words by 8 bits. It uses an advanced Full CMOS process technology and high speed and low power circuit technology. Thus it is suitable for high speed and low power applications, especially where battery back-up is required.

Features

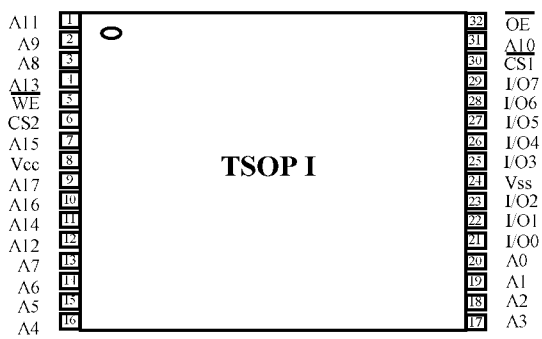
- Power Supply Voltage
  GM76FV8256 Family : 3.0 ~ 3.6V
  GM76FU8256 Family : 2.7 ~ 3.3V
  GM76FS8256 Family : 2.2 ~ 2.7V
  GM76FR8256 Family : 1.8 ~ 2.2V
- Completely Static RAM : No Clock or Timing Strobe Required
- TTL compatible inputs and outputs
- Capability of Battery Back-up Operation
- Package : 32-TSOP-I, 32-sTSOP-I

Product Family

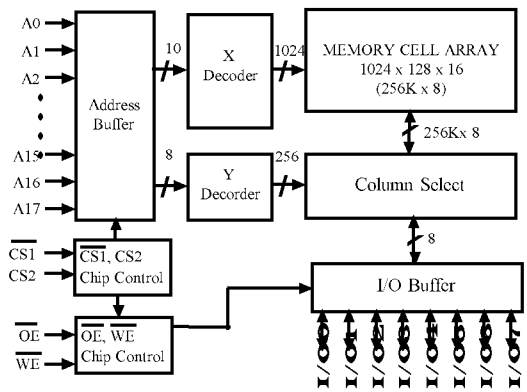
Product Family	Operating Temp. Range	Voltage Range	Speed	Standby Current Iccs2(LL/SL)	Operating Current(Icc1)
GM76FV8256LL/SL	Commercial (0 ~ 70℃)	3.0 ~ 3.6V	*55/70/85ns	10/2 uA	70mA
GM76FU8256LL/SL		2.7 ~ 3.3V	*55/70/85ns		65mA
GM76FS8256LL/SL		2.2 ~ 2.7V	*85/100ns		40mA
GM76FR8256LL/SL		1.8 ~ 2.2V	*100/120ns		30mA
GM76FV8256LLI/SLI	Industrial (-40 ~ 85℃)	3.0 ~ 3.6V	*55/70/85ns	10/2 uA	70mA
GM76FU8256LLI/SLI		2.7 ~ 3.3V	*55/70/85ns		65mA
GM76FS8256LLI/SLI		2.2 ~ 2.7V	*85/100ns		40mA
GM76FR8256LLI/SLI		1.8 ~ 2.2V	*100/120ns		30mA

* The parameter is measured with 30pF test load.

Pin Configuration



Block Diagram



Pin Description

Pin	Function	Pin	Function
A0-A17	Address Inputs	I/O0-I/O7	Data Inputs/Outputs
$\overline{WE}$	Write Enable Input	V_{CC}	Power Supply
$\overline{CS1}$, CS2	Chip Select Input	V_{SS}	Ground
$\overline{OE}$	Output Enable Input		

Absolute Maximum Ratings*

Symbol	Parameter		Rating	Unit
T_A	Ambient Temperature under Bias	GM76FV8256 GM76FU8256 GM76FS8256 GM76FR8256	0 ~ 70	℃
		GM76FV8256-I GM76FU8256-I GM76FS8256-I GM76FR8256-I	-40 ~ 85	
T_{STG}	Storage Temperature		-55 ~ 150	℃
T_{SOL}	Soldering Temperature and Time		260, 10 (at lead)	℃, S
V_{CC}	Supply Voltage		-0.2 ~ 4.0**	V
V_{IN}	Input Voltage		-0.2 ~ V_{CC} + 0.5	V
$V_{I/O}$	Input and Output Voltage		-0.2 ~ V_{CC} + 0.5	V
P_D	Power Dissipation		1	W

*: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** : Maximum Vcc = -0.2 to 4.6V for GM76FV8256 Family and GM76FU8256 Family

Recommended DC Operating Conditions*

Symbol	Parameter	Product	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	GM76FV8256 Family GM76FU8256 Family GM76FS8256 Family GM76FR8256 Family	3.0 2.7 2.2 1.8	3.3 3.0 2.5 2.0	3.6 3.3 2.7 2.2	V
V_{IH}	Input High Voltage	GM76FV8256 Family GM76FU8256 Family GM76FS8256 Family GM76FR8256 Family	2.2 2.2 2.0 1.6	-	Vcc+ 0.2	V
V_{IL}	Input Low Voltage	All Product	-0.2**	-	0.4	V

* 1) Commercial Product : Ta = 0 ~ 70℃, unless otherwise specified
2) Industrial Product : Ta = -40 ~ 85 ℃, unless otherwise specified

** V_{IL}(min) = -1.5V for ≤ 30ns pulse

Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A0 to A17	DATA I/O	MODE
L	H	L	H	Stable	Output Data	Read
L	H	X	L	Stable	Input Data	Write
L	H	H	H	Stable	Hi-Z	Output Disable
H	X	X	X	-	Hi-Z	Standby
X	L	X	X	-	Hi-Z	

*Note: X means don't care

Capacitance (f = 1MHz, T_A = 25℃)

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_I = 0V	-	8	pF
$C_{I/O}$	Output Capacitance	V_O = 0V	-	10	pF

*Note: This parameter is sampled and not 100% tested.

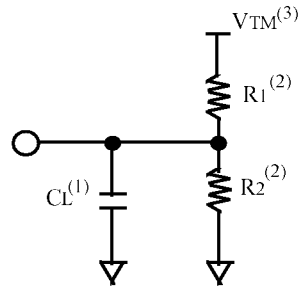
DC Operating Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{I(L)}$	Input Leakage Current	V_{IN} = 0 to V_{CC}		-1	-	1	uA
$I_{O(L)}$	Output Leakage Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} $\overline{OE}$ = V_{IH}, $V_{SS} \le V_{OUT} \le V_{CC}$		-1	-	1	uA
V_{OH}	High Level Output Voltage	I_{OH} = -1.0mA at Vcc=3.0/3.3V I_{OH} = -0.5mA at Vcc=2.5V I_{OH} = -0.44mA at Vcc=2.0V		2.2 2.0 1.6	-	-	V
V_{OL}	Low Level Output Voltage	I_{OL}= 2.1mA at Vcc=3.0/3.3V I_{OL} = 0.5mA at Vcc=2.5V I_{OL} = 0.33mA at Vcc=2.0V		-	-	0.4	V
I_{CC}	Operating Supply Current	$\overline{CS1}$ = V_{IL} and CS2 = V_{IH}, V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0mA		-	-	10	mA
I_{CC1}	Average Operating Current	$\overline{CS1}$ = V_{IL} and CS2 = V_{IH} V_{IN} = V_{IH}/V_{IL} , I_{OUT} = 0mA tcycle = Min, cycle	Vcc=3.3V@55ns	-	-	70	mA
			Vcc=3.0V@55ns	-	-	65	
			Vcc=2.5V@85ns	-	-	40	
			Vcc=2.0V@100ns	-	-	30	
I_{CC2}		$\overline{CS1}$ = 0.2V, CS2 = V_{CC}-0.2V V_{IN} = V_{CC} - 0.2V/0.2V I_{OUT} = 0mA, tcycle = 1us		-	-	10	mA
I_{CCS1}	Standby Current(TTL)	$\overline{CS1}$ = V_{IH}, CS2 = V_{IL}		-	-	0.3	mA
I_{CCS2}	Standby Current(CMOS)	$\overline{CS1}$ = V_{CC}-0.2V,CS2 = 0.2V	SL	-	-	2	uA
			LL	-	-	10	

AC Operating Characteristics

Test Conditions

Parameter	Value			
	Vcc	3.0,3.3V	2.5V	2.0V
Input Pulse Level	0.4 to 2.2V			0.4 to 1.8V
Input Rise and Fall Time	5ns			
Input and Output Timing Reference Levels	1.5V		1.1V	0.9V
Output Load	C_L = 30pF(100 pF) + 1 TTL Load			



(1) Incuding Scope and Jig Capacitance
(2) R_1 = 3070Ω , R_2 = 3150 Ω
(3) VTM = 2.8V for Vcc = 3.0/3.3V
= 2.3V for Vcc = 2.5V
= 1.8V for Vcc = 2.0V

AC Operating Characteristics

Read Cycle

(Commercial Product :Ta = 0 ~ 70℃, Industrial Product : Ta = -40 ~ 85℃)

Symbol	Parameter	55ns		70ns		85ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	55	-	70	-	85	-	ns
t_{AA}	Address Access Time	-	55	-	70	-	85	ns
t_{ACS1}	Chip Select 1 Access Time	-	55	-	70	-	85	ns
t_{ACS2}	Chip Select 2 Access Time	-	55	-	70	-	85	ns
t_{OE}	Output Enable Access Time	-	30	-	35	-	45	ns
t_{CLZ1}	Chip Select 1 Output Setup Time	5	-	5	-	10	-	ns
t_{CHZ1}	Chip Select 1 Output Floating	0	20	0	25	0	30	ns
t_{CLZ2}	Chip Select 2 Output Setup Time	5	-	5	-	10	-	ns
t_{CHZ2}	Chip Select 2 Output Floating	0	20	0	25	0	30	ns
t_{OLZ}	Output Enable Output Setup Time	5	-	5	-	5	-	ns
t_{OHZ}	Output Enable Output Floating	0	20	0	25	0	30	ns
t_{OH}	Output Hold Time	5	-	10	-	10	-	ns

Write Cycle

Symbol	Parameter	55ns		70ns		85ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	55	-	70	-	85	-	ns
t_{CW1}	Chip Select Time 1	50	-	65	-	75	-	ns
t_{CW2}	Chip Select Time 2	50	-	65	-	75	-	ns
t_{AW}	Address Enable Time	50	-	60	-	70	-	ns
t_{AS}	Address Setup Time	0	-	0	-	0	-	ns
t_{WP}	Write Pulse Width	45	-	50	-	60	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{DW}	Input Data Setup Time	25	-	30	-	35	-	ns
t_{DH}	Input Data Hold Time	0	-	0	-	0	-	ns
t_{WHZ}	Write to Output in High-Z	0	20	0	25	0	30	ns
t_{OW}	Output Active from End of Write	5	-	5	-	5	-	ns

AC Operating Characteristics

Read Cycle

(Commercial Product :Ta = 0 ~ 70℃, Industrial Product : Ta = -40 ~ 85℃)

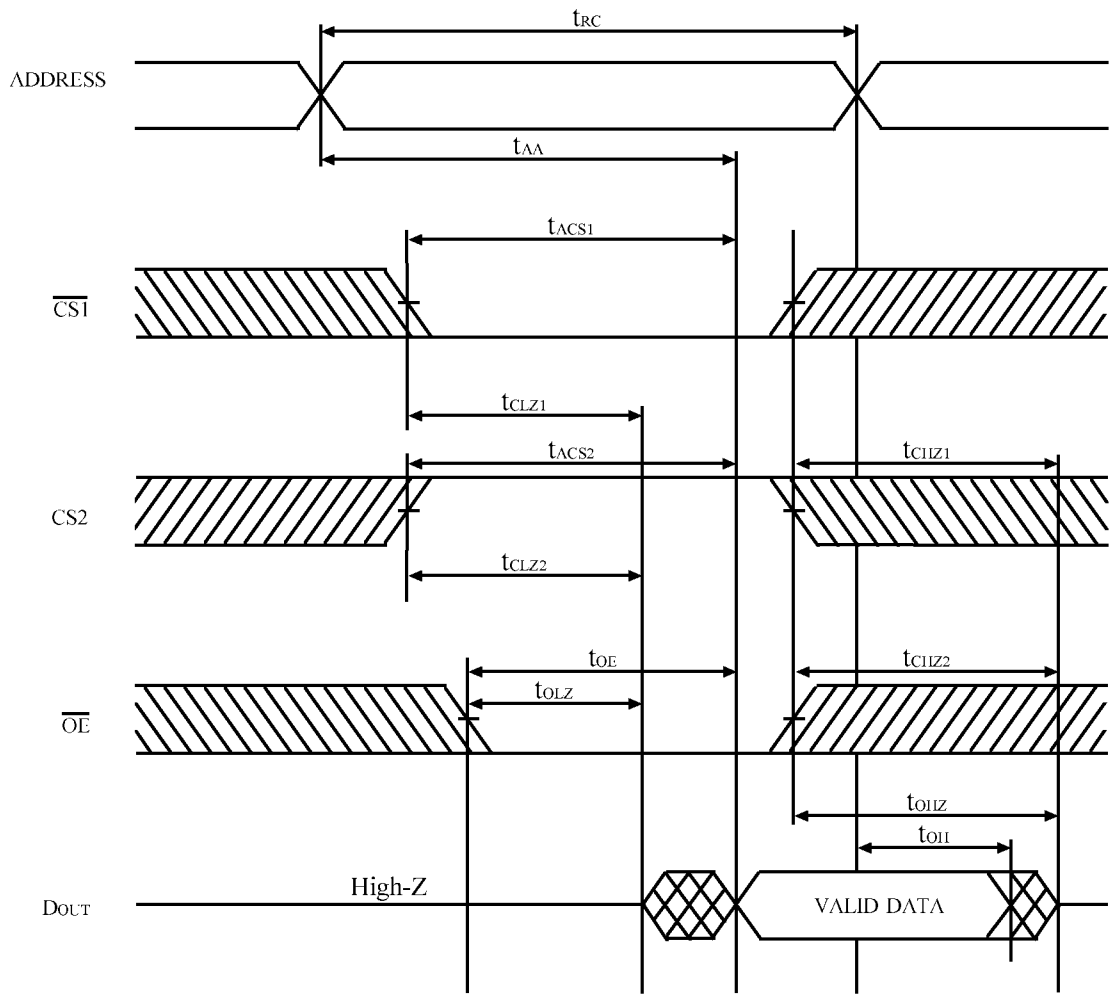
Symbol	Parameter	100ns		120ns		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100	-	120	-	ns
t_{AA}	Address Access Time	-	100	-	120	ns
t_{ACS1}	Chip Select 1 Access Time	-	100	-	120	ns
t_{ACS2}	Chip Select 2 Access Time	-	100	-	120	ns
t_{OE}	Output Enable Access Time	-	50	-	60	ns
t_{CLZ1}	Chip Select 1 Output Setup Time	10	-	20	-	ns
t_{CHZ1}	Chip Select 1 Output Floating	0	35	0	35	ns
t_{CLZ2}	Chip Select 2 Output Setup Time	10	-	10	-	ns
t_{CHZ2}	Chip Select 2 Output Floating	0	35	0	35	ns
t_{OLZ}	Output Enable Output Setup Time	5	-	5	-	ns
t_{OHZ}	Output Enable Output Floating	0	35	0	35	ns
t_{OH}	Output Hold Time	10	-	15	-	ns

Write Cycle

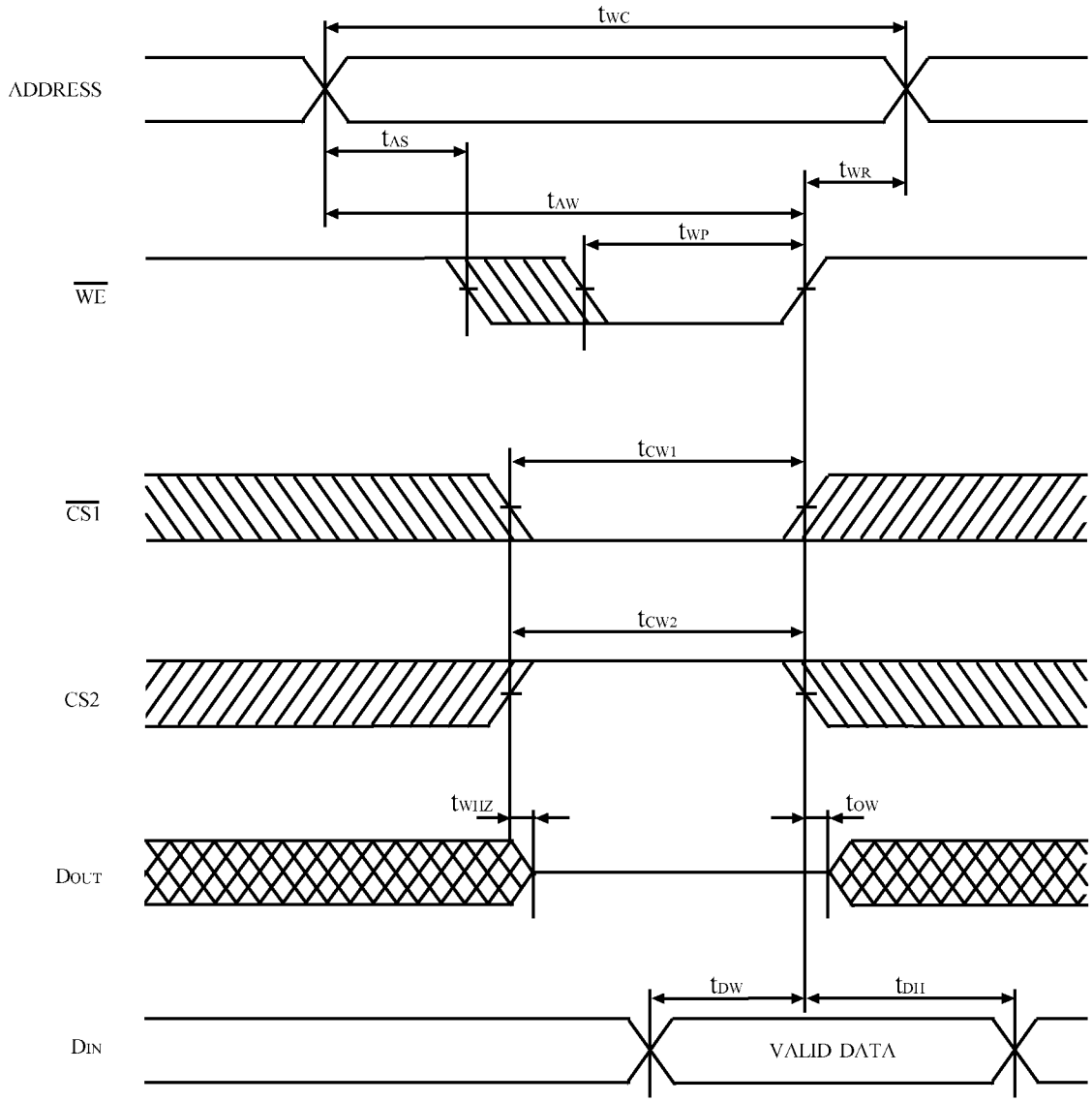
Symbol	Parameter	100ns		120ns		Unit
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	100	-	120	-	ns
t_{CW1}	Chip Select Time 1	85	-	100	-	ns
t_{CW2}	Chip Select Time 2	85	-	100	-	ns
t_{AW}	Address Enable Time	80	-	90	-	ns
t_{AS}	Address Setup Time	0	-	0	-	ns
t_{WP}	Write Pulse Width	70	-	80	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{DW}	Input Data Setup Time	40	-	50	-	ns
t_{DH}	Input Data Hold Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High-Z	0	40	0	40	ns
t_{OW}	Output Active from End of Write	10	-	10	-	ns

Timing Waveforms

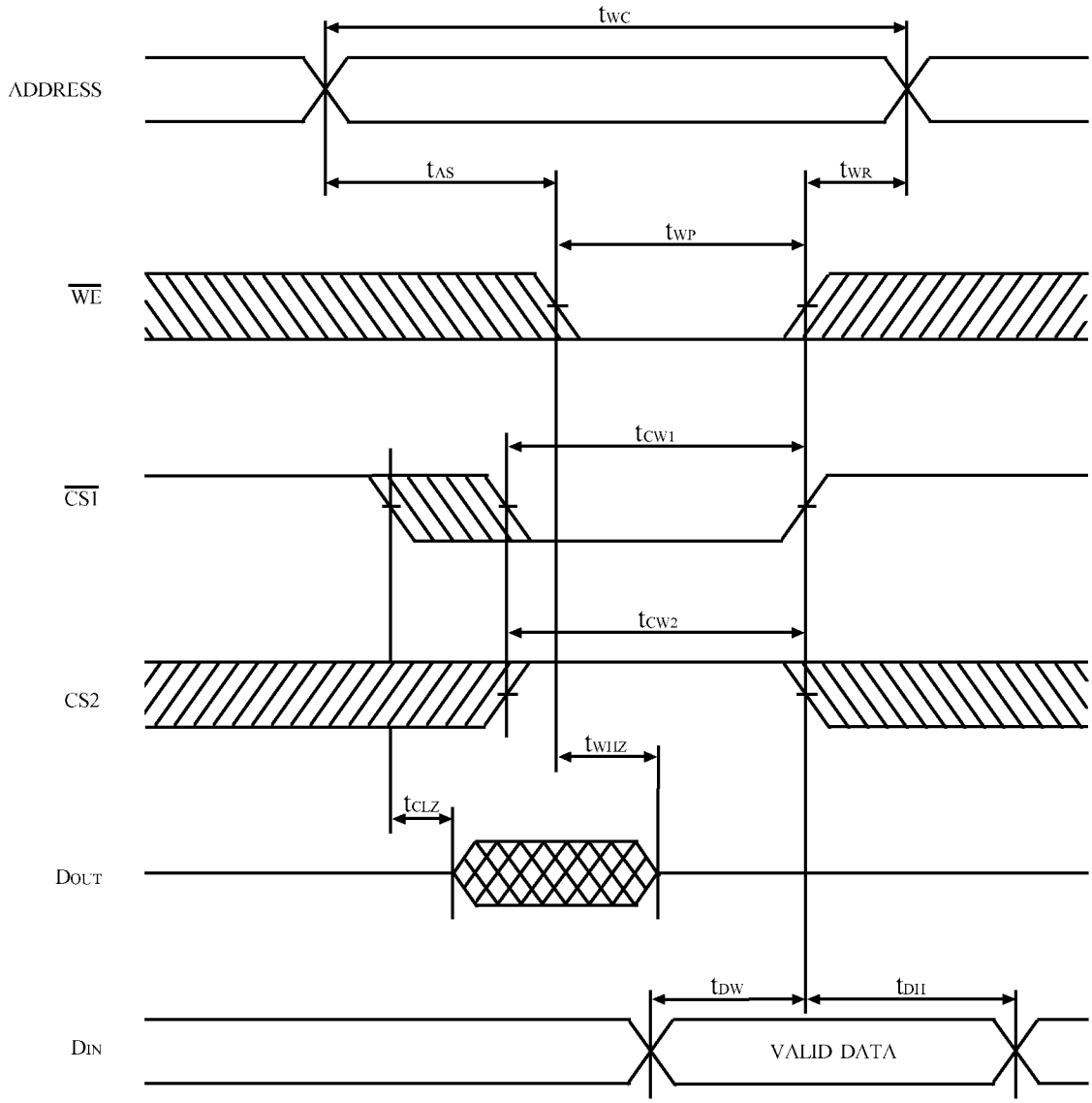
Read Cycle (Note 1)



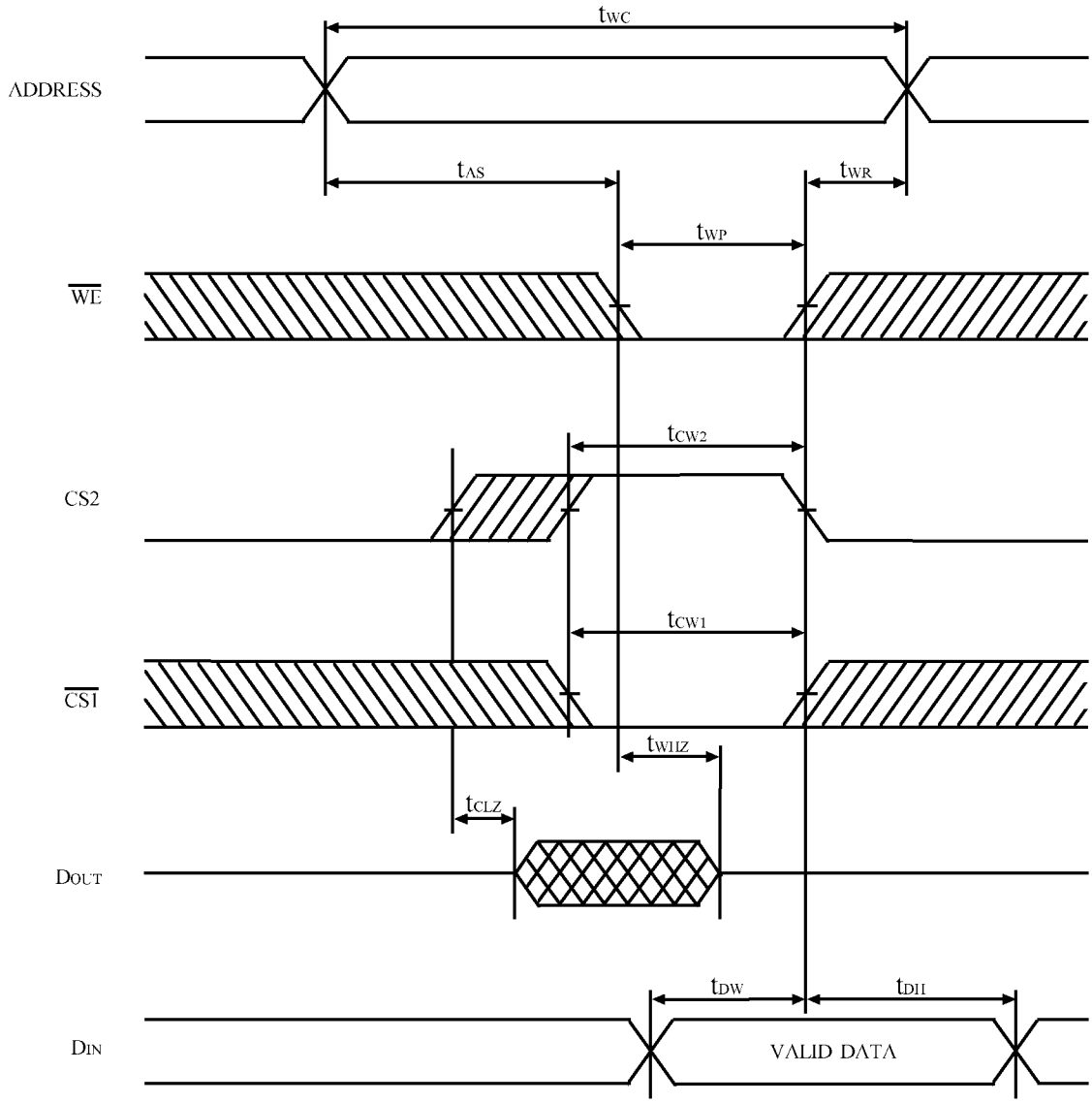
Write Cycle (1) ($\overline{WE}$ Controlled) (Notes 2, 3, 4)



Write Cycle (2) ($\overline{CS1}$ Controlled) (Notes 4)



Write Cycle (3) (CS2 Controlled) (Notes 4)



Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition. Outputs remain in a high impedance state.
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition. Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is high for write cycle. Outputs are in a high impedance state during this period.

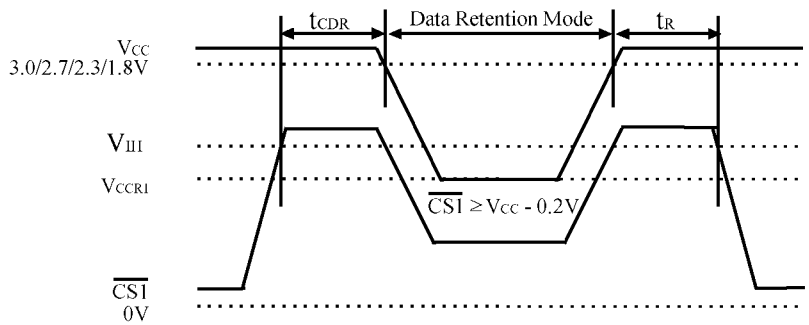
Data Retention Characteristics

Symbol	Parameter			Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage			1.5	-	3.6	V
I_{CCR}	Data Retention Current	VCC=3.0V	SL	-	0.5	2	*u*A
			LL	-	0.5	10	
t_{CDR}	Chip Select to Data Retention Time			0			ns
t_R	Operation Recovery Time			$tRC_{(2)}$			ns

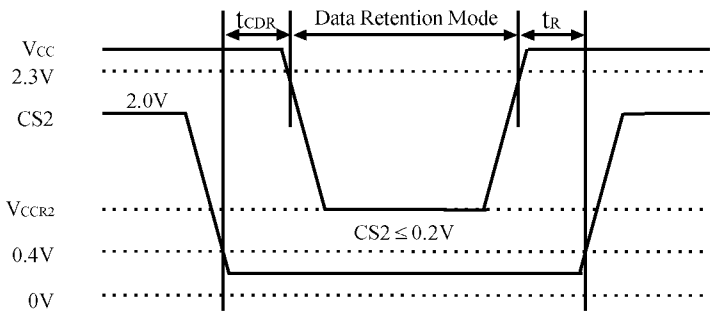
(1) Test Condition
-- Commercial Product : Ta = 0 ~ 70℃
-- Industrial Product : Ta = -40 ~ 85℃

(2) tRC = Read cycle time

• Low V_{CC} Data Retention Mode: (1) $\overline{CS1}$ Controlled



• Low V_{CC} Data Retention Mode: (2) CS2 Controlled

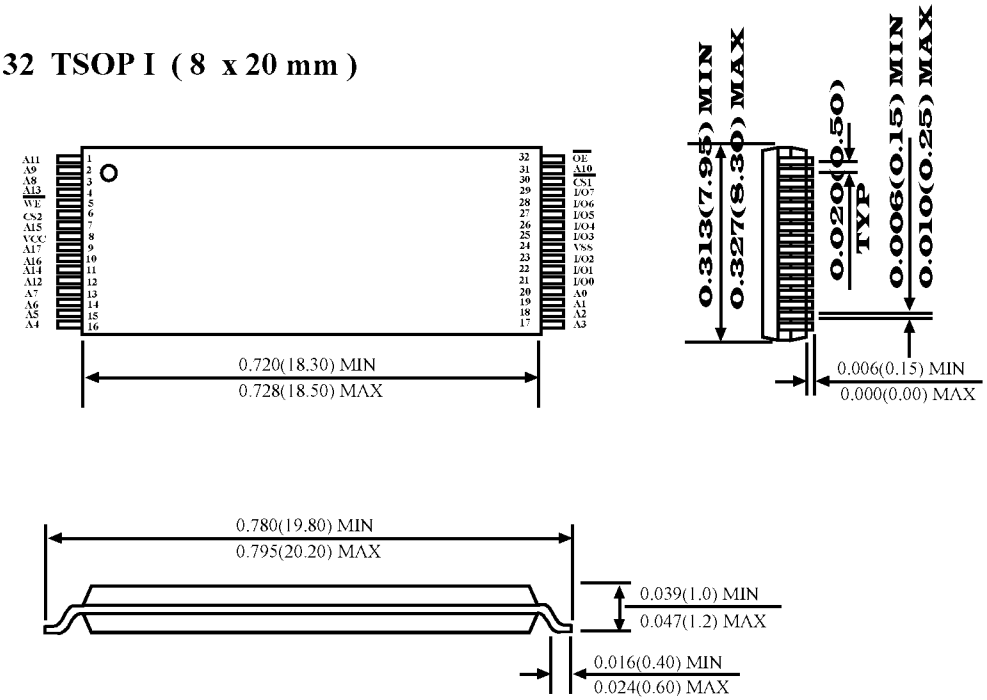


Notes: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and D_{IN} buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2 ≥V_{CC} - 0.2V or CS2≤0.2V. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Package Dimensions

Unit: Inches (mm)

32 TSOP I (8 x 20 mm)



32 Small TSOP I (8 x 13.4 mm)