DESCRIPTION

The HYM5V72A414A is a 4M x 72-bit EDO mode CMOS DRAM module consisting of eighteen HY51V17404B in 24/26 pin SOJ or TSOPII and one 2048 bit EEPROM on a 168 pin glass-epoxy printed circuit board. 0.1μF and 0.01μF decoupling are mounted for each DRAM. The HYM5V72A414AKG/ATKG/ASLKG/ASLTKG is Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 32M byte memory.

FEATURES

- Low power dissipation
  Max. self-refresh 19.4mW (SL-part)
  Max. battery back-up 32.4mW (SL-part)
  Max. CMOS standby 25.9mW (SL-part)
  64.8mW
  Max. TTL standby 64.8mW
  Max. operating

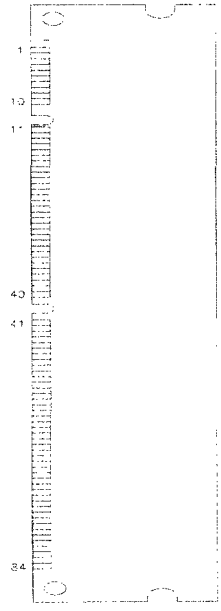
Speed	Power
60	7.78W
70	6.48W
80	5.83W

- Single power supply of 3.3V ± 10%
- TTL compatible inputs and outputs
- Fast access time

Speed	tRAC	tCAC	tHPC
60	60ns	15ns	25ns
70	70ns	18ns	30ns
80	80ns	20ns	35ns

- EDO mode operation
- /CAS-before-/RAS, /RAS-only, Hidden refresh, Self-refresh
- 2048 refresh cycles / 256ms (SL-part)
  2048 refresh cycles / 32ms
- Serial Presence Detect

PIN CONNECTION



PIN CONNECTION

/RAS0-/RAS2	Row Address Strobe
/CAS0-/CAS7	Column Address Strobe
/WE0, /WE2	Write Enable
/OE0, /OE2	Output Enable
A0-A10	Address Input
DQ0-DQ71	Data Input/Output
SLC	Serial PD Clock Input
SDA	Serial PD Data Input/Output
SA0-SA2	Serial PD Device Add. Input
VCC	Power (+3.3V)
VSS	Ground

PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	/OE2	86	DQ36	128	NC
3	DQ1	45	/RAS2	87	DQ37	129	NC
4	DQ2	46	/CAS2	88	DQ38	130	/CAS6
5	DQ3	47	/CAS3	89	DQ39	131	/CAS7
6	Vcc	48	/WE2	90	Vcc	132	NC
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	Vss	106	DQ53	148	Vss
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE0	69	DQ28	111	NC	153	DQ64
28	/CAS0	70	DQ29	112	/CAS4	154	DQ65
29	/CAS1	71	DQ30	113	/CAS5	155	DQ66
30	/RAS0	72	DQ31	114	/RAS1	156	DQ67
31	/OE0	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
32	A2	76	DQ34	118	A3	160	DQ70
34	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	NC	167	SA2
42	NC	84	Vcc	126	NC	168	Vcc

SERIAL PD BYTE DEFINITION

BYTENUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE
Byte 0	Number of Byte written during module production	15 Bytes	0Fh
Byte 1	Total Byte of Serial Presence Detect Device	256 Bytes	08h
Byte 2	Memory Type	EDO	02h
Byte 3	Number of ROW Addresses	11	0Bh
Byte 4	Number of COLUMN Address	11	0Bh
Byte 5	Number of Banks	1 Bank	01h
Byte 6	Module Data Width	72bit	48h
Byte 7	Module Data Width (Continued)	Not Used	00h
Byte 8	Module Interface Levels	LVTTL	01h
Byte 9	t_{RAC}	60ns 70ns 80ns	3ch 46h 50h
Byte 10	t_{CAC}	15ns 18ns 20ns	0Fh 12h 14h
Byte 11	Module Configuration Type	ECC	02h
Byte 12	Refresh Rate/Type	Normal (15.6 μs) SL-Part (125 μs)	00h 85h
Byte 13	Primary DRAM width	x4	04h
Byte 14	Error Checking DRAM width	x4	04h
Byte 15-255	Undefined	Undefined	Undefined

NOTE :

1. Serial PD interface is standard IIC architecture.
2. Pull-up resistors (4.7K typical value) are required on all open collector bus devices (SCL and SDA).
3. Current sink capability on SCL and SDA (I_{OL} max) must be at least 3ma to maintain a valid low level.

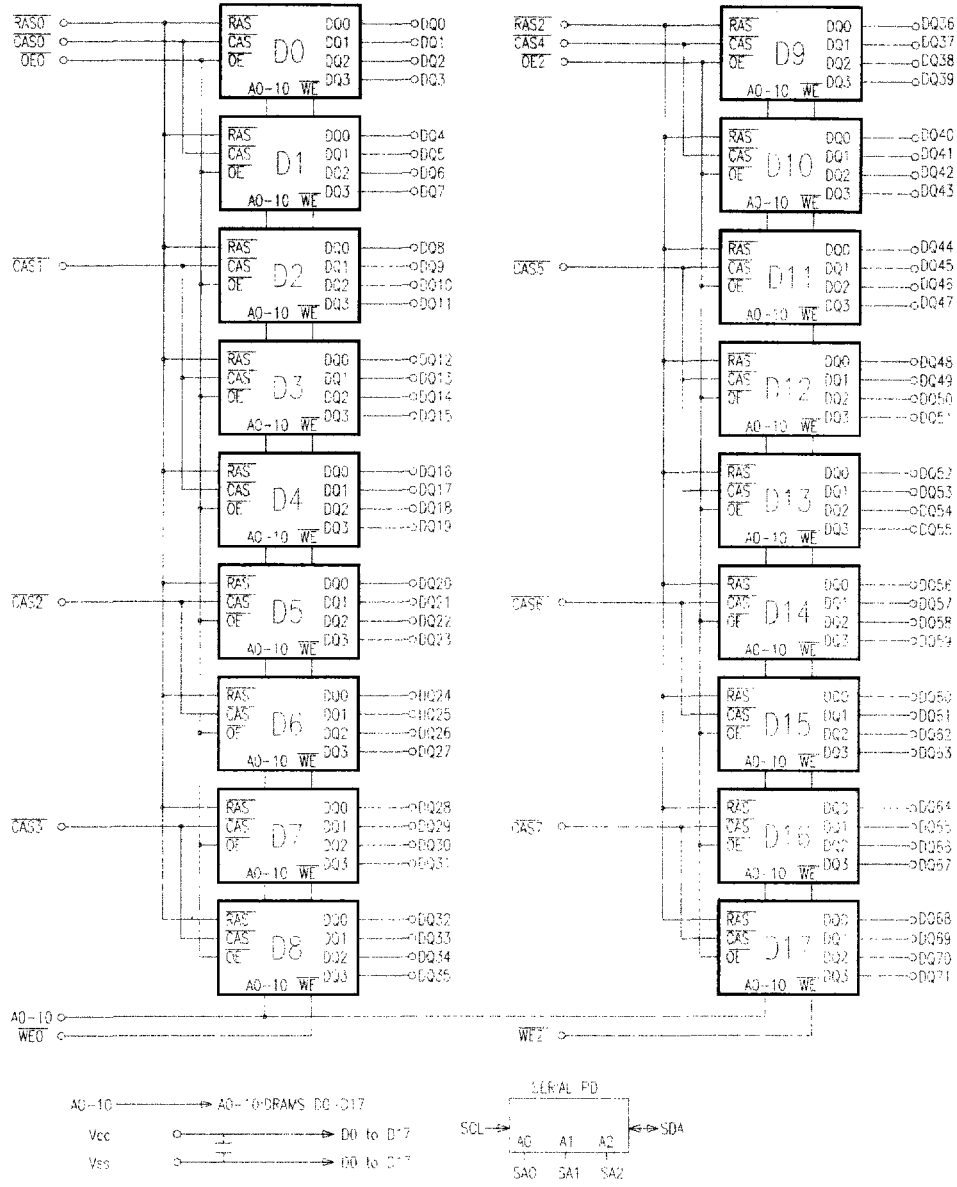
IIC BUS INTERFACE

SYMBOL	RATING	NOTE
C_{MAX}	400pF	1
f_{MAX}	80 KHz (3.3V) 100 KHz (5.0V)	2
$I_{OL\ MAX}$	3mA	

NOTE :

1. The maximum number of devices connected on the IIC bus is controlled by the maximum allowable capacitance which is 400_{pF} per line.
2. The maximum IIC system clock frequency depends on V_{CC}.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	-1.0 to 4.6	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	20	mA
P_D	Power Dissipation	18	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(TA=0°C to 70°C, V_{CC}=3.3V ±10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}$+1.0, All other pins not under test=V_{SS}		-180	180	µA	
I_{LO}	Output Leakage Current (High impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$ /RAS & /CAS at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current Operating	t_{RC}=t_{RC} (min.)	60	-	2160	mA	1,2,3
			70	-	1800		
			80	-	1620		
I_{CC2}	V_{CC} Supply Current TTL Standby	/RAS & /CAS at V_{IH}, other inputs ≥ V_{SS}		-	36	mA	
I_{CC3}	V_{CC} Supply Current /RAS-only refresh	t_{RC}=t_{RC}(min.)	60	-	2160	mA	1,3
			70	-	1800		
			80	-	1620		
I_{CC4}	V_{CC} Supply Current, EDO mode	t_{HPC}= t_{HPC} (min.)	60	-	2160	mA	1,2,3
			70	-	1800		
			80	-	1620		
I_{CC5}	V_{CC} Supply Current CMOS Standby	/RAS & /CAS ≥ V_{CC} – 0.2V		-	18	mA	
			SL-part	-	7.2		5
I_{CC6}	V_{CC} Supply Current /CAS before /RAS refresh	t_{RC}=t_{RC}(min.)	60	-	2160	mA	1,3
			70	-	1800		
			80	-	1620		
I_{CC7}	V_{CC} Supply Current, Battery Back Up (SL-part only)	t_{RC}= 125µs, /CAS = CBR cycling or 0.2V, /WE = V_{CC} – 0.2V A0 - A10 = V_{CC} – 0.2V or 0.2V DQ0-DQ71=V_{CC}-0.2V, 0.2V or open	$t_{RAS} \le$ 300ns	-	6.3	mA	1,4,5
			$t_{RAS} \le$ 1 µs	-	10.8		
I_{CC8}	V_{CC} Supply Current Self Refresh (SL-part only)	/RAS & /CAS= V_{IL} /OE & /WE & A0-A10= V_{CC}-0.2V or 0.2V DQ0-DQ71= V_{CC}-0.2V, 0.2V or open		-	5.4	mA	5
V_{OL}	Output Low Voltage	I_{OL}= 2.0mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= 2.0mA		2.4	-	V	

NOTE

1. I_{CC1}, I_{CC3}, I_{CC4},I_{CC6} and I_{CC7} depend on cycle rate.
2. output loading. Specified values are obtained with the ouptup open.
3. I_{CC} is specified as average current. For I_{CC1},I_{CC3} and I_{CC6} address can be changed maximum two times while /RAS=V_{IL}. For I_{CC4}, address can be changed maximum once while /CAS=V_{IH}.
4. Only t_{RAS}(max.)=1µs is applied to refresh of battery backup but t_{RAS}(max.)=10µs is applied to normal functional operation.
5. I_{CC5}(max.)=7.2mA, I_{CC7} and I_{CC8} are applied to SL-part only (HYM5V72A414ASLKG/ASLTKG).

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc= 3.3V ±10%, Vss= 0V, unless otherwise noted.) NOTE : 1,2,3

#	SYMBOL	PARAMTER	HYM5V72A414A K-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	/RAS to /CAS Precharge Time	155	-	180	-	200	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	Time from /CAS Precharge	75	-	85	-	95	-	ns	
5	tRAC	Access Time from /RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from /CAS	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Coulmn Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from /CAS Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	/CAS to Output Low Impedance	3	-	3	-	3	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	3	15	3	18	3	20	ns	5
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	/RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	/RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	/RAS Pulse Width (EDO Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	/RAS Hold Time	15	-	18	-	20	-	ns	
16	tCSH	/CAS Hold Time	45	-	50	-	55	-	ns	
17	tCAS	/RAS Pulse Width	11	10K	14	10K	17	10K	ns	
18	tRCD	/RAS to /CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	/RAS to Column Address Delay Time	15	30	15	35	17	40	ns	10
20	tCRP	/CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	/CAS Precharge Time	10	-	12	-	14	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	12	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	15	-	ns	
26	tAR	Column Address Hold Time from /RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to /RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	
32	tWCR	Write Command Hold Time from /RAS	50	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	
34	tRWL	Write Command to /RAS Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to /CAS Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	tDHR	Data-In Hold Time Referenced to /RAS	50	-	50	-	55	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

#	SYMBOL	PARAMTER	HYM5V72A414A K-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	/CAS to /WE Delay Time	40	-	45	-	50	-	ns	8
42	tRWD	/RAS to /WE Delay Time	80	-	92	-	105	-	ns	8
43	tAWD	Column Address to /WE Delay Time	50	-	60	-	60	-	ns	8
44	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	/RAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	/RAS Hold Time Reference to /OE	10	-	10	-	10	-	ns	
49	tOEA	/OE Access Time	-	15	-	18	-	20	ns	
50	tOED	/OE to Data Delay	15	-	18	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from /OE	3	15	3	18	3	20	ns	5
52	tOEH	/OE Command Hold Time	15	-	18	-	20	-	ns	
53	tCPWD	/WE Delay Time from /CAS Precharge	55	-	65	-	75	-	ns	8
54	tRHCP	/RAS Hold Time from /CAS Precharge	35	-	40	-	45	-	ns	
55	tWRP	/WE to /RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	/WE to /RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tRASS	/RAS Pulse Width (Slef Refresh Cycle)	100	-	100	-	100	-	ns	
58	tRPS	/RAS Precharge Time (Self Refresh Cycle)	90	-	110	-	130	-	ns	
59	tCHS	/CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
60	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
61	tREZ	Output Buffer Turn-off Delay (/RAS)	3	15	3	18	3	20	ns	5,15
62	tWEZ	Output Buffer Turn-off Delay (/WE)	3	15	3	18	3	20	ns	5
63	tWPE	/WE Pulse Width for Output Disable	5	-	8	-	10	-	ns	
64	tOEP	/OE Pulse Width for Output Disable	5	-	8	-	10	-	ns	
65	tOCH	/OE Low to /CAS High Delay Time	0	-	0	-	0	-	ns	
66	tCHO	/CAS High to /OE High Hold Time	5	-	8	-	10	-	ns	
67	tWED	/WE to Data Delay Time	15	-	18	-	20	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS intilization cycles instead of 8 /RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If /RAS= Vss during power-up, the HYM5V72A414A could begin an active cycle. This conditionn results in higher power-up current than necessary demands from the power-up. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. Refer to the HY51V17404A data sheet for detailed information.
4. Measured with a load equivalent to 1 TTL loads and 100pF.(V_{OH}=2.0V, V_{OL}=0.8V)
5. t_{CEZ}(max.), t_{OEZ}(max.), t_{REZ}(max.) and t_{WEZ}(max.) define the time at which the output achiveds the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in late write or read-modify-write Cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throught the entire cycle
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. Measured with the specified current load and 100pF.
12. A burst of 2048 /CAS-before-/RAS refresh cycles must bwe executed within 32ms after existing self refresh (for SL-part).
13. If $t_{CWD} \geq t_{WCS}$(min.) $t_{RWD} \geq t_{RWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPWD} \geq t_{CPWD}$(min.), the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neighter of the above conditions are met, the condition of the data out (at access time and until /CAS goes back to V_{IH}) is indeterminated.
14. In /CAS before /RAS self refresh mode.

    In case of using distributed /CAS before /RAS refresh, refresh 2048 times during a 256ms after reset

    In case of using burst /CAS before /RAS refresh, refresh 2048 times during a 32ms after reset

    In case of using /RAS only refresh, refresh against all refresh address during a 32ms after rese
15. If /RAS goes to high before /CAS high going, the open circuit condition of the output is achieved by /CAS high going.

    If /CAS goes to high before /RAS high going, the open circuit condition of the output is achieved by /RAS high going.

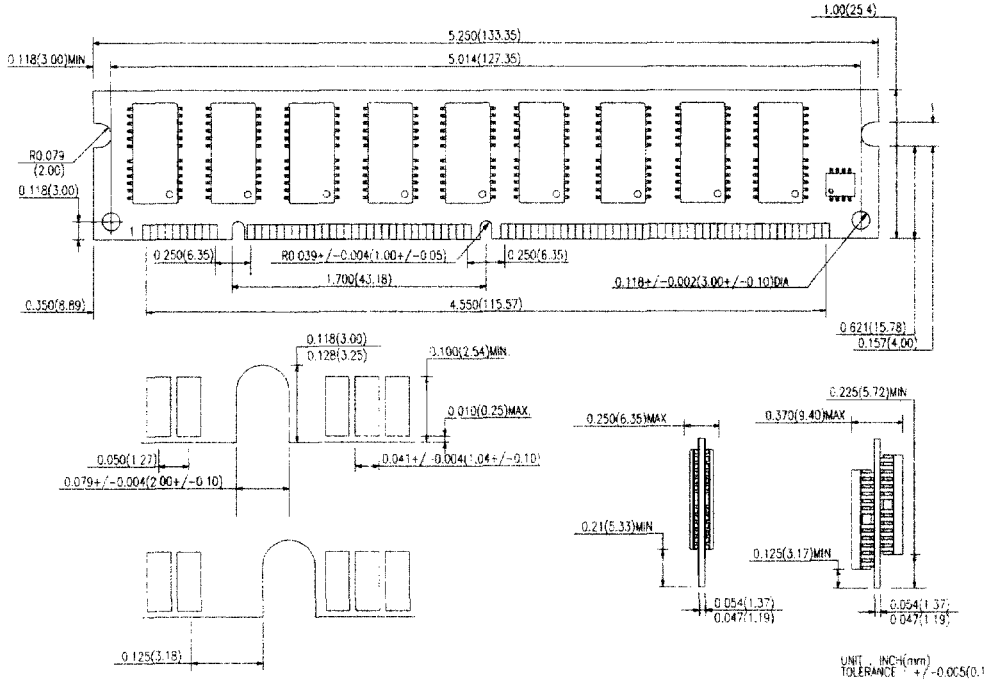
CAPACITANCE

(TA=25°C, Vcc=3.3V± 10%, Vss=0V, f=1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	100	pF
C_{IN2}	Input Capacitance (/WE0, /WE2, /OE0, /OE2)	-	73	pF
C_{IN3}	Input Capacitance (/RAS0-/RAS2)	-	70	pF
C_{IN4}	Input Capacitance (/CAS0-/CAS7)	-	13	pF
C_{DQ}	Data Input/output Capacitance (DQ0-DQ71)	-	15	pF

PACKAGE DIMENSION

168pin Unbuffered Dual Inline Memory Module (KG;Gold plated)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V72A414AKG	60/70/80		DIMM	Gold
HYM5V72A414ASLKG	60/70/80	SL-part	DIMM	Gold
HYM5V72A414ATKG	60/70/80		DIMM	Gold
HYM5V72A414ASLTKG	60/70/80	SL-part	DIMM	Gold