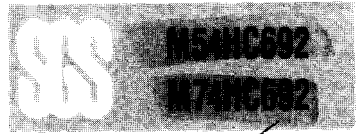


HS-C²MOS™ INTEGRATED CIRCUITS

040749



PRODUCT PREVIEW

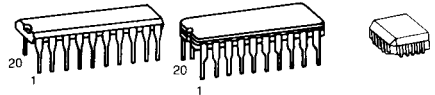
DECADE COUNTER REGISTER (3-STATE)

DESCRIPTION

The M54/74HC692 is a high speed CMOS DECADE COUNTER REGISTER (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device incorporates synchronous counter, four-bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counter can be programmed from the data inputs and have enable P and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three-state outputs, QA, QB, QC, and QD.

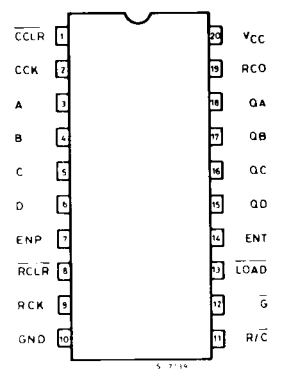
Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered. The clear line is active low and is, synchronous.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



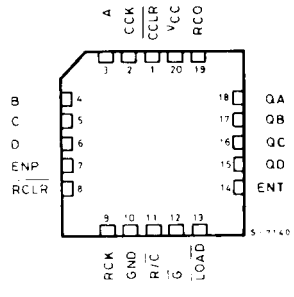
B1 Plastic Package **F1** Ceramic Package **C1** Chip Carrier
ORDERING NUMBERS: M54HC692 F1
M74HC692 B1
M74HC692 F1
M74HC692 C1

PIN CONNECTIONS (top view)



Dual in line

CHIP CARRIER



FEATURES

- Low Power Dissipation
I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity
V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Output Drive Capability
10 LSTTL Loads
- Symmetrical Output Impedance
|I_{OH}| = I_{OL} = 4 mA (Min.)
- Balanced Propagation Delays
t_{PLH} = t_{PHL}
- Wide Operating Voltage Range
V_{CC} (opr) = 2V to 6V
- Pin and Function compatible
with 54/74LS692

M54HC692

M74HC692

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
CCLR	LOAD	ENP	ENT	CCK	RCLR	RCK	R/C	G	QA	QB	QC	QD	
*	*	*	*	*	*	*	*	H	Z	Z	Z	Z	High Impedance
L	*	*	*	\uparrow	*	*	L	L	L	L	L	L	Clear Counter
H	L	*	*	\uparrow	*	*	L	L	a	b	c	d	Load Counter
H	H	L	*	\uparrow	*	*	L	L	No Change			No count	
H	H	*	L	\uparrow	*	*	L	L	No Change			No count	
H	H	H	H	\uparrow	*	*	L	L	Count up			Count up	
*	*	*	*	\downarrow	*	*	L	L	No Change			No count	
*	*	*	*	*	L	\uparrow	H	L	L	L	L	L	Clear Register
*	*	*	*	*	H	\uparrow	H	L	a'	b'	c'	d'	Load Register
*	*	*	*	*	*	\downarrow	H	L	No change			No Load	

* : Don't care

Z : High Impedance

a-d : The level of steady state inputs at inputs A through D respectively.

a'-d' : The level of steady state outputs at internal counter outputs QA' through QD' respectively.

RCO FUNCTION: $RCO = QA.QD.ENT$

INPUT AND OUTPUT EQUIVALENT CIRCUIT

