



Guaranteed Low Skew 3.3V CMOS Clock Driver/Buffer

QS53807
QS532807

FEATURES/BENEFITS

- JEDEC compatible LVTTTL level
- 10 low skew clock outputs
- Clock input is 5V tolerant
- Pinout and function compatible with QS5807
- QS532807 has 25Ω on-chip resistors for low noise
- Input hysteresis for better noise margin
- Guaranteed low skew
 - 0.35ns same transition
 - 0.6ns opposite transition
 - 0.75ns different devices
- Industrial temperature range
- Available in QSOP (Q) and SOIC (SO)

DESCRIPTION

The QS53807 and QS532807 clock driver/buffer circuits can be used for clock buffering schemes where low skew is a key parameter. The QS53806 offers ten non-inverting outputs. Designed in QSI's proprietary QCMOS process, these devices provide low propagation delay buffering with on-chip skew of 0.35ns for same-transition, same-bank signals. The QS532807 has on-chip series termination resistors for lower noise clock signals. The series resistor versions are recommended for driving unterminated lines with capacitive loading and other noise sensitive clock distribution circuits. These clock buffer products are designed for use in high-performance workstations, embedded and personal computing systems. Several devices can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. See Application Note AN-21 for more information on low-skew clock buffers.

Figure 1. Functional Block Diagram

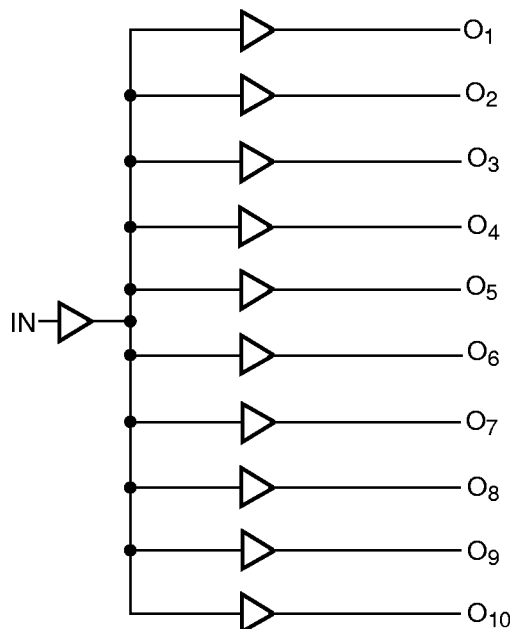


Figure 2. Pin Configurations (All Pins Top View)

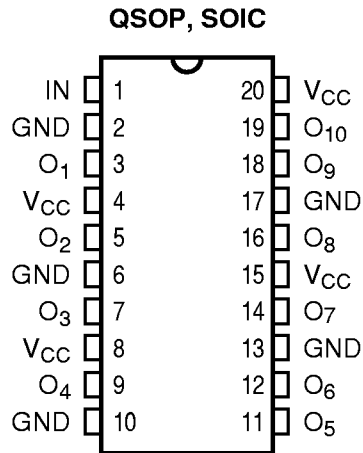


Table 1. Pin Description

Name	I/O	Description
IN	I	Clock Input
O _x	O	Clock Outputs

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to 4.6V
DC Output Voltage V _{OUT}	-0.5V to V _{CC} + 0.5V
DC Input Voltage V _{IN}	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	-3.0V
DC Input Diode Current with V _{IN} < 0	-20mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation At T _A =85°C, QSOP	0.82 watts
SOIC	0.75 watts
T _{STG} Storage Temperature	-65° to 150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

Pins	QSOP		SOIC		Unit
	Typ	Max	Typ	Max	
C _{IN}	3	6	5	7	pF

Note: Capacitance is characterized but not tested.

Table 4. DC Electrical Characteristics Over Operating Range

Industrial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.3 \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Inputs	2.0	1.7	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Inputs	-0.5	—	0.8	
V_{IC}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}^{(3)}$	—	-0.7	-1.2	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -100\mu\text{A}$	$V_{CC}-0.2$	—	—	
		$V_{CC} = \text{Min.}, I_{OH} = -8\text{mA}$	2.4	—	—	
V_{OL}	Output LOW Voltage QS53807	$V_{CC} = \text{Min.}, I_{OL} = 100\mu\text{A}$	—	—	0.2	
		$V_{CC} = \text{Min.}, I_{OL} = 16\text{mA}$	—	—	0.4	
		$V_{CC} = \text{Min.}, I_{OL} = 24\text{mA}$	—	—	0.5	
V_{OL}	Output LOW Voltage QS532807	$V_{CC} = \text{Min.}, I_{OL} = 100\mu\text{A}$	—	—	0.2	
		$V_{CC} = \text{Min.}, I_{OL} = 6\text{mA}$	—	—	0.4	
		$V_{CC} = \text{Min.}, I_{OL} = 8\text{mA}$	—	—	0.5	
$ I_{IN} $	Input Leakage Current	$0 \leq V_{IN} \leq 5.5\text{V}$	—	—	1	μA
I_{OS}	Short Circuit Current ^(2,3)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}$	-60	-195	—	mA
$ I_{ODH} $	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}$	-50	-80	-200	mA
$ I_{ODL} $	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}$	50	112	200	mA
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
R_{OUT}	Output Resistance ⁽⁴⁾ QS532807	$V_{CC} = \text{Min.}$	—	28	—	Ω

Notes:

1. Typical values indicate $V_{CC} = 3.3\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. Not more than one output should be used to test this high power condition, and the duration is ≤ 1 second.
3. Guaranteed by design but not production tested.
4. Output resistance represents the total output impedance of the logic device and includes added series termination resistance.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ ⁽³⁾	Max	Unit	
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$	0.01	100	μA	
ΔI_{CC}	Supply Current per Input HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.0\text{V}$ Input toggling @ 50% duty cycle	0.1	30	μA	
I_{CCD}	Dynamic Power Supply Current Per Output ⁽²⁾	$V_{CC} = \text{Max.}, \text{outputs enabled}$	60	90	$\mu\text{A}/\text{MHz}$	
I_C	Total Power Supply ^(2,4) Current	$V_{CC} = \text{Max.},$ Input @ 50% duty cycle, $f_I = 10\text{MHz}$	$V_{IN} = V_{CC} \text{ or}$ $V_{IN} = \text{GND}$	6.0	10	mA
		$V_{CC} = \text{Max.},$ Input @ 50% duty cycle, $f_I = 2.5\text{MHz}$	$V_{IN} = V_{CC} \text{ or}$ $V_{IN} = \text{GND}$	1.5	3.0	

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Guaranteed but not production tested. $C_L = 0\text{pF}$.
- Typical values are for reference only. Conditions are $V_{CC} = 3.3\text{V}$ and $T_A = 25^\circ\text{C}$.
- $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_O)(N_O)$
where:
 D_H = Input duty cycle
 N_T = Number of TTL HIGH inputs at D_H (one)
 f_O = Output Frequency
 N_O = Number of outputs at f_O (ten)

Table 6. Switching Characteristics Over Operating Range

Industrial: $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 3.3 \pm 0.3\text{V}$

For QS53807, $C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$.

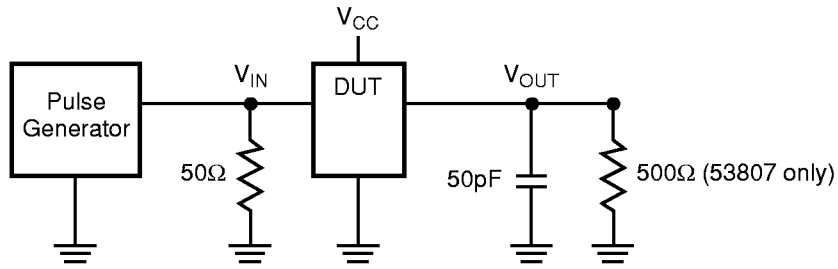
For QS532807, $C_{LOAD} = 50\text{pF}$ (no resistor)

Symbol	Description ⁽¹⁾	—		A		Unit
		Min	Max	Min	Max	
$t_{SK(01)}$	Skew between outputs – same transition	—	0.5	—	0.35	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$)	—	0.5	—	0.35	
$t_{SK(t)}$	Part-to-part skew ⁽²⁾	—	1.0	—	0.75	
t_{PLH} t_{PHL}	Propagation Delay ⁽³⁾ IN to Ox	QS53807	1.5	4.8	1.5	4.3
		QS532807	1.5	5.2	1.5	4.8
t_R	Output Rise Time, 0.8V to 2.0V	QS53807	—	1.5	—	1.5
		QS532807	—	2.0	—	2.0
t_F	Output Fall Time, 2.0V to 0.8V	QS53807	—	1.5	—	1.5
		QS532807	—	2.0	—	2.0

Notes:

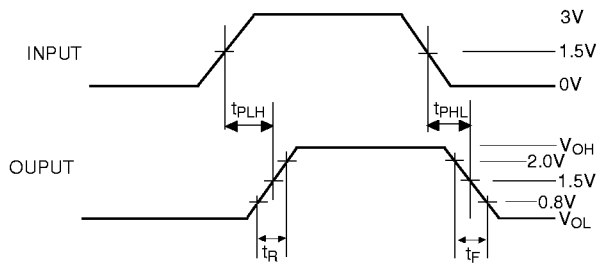
- Skew parameters are guaranteed but not production tested. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- $t_{SK(t)}$ only applies to devices of the same transition, part type, temperature, power supply voltage, loading, package and speed grade.
- The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delay limits do not imply skew.

Figure 3. Test Circuits and Waveforms

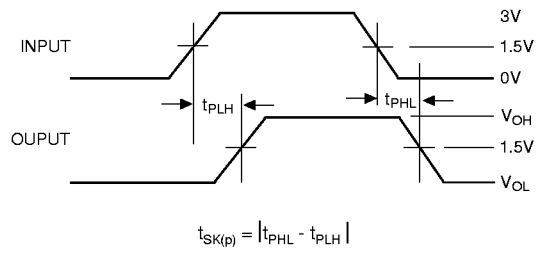


Pulse generator for all pulses: $f \leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

Test Circuit

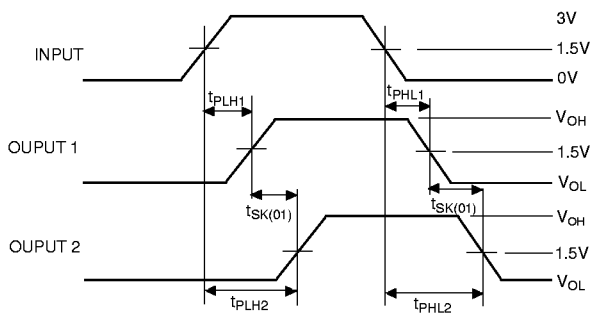


Propagation Delay



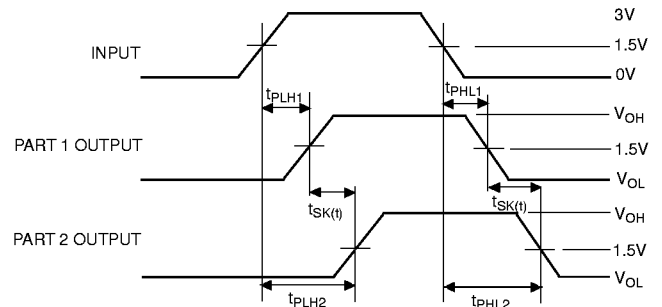
$$t_{SK(p)} = |t_{PHL} - t_{PLH}|$$

Pulse Skew - $t_{SK(p)}$



$$t_{SK(01)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Output Skew - $t_{SK(01)}$



$$t_{SK(t)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Part-to-Part Skew - $t_{SK(t)}$

Figure 3. Ordering Information

Example:

