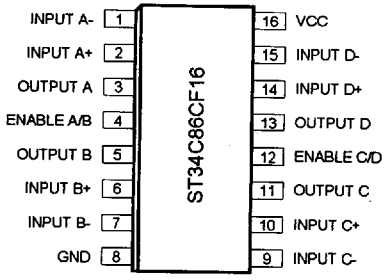
QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

GENERAL DESCRIPTION

The ST34C86 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST34C86 has an input sensitivity of 200mv over the common mode input voltage range of ± 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C86 circuit.

The ST34C86 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C86 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C86 is suitable for low power 5V operation.

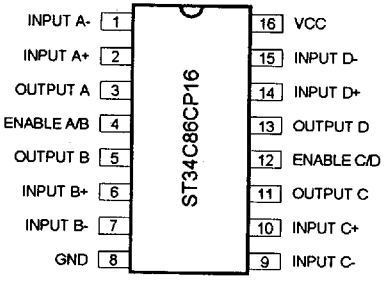
SOIC package



FEATURES

- Pin-to-pin compatible with National DS34C86
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

Plastic-DIP package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C86CP16	Plastic-DIP	0° C to + 70° C
ST34C86CF16	SOIC	0° C to + 70° C
ST34C86IP16	Plastic-DIP	-40° C to + 85° C
ST34C86IF16	SOIC	-40° C to + 85° C

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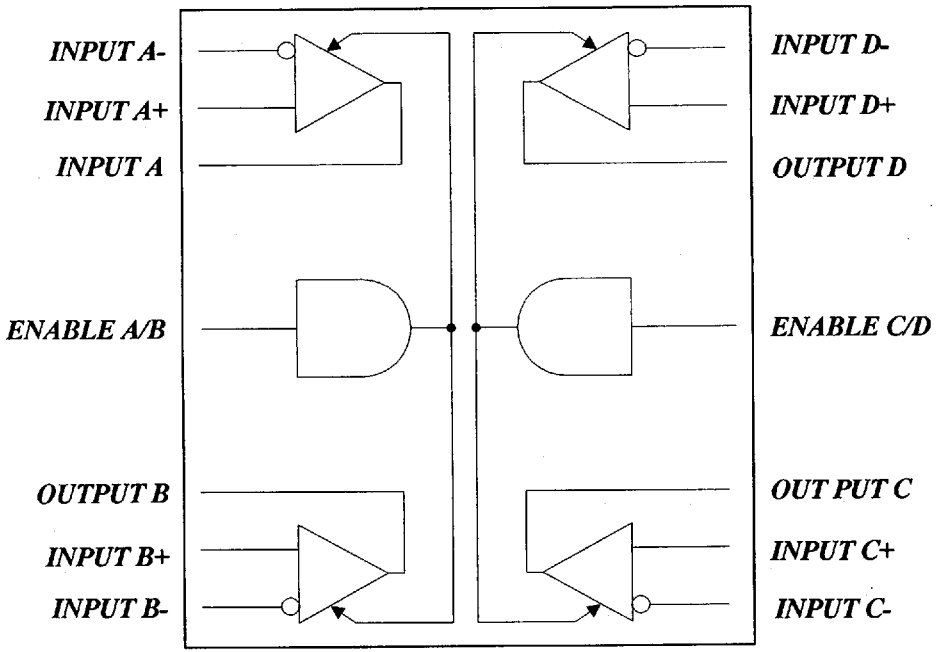
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE A/B	4	I	Gate control (active high). This pin enables/disables the two line receiver outputs (out A and out B).
OUTPUT B	5	O	Receiver B output pin.
INPUT B+	6	I	Receiver B differential non-inverting input pin.
INPUT B-	7	I	Receiver B differential inverting input pin.
GND	8	O	Signal and power ground.
INPUT C-	9	I	Receiver C differential inverting input pin.
INPUT C+	10	I	Receiver C differential non-inverting input pin.
OUTPUT C	11	O	Receiver C output pin.
ENABLE C/D	12	I	Gate control (active high). This pin enables/disables the two line receiver outputs (output C and output D).
OUTPUT D	13	O	Receiver D output pin.
INPUT D+	14	I	Receiver D differential non-inverting input pin.
INPUT D-	15	I	Receiver D differential inverting input pin.
VCC	16	I	Power supply pin.

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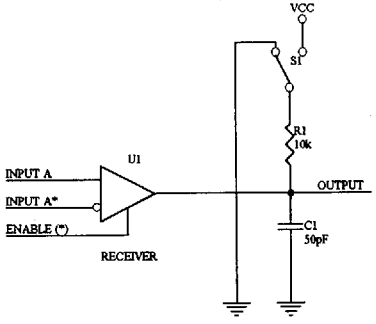
Functional table

Enable A/B C/D	Output	Differential Non-Inverting Input	Differential Inverting Input
L	Z	X	X
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	S1=VCC
T_2	Propagation delay, input to putput		18	20	ns	S1=GND
T_3	Output enable time		18	20	ns	V_{DIF}=2.5V
T_4	Output disable time		18	20	ns	V_{DIF}=2.5V

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any logic pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{OH}	Output high level	3.8	4.2		V	I_{OH}= -6mA
V_{OL}	Output low level			0.4	V	I_{OH}= 6mA
V_{ID}	Differential input level	-0.2		+0.2	V	-7V < V_{CM} < +7V
V_H	Input hysteresis		50		mV	
I_{IN}	Input current			±1.0	µA	
I_{CC}	Operating current		12		mA	V_{DIF}=+1V
I_{OZ}	Three state output leakage		±1.0	±5.0	µA	V_{OUT}=VCC or GND
I_{EN}	Enable input current		±1.0		µA	V_{IN}=VCC or GND
V_R	Input resistance	5		15	KΩ	-7V < V_{CM} < +7V

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DIFFERENTIAL LINE RECEIVER TIMING