

## 64Mb SDR SDRAM

### Features

- Clock frequency: 166, 143 MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Four banks operation
- Single 3.3V power supply
- LVTTTL interface
- Programmable burst length -- (1, 2, 4, 8, full page)
- Programmable burst sequence: Sequential/Interleave
- 4096 refresh cycles every 64 ms
- Random column address every clock cycle
- Programmable  $\overline{\text{CAS}}$  latency (2, 3 clocks)
- Burst read/write operation capability
- Burst termination by burst stop and precharge command
- Byte controlled by LDQM and UDQM
- Packages 400-mil 54-pin TSOP-II
- Lead-free package

### General Description

The NT5SV4M16 is a high-speed CMOS synchronous DRAM containing 67,108,864 bits. It is organized as 4 Banks of 1024K Words x 16 Bits DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

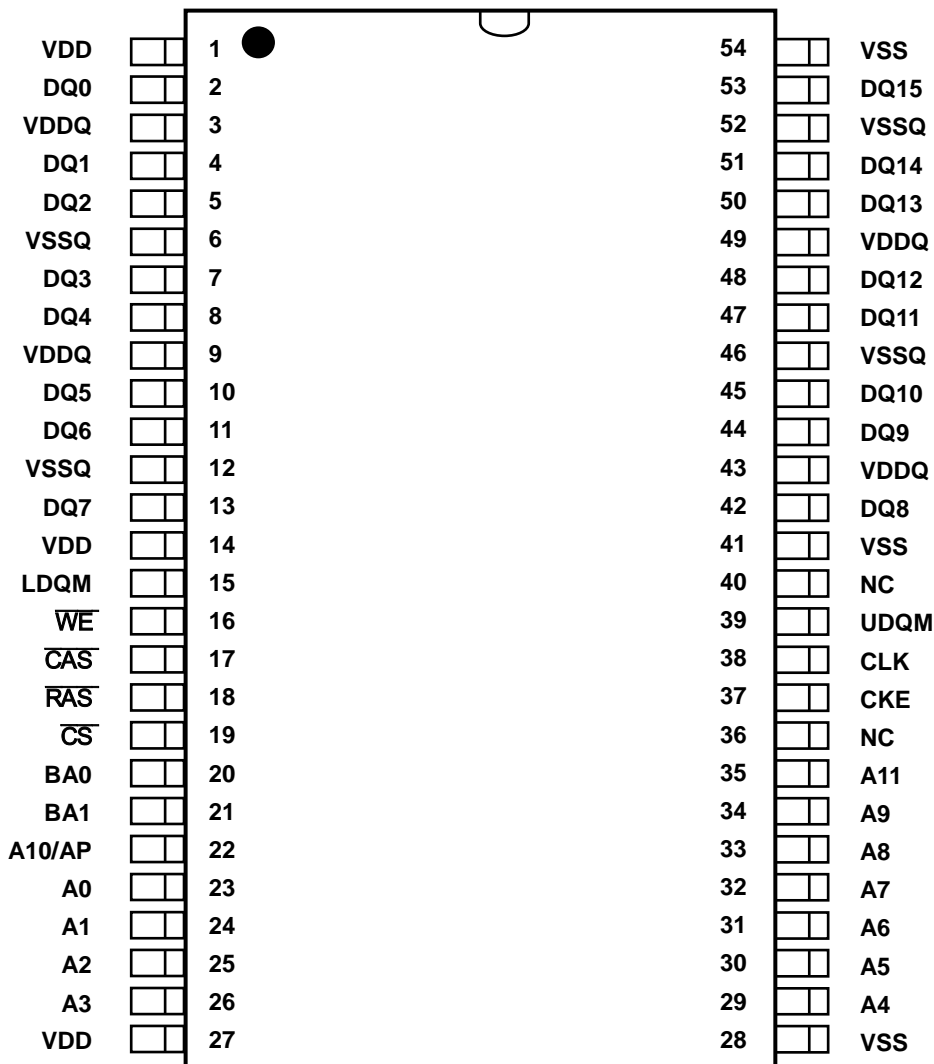
### Ordering Information

Commercial Range: 0°C to 70°C

Part No.	Organization	tCK	Frequency	Package
NT5SV16M4FS-6K	4M x 16	6ns	166MHz	400mil
NT5SV16M4FS-75B	4M x 16	7ns	133MHz	54-pin TSOPII

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Pin Assignment



Pin Descriptions

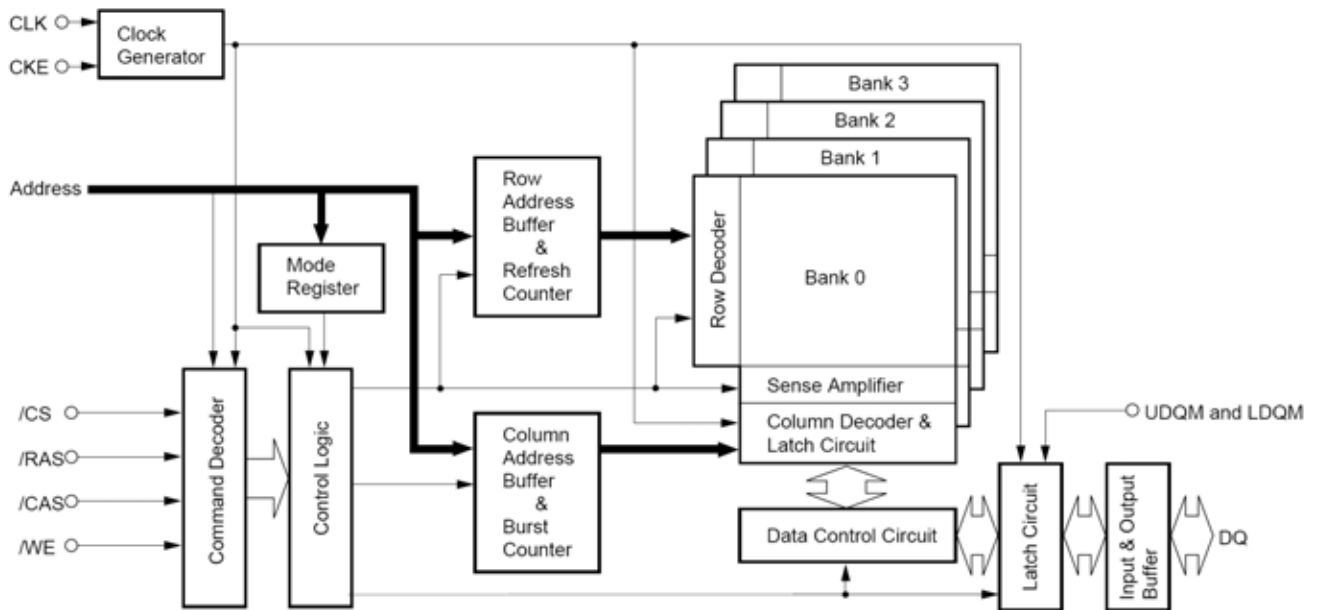
A0-A11	Address Input	$\overline{\text{CAS}}$	Column Address Strobe Command
A0-A11	Row Address Input	$\overline{\text{WE}}$	Write Enable
BA0,1	Bank Select Address	LDQM	Lower Byte, Input/Output Mask
A0-A7	Column Address Input	UDQM	Lower Byte, Input/Output Mask
DQ0-DQ15	Data DQ	VDD	Power
CLK	System Clock Input	VSS	Ground
CKE	Clock Enable	VDDQ	Power Supply for DQ Pin
$\overline{\text{CS}}$	Chip Select	VSSQ	Ground for DQ Pin
$\overline{\text{RAS}}$	Row Address Strobe Command	NC	No Connection

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## Pin Functions

Symbol	Type	Function
A0-A11	Input	<b>Address Inputs:</b> A0-A11 are used as row address inputs during active command input and A0-A7 as column address inputs during read or write command input. A10 is also used to determine the precharge mode during other commands. If A10 is LOW during precharge command, the bank selected by A11 is precharged, but if A10 is HIGH, both banks will be precharged. When A10 is HIGH in read or write command cycle, the precharge starts automatically after the burst access.
BA0, BA1	Input	<b>Bank Select:</b> Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
CLK	Input	<b>Clock:</b> CLK is driven by the system clock. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
CKE	Input	<b>Clock Enable:</b> The CKE input determines whether the CLK input is enables within the device. When CKE is HIGH, the next rising edge of the CLK signal will be valid, and when LOW, invalid. When CKE is LOW< the device will be in either the power-down mode, the clock suspend mode, or the self refresh mode. The CKE is an asynchronous input.
$\overline{CS}$	Input	<b>Chip Select:</b> $\overline{CS}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when $\overline{CS}$ is sampled HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
$\overline{RAS}$	Input	<b>Row Address Strobe:</b> $\overline{RAS}$ in conjunction with $\overline{CAS}$ and $\overline{WE}$ , forms the device command. See the "Command Truth Table" item for details on device commands.
$\overline{CAS}$	Input	<b>Column Address Strobe:</b> $\overline{CAS}$ in conjunction with $\overline{RAS}$ and $\overline{WE}$ , forms the device command. See the "Command Truth Table" item for details on device commands.
$\overline{WE}$	Input	<b>Write Enable:</b> $\overline{WE}$ in conjunction with $\overline{RAS}$ and $\overline{CAS}$ , forms the device command. See the "Command Truth Table" item for details on device commands.
LDQM, UDQM	Input	<b>Data Input/Output Mask:</b> LDQM and UDQM control the lower the upper bytes of the DQ buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enables, and when HIGH, disables. The outputs go to the HIGH impedance state when LDQM/UDQM is HIGH. In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is LOW the corresponding buffer byte is enables, and data can be written to the device. When LDQM or UDQM is HIGH, input data is masked and cannot be written to the device.
DQ0-DQ15	I/O	<b>Data I/O:</b> DQ0-15 are data input/output pins. DQ through these pins can be controlled in byte units using the LDQM and UDQM pins.
NC	-	<b>No Connect:</b> These pins should be left unconnected.
VDDQ	Supply	<b>DQ Power:</b> VDDQ is the output buffer power supply.
VDD	Supply	<b>Power Supply:</b> VDD is the device internal power supply.
VSS	Supply	<b>Ground:</b> VSS is the device internal ground.
VSSQ	Supply	<b>DQ Ground:</b> VSSQ is the output buffer ground

# Block Diagram



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## Absolute Maximum Rating

Symbol	Parameters	Rating	Unit
$V_{IN}, V_{OUT}$	Input, Output Voltage	-1.0 ~ +4.6	V
$V_{DD}, V_{DDQ}$	Power Supply Voltage	-1.0 ~ +4.6	V
$T_A$	Operating Temperature	0 ~ 70	°C
$T_{STG}$	Storage Temperature	- 55 ~ +125	°C
$P_D$	Power Dissipation	1	W
$I_{OS}$	Short Circuit Output Current	50	mA

**Note:** Permanent device damage may occur if Absolute Maximum Rating is exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability

Recommended DC Operating Conditions ( $T_A = 0\sim 70^\circ\text{C}$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
$V_{DD}, V_{DDQ}$	Power Supply Voltage,	3.0	3.3	3.6	V	
$V_{IH}$	Input High Voltage	2.0	–	$V_{DD} + 0.3$	V	1
$V_{IL}$	Input Low Voltage	-0.3	0	0.8	V	2
$V_{OH}$	Output High Voltage	2.4	–	–	V	$I_{OH} = -2\text{mA}$
$V_{OL}$	Output Low Voltage	–	–	0.4	V	$I_{OL} = 2\text{mA}$
$I_{IL}$	Input Leakage Voltage	-5	–	5	$\mu\text{A}$	3
$I_{OL}$	Output Leakage Voltage	-5	–	5	$\mu\text{A}$	4

**Note:**

- $V_{IH(\text{max})} = 4.6\text{V AC}$  for pulse width  $\leq 10\text{ns}$  acceptable.
- $V_{IL(\text{min})} = -1.5\text{V AC}$  for pulse width  $\leq 10\text{ns}$  acceptable.
- Any input  $0\text{V} \leq V_{IN} \leq V_{DD} + 0.3$ , all other pins are not under test = 0V.
- $V_{OUT}$  is disabled,  $0\text{V} \leq V_{OUT} \leq V_{DD}$

Capacitance ( $V_{DD} = 3.3\text{V}$ ,  $f = 1\text{MHz}$ ,  $T_a = 25^\circ\text{C}$ )

Symbol	Parameter	Min.	Max.	Unit
$C_{IN1}$	Input Capacitance: A0-A11	2	4	pF
$C_{IN2}$	Input Capacitance: (CLK, CKE, /CS, /RAS, /CAS, /WE, LDQM, UDQM)	2	4	pF
$C_{I/O}$	Input/Output Capacitance	2	5	pF

**Note:** These parameters are periodically sampled and are not 100% tested.

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DC Characteristics ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0\sim 70^{\circ}C$ )

Parameter/Test condition	Symbol	Max.		Unit
		-6	-7	
Operating Current $t_{RC} \geq t_{RC}(\min)$ , Outputs Open One bank active	$I_{DD1}$	85	80	mA
Precharge Standby Current in power down mode $t_{CK} = t_{CK}(\min)$ , $CKE \leq V_{IL}(\max)$	$I_{DD2P}$	2	2	
Precharge Standby Current in power down mode $t_{CK} = \infty$ , $CKE \leq V_{IL}(\max)$	$I_{DD2PS}$	2	2	
Precharge Standby Current in non-power down mode $t_{CK} = t_{CK}(\min)$ , $\overline{CS} \geq V_{IH}(\min)$ , $CKE \geq V_{IH}$ Input signals are changed very 2CLKs	$I_{DD2N}$	35	35	
Precharge Standby Current in non-power down mode $t_{CK} = \infty$ , $CLK \leq V_{IL}(\max)$ , $CKE \geq V_{IH}$	$I_{DD2NS}$	15	15	
Active Standby Current in power down mode $t_{CK} = t_{CK}(\min)$ , $CKE \leq V_{IL}(\max)$	$I_{DD3P}$	15	15	
Active Standby Current in power down mode $t_{CK} = \infty$ , $CKE \leq V_{IL}(\max)$	$I_{DD3PS}$	10	10	
Active Standby Current in non-power down mode $t_{CK} = t_{CK}(\min)$ , $CKE \geq V_{IH}(\min)$ , $\overline{CS} \geq V_{IH}(\min)$ Input signals are changed very 2clks	$I_{DD3N}$	30	30	
Active Standby Current in non-power down mode $CKE \geq V_{IH}(\min)$ , $CLK \leq V_{IL}(\max)$ , $t_{CK} = \infty$	$I_{DD3NS}$	25	25	
Operating Current (Burst mode) $t_{CK} = t_{CK}(\min)$ , Outputs Open, All banks active	$I_{DD4}$	150	140	
Refresh Current $t_{RC} \geq t_{RC}(\min)$	$I_{DD5}$	150	140	
Self Refresh Current $CKE \leq 0.2V$	$I_{DD6}$	2	2	

**Note:**

- $I_{DD1}$ ,  $I_{DD2N}$ ,  $I_{DD2P}$ ,  $I_{DD3N}$ ,  $I_{DD4}$ , and  $I_{DD5}$  depend on the cycle rate and these values are measured by the cycle rate under the minimum value of  $t_{CK}$  and  $t_{RC}$ . Input signals are changed one time during  $t_{CK}$ .
- $I_{DD1}$  and  $I_{DD4}$  depend on the output loading. Specified values are obtained with the output open.

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AC Characteristics ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0\sim 70^{\circ}C$ )<sup>(1,2,3)</sup>

Parameter	Symbol	-6		-7		Unit		
		Min.	Max.	Min.	Max.			
Clock Cycle Time	CL* = 3	t <sub>CK3</sub>	6	—	7	—	ns	
	CL* = 2	t <sub>CK2</sub>	10	—	10	—		
Clock High Time		t <sub>CH</sub>	2.5	—	2.5	—		
Clock Low Time		t <sub>CL</sub>	2.5	—	2.5	—		
Access Time from CLK (positive edge)	CL* = 3	t <sub>AC3</sub>	—	5.5	—	6		
	CL* = 2	t <sub>AC2</sub>	—	6	—	6		
Data Output Hold Time	CL* = 3	t <sub>OH3</sub>	2	—	2	—		
	CL* = 2	t <sub>OH2</sub>	2	—	2	—		
Data Output Low Impedance		t <sub>LZ</sub>	0	—	0	—		
Data Output High Impedance		t <sub>HZ</sub>	2	6	2	7		
Data/Address/Control Input Setup Time		t <sub>IS</sub>	1.5	—	1.5	—		
Data/Address/Control Input Hold Time		t <sub>IH</sub>	1	—	1	—		
Command Period (ACT to ACT)		t <sub>RC</sub>	60	—	65	—		
Command Period (REF to REF)		t <sub>RFC</sub>	60	—	70	—		
Command Period (ACT to PRE)		t <sub>RAS</sub>	42	100K	45	100K		
Command period (PRE to ACT)		t <sub>RP</sub>	18	—	20	—		
Active Command to Read /Write Command Delay Time		t <sub>RCD</sub>	18	—	20	—		
Command Period (ACT[0] to ACT[1])		t <sub>RRD</sub>	12	—	14	—		
WRITE recovery time		t <sub>WR</sub>	2	—	2	—		tCK
Input Data to Column Address Delay Time		t <sub>CDL</sub>	1	—	1	—		
Input Data to Precharge Command Delay Time		t <sub>DPL</sub>	2	—	2	—		
Input Data to Burst Stop Delay Time		t <sub>BDL</sub>	1	—	1	—		
Column Address to Column Address Delay Time		t <sub>CCD</sub>	1	—	1	—		
Transition Time		t <sub>T</sub>	—	1	—	1	ns	
Refresh Cycle Time (2048)		t <sub>REF</sub>	—	64	—	64	ms	

\* CL is CAS# Latency.

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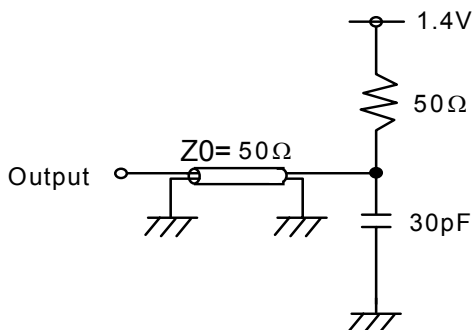
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**Note:**

1. When power is first applied, memory operation should be started 100 $\mu$ s after  $V_{DD}$  and  $V_{DDQ}$  reach their stipulated voltage. Also note that the power-on sequence must be executed before starting memory operation.
2. Measured with  $t_T = 1$ ns.
3. The reference level is 1.4V when measuring input signal timing. Rise and fall times are measured between  $V_{IH}$  (min.) and  $V_{IL}$ (max.).
4.  $t_{HZ}$  (max.) is defined as the time required for the output voltage to transition by  $\pm 200$ mV from  $V_{OH}$ (min.) or  $V_{OL}$  (max.) when the output is in the high impedance state.
5. If  $t_T \geq 1$ ns, parameters are changed as follows;  
 $t_{CH}$ ,  $t_{CL}$ ,  $t_{IS}$ ,  $t_{IH}$ : should be added  $\{[t_T \text{ (rise)} + t_T \text{ (fall)}]/2 - 1\}$

**AC Operating Test Conditions ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0\sim70^{\circ}C$ )**

Parameter	Value
Input Signal Levels (Vih/Vil)	2.4V / 0.4V
Reference Level of Output Signals	1.4V
Output Load	Reference to the Under Output Load
Transition Time (Rise and Fall) of Input Signals	1ns
Reference Level of Input Signals	1.4V



**LVTTTL A.C. Test Load**

## 64Mb SDR SDRAM

### Commands

#### Mode Register Set Command

( $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$  = LOW)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore, the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting LOW on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  (The SDRAM should be in active mode should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0-A11 and BA0-1 in the same cycle as  $\overline{CA}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  going LOW is the data written in the mode register. Two clock cycles are required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields into depending on functionality. The burst length field use A0-A2, Burst type uses A3,  $\overline{CAS}$  latency (read latency from column address) use A4-A6, vendor specific options or test mode use A7-A8, A10/AP-A11 and BA0-1. The write burst length is programmed using A9. A7-A8, A10/AP-A11, and BA0-1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and  $\overline{CAS}$  latency.

#### Active Command

( $\overline{CS}$ ,  $\overline{RAS}$  = LOW,  $\overline{CAS}$ ,  $\overline{WE}$  = HIGH)

This SDRAM includes four banks of 4,096 rows each. This command address BA0,1 selects one of the four banks according and activates the row selected by the pins A0 to A11. This command corresponds to the fall of the  $\overline{RAS}$  signal from HIGH to LOW in conventional DRAMs.

#### Precharge Command

( $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{WE}$  = LOW,  $\overline{CAS}$  = HIGH)

This command begins precharge operation of the bank selected by pins A10/AP and BA0-1. When A10 is HIGH, all banks are precharged at the same time. When A10 is LOW, the bank selected by BA0-1 is precharged. After executing this command, the next command for the selected bank(s) is executed after passage of the period  $t_{RP}$ , which is the period required for bank precharging. This Command corresponds to the  $\overline{RAS}$  signal from LOW to HIGH in conventional DRAMs.

#### Read Command

( $\overline{CS}$ ,  $\overline{CAS}$  = LOW,  $\overline{RAS}$ ,  $\overline{WE}$  = HIGH)

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This command selects the bank specified by the BA0-1 pins and begins a burst read operation at the start address specified by pin A0 to A11. Data is output following  $\overline{\text{CAS}}$  latency. The selected bank must be activated before executing this command. This Command corresponds to the  $\overline{\text{RAS}}$  signal from LOW to HIGH in conventional DRAMs. When the A10/AP pin is HIGH, this command functions as a read with Auto Precharge command. After the burst read completes, the bank selected by pin A11 is precharged. When A10 pin is LOW, the bank selected by the BA0-1 pins remains in the activated state after the burst read completes.

### Write Command

( $\overline{\text{CS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  = LOW, /RAS = HIGH)

When burst write mode has been selected with the mode register set command, this command selects the bank specified by the BA0-1 pins pin and begins a burst write operation at the start address specified by pins A0 to A11. This first data must be input to the DQ pins in the cycle with this command. The selected bank must be activated before executing this command. When A10/AP pin is HIGH, this command functions as a write with Auto Precharge command. After the burst write completes, the bank selected by pin BA0-1 is precharged. When the A10/AP pin is LOW, the bank selected by the BA0-1 pins remains in the activated state after the burst write completes.

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### Auto Refresh Command

$(\overline{CS}, \overline{RAS}, \overline{CAS} = \text{LOW}, \overline{WE}, \text{CKE} = \text{HIGH})$

This command executes the Auto Refresh operation. The row address and bank to be refreshed are automatically generated during this operation. All banks must be placed in the idle state before executing this command. The stipulated period ( $t_{RC}$ ) is required for a single refresh operation, and no other commands can be executed during this period. The SDRAM goes to the idle state after the internal refresh operation completes. This command must be executed at least 4096 times every 64ms. This command corresponds to CBR Auto Refresh in conventional DRAMs.

### Self Refresh Command

$(\overline{CS}, \overline{RAS}, \overline{CAS}, \text{CKE} = \text{LOW}, \overline{WE} = \text{HIGH})$

This command executes the Self Refresh operation. The row address, the bank, and the refresh interval to be refreshed are automatically generated internally during this operation. The Self Refresh operation is started by dropping the CKE pin from HIGH to LOW. The Self Refresh operation continues as long as the CKE pin remains LOW and there is no need for external control of any other pins. The Self Refresh operation is terminated by raising the CKE pin from LOW to HIGH. The next command cannot be executed until the SDRAM internal recovery period ( $t_{RC}$ ) has elapsed. After the Self Refresh, since it is impossible to determine the address of the last row to be refreshed, an Auto Refresh should immediately be performed for all addresses (4,096 cycles).

### Burst Stop Command

$(\overline{CS}, \overline{WE} = \text{LOW}, \overline{RAS}, \overline{CAS} = \text{HIGH})$

This command forcibly terminates burst read and write operations. When this command is executed during a burst read operation, data output stops after the  $\overline{CAS}$  latency period has elapsed.

### No Operation

$(\overline{CS} = \text{LOW}, \overline{RAS}, \overline{CAS}, \overline{WE} = \text{HIGH})$

This command has no effect on the SDRAM.

### Device Deselect Command

$(\overline{CS} = \text{HIGH})$

This command does not select the SDRAM for an object of operation. In other words, it performs no operation with respect to the SDRAM.

## 64Mb SDR SDRAM

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### Power Down Command

(CKE = LOW)

When both banks are in the idle state, or when at least one of the banks is not in the idle state, this command can be used to suppress device power dissipation by reducing device internal operations to the absolute minimum. Power Down mode is started by dropping the CKE pin from HIGH to LOW. Power Down mode continues as long as the CKE pin is held LOW. All pins other than CEK pins are invalid and none of the other commands can be executed in this mode. The Power Down operation is terminated by raising the CKE pin from LOW to HIGH. The next command cannot be executed until the recovery period ( $t_{CKA}$ ) has elapsed. Since this command differs from the Self Refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period ( $t_{REF}$ ). Thus the maximum time that Power Down mode can be held is just under the refresh cycle time.

## 64Mb SDR SDRAM

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### Clock Suspend

(CKE = LOW)

This command can be used to stop the SDRAM internal clock temporarily during a read or write cycle. Clock Suspend mode is started by dropping the CKE pin from HIGH to LOW. Clock suspend mode continues as long as the CKE pin is held LOW. All input pins other than the CKE pin are invalid and none of the other commands can be executed in this mode. Also note that the SDRAM internal state is maintained. Clock Suspend mode is terminated by rising the CKE pin from LOW to HIGH, at which point SDRAM operation restarts, the next command cannot be executed until the recovery period ( $t_{CKA}$ ) has elapsed. Since this command differs from the Self Refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period ( $t_{REF}$ ). Thus the maximum time that Clock Suspend mode can be held is just under the refresh cycle time.

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Command Truth Table<sup>(1,2)</sup>

Command	Symbol	CKE <sub>n-1</sub>	CKE <sub>n</sub>	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0-1	A10	A0-A11	DQ
Mode Register Set <sup>(3,4)</sup>	MRS	H	X	L	L	L	L	X	OP CODE			X
Auto Refresh <sup>(5)</sup>	REF	H	H	L	L	L	H	X	X	X	X	High-Z
Self Refresh <sup>(5,6)</sup>	SREF	H	L	L	L	L	H	X	X	X	X	High-Z
Precharge Selected Bank	PRE	H	X	L	L	H	L	X	V	L	X	X
Precharge All Banks	PALL	H	X	L	L	H	L	X	X	H	X	X
Bank Activate <sup>(7)</sup>	ACT	H	X	L	L	H	H	X	V	Row address		X
Write	WRIT	H	X	L	H	L	L	X	V	L	Column address <sup>(18)</sup>	X
Write and Auto Precharge <sup>(8)</sup>	WRITA	H	X	L	H	L	L	X	V	H		X
Read <sup>(8)</sup>	READ	H	X	L	H	L	H	X	V	L	Column address <sup>(18)</sup>	X
Read and Auto precharge <sup>(8)</sup>	READA	H	X	L	H	L	H	X	V	H		X
Burst Stop <sup>(9)</sup>	BST	H	X	L	H	H	L	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X	X
Device Deselect	DESL	H	X	H	X	X	X	X	X	X	X	X
Clock Suspend Mode	SBY	L	X	X	X	X	X	X	X	X	X	X
Data Write/Output Enable	ENB	H	X	X	X	X	X	L	X	X	X	Active
Data Mask/Output Disable	MASK	H	X	X	X	X	X	H	X	X	X	High-Z

DQM Truth Table<sup>(1,2)</sup>

Command	Symbol	CKE <sub>n-1</sub>	CKE <sub>n</sub>	UDQM	LDQM
Data Write/Output Enable	ENB	H	X	L	L
Data Mask/Output Disable	MASK	H	X	H	H
Upper Byte Data Write/Output Enable	ENBU	H	X	L	X
Lower Byte Data Write/Output Enable	ENBL	H	X	X	L
Upper Byte Data Mask/Output Disable	MASKU	H	X	H	X
Lower Byte Data Mask/Output Disable	MASKL	H	X	X	H

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CKE Truth Table<sup>(1,2)</sup>

Command	Symbol	Current State	CKE <sub>n-1</sub>	CKE <sub>n</sub>	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-1	A10	A0-A11
Start Clock Suspend Mode	SPND	Active	H	L	X	X	X	X	X	X	X
Clock Suspend	—	Other States	L	L	X	X	X	X	X	X	X
Terminate Clock Suspend Mode	—	Clock Suspend	L	H	X	X	X	X	X	X	X
Auto Refresh	REF	Idle	H	H	L	L	L	H	X	X	X
Start Self Refresh Mode	SELF	Idle	H	L	L	L	L	H	X	X	X
Terminate Self Refresh Mode	SELFX	Self Refresh	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
Start Power Down Mode	PDWN	Idle	H	L	L	H	H	H	X	X	X
			H	L	H	X	X	X	X	X	X
Terminate Power Down Mode	—	Power Down	L	H	X	X	X	X	X	X	X

## Operation Command Table<sup>(1,2)</sup>

Current State	Command	Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-1	A10	A0-A11
Idle	DESL	No Operation or Power Down <sup>(12)</sup>	H	X	X	X	X	X	X
	NOP	No Operation or Power Down <sup>(12)</sup>	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Row Active	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	No Operation	L	L	H	L	V	V	X
	REF/SELF	Auto Refresh or Self Refresh	L	L	L	H	X	X	X
	MRS	Mode Register Set	L	L	L	L	OP CODE		
Row Active	DESL	No Operation	H	X	X	X	X	X	X
	NOP	No Operation	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Read Start <sup>(17)</sup>	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Write Start <sup>(17)</sup>	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal <sup>(10)</sup>	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Precharge <sup>(15)</sup>	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Read	DESL	Burst Read Continues, Row Active When Done	H	X	X	X	X	X	X
	NOP	Burst Read Continues, Row Active When Done	L	H	H	H	X	X	X
	BST	Burst Interrupted, Row Active After Interrupt	L	H	H	L	X	X	X
	READ/READA	Burst Interrupted, Read Start After Interrupt <sup>(16)</sup>	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Burst Interrupted, Write Start After Interrupt <sup>(11,16)</sup>	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal <sup>(10)</sup>	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Burst Read Interrupted, Precharge After Interrupt	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		

**Operation Command Table<sup>(1,2)</sup> (Cont.)**

Current State	Command	Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-1	A10	A0-A11
Write	DESL	Burst Write Continues, Write Recovery When Done	H	X	X	X	X	X	X
	NOP	Burst Write Continues, Write Recovery When Done	L	H	H	H	X	X	X
	BST	Burst Write Interrupted, Row Active After Interrupt	L	H	H	L	X	X	X
	READ/READA	Burst Write Interrupted, Read Start After Interrupt <sup>(16)</sup>	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Burst Write Interrupted, Write Restart After Interrupt <sup>(11,16)</sup>	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal <sup>(10)</sup>	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Burst Write Interrupted, Precharge After Interrupt	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Read With Auto Precharge	DESL	Burst Read Continues, Precharge When Done	H	X	X	X	X	X	X
	NOP	Burst Read Continues, Precharge When Done	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal <sup>(10)</sup>	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Illegal <sup>(10)</sup>	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Write With Auto Precharge	DESL	Burst Write Continues, Write Recovery and Precharge When Done	H	X	X	X	X	X	X
	NOP	Burst Write Continues, Write Recovery and Precharge When Done	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal <sup>(10)</sup>	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Illegal <sup>(10)</sup>	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		

**Operation Command Table<sup>(1,2)</sup> (Cont.)**

Current State	Command	Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-1	A10	A0-A11
Row Precharge	DESL	No Operation, Idle State After $t_{RP}$ Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Idle State After $t_{RP}$ Has Elapsed	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal <sup>(10)</sup>	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Illegal <sup>(10)</sup>	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal <sup>(10)</sup>	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	No Operation, Idle State After $t_{RP}$ Has Elapsed <sup>(10)</sup>	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Immediately Following Row Active	DESL	No Operation, Row Active After $t_{RCD}$ Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Row Active After $t_{RCD}$ Has Elapsed	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal <sup>(10)</sup>	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Illegal <sup>(10)</sup>	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal <sup>(10,14)</sup>	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Illegal <sup>(10)</sup>	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Write Recovery	DESL	No Operation, Row Active After $t_{DLP}$ Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Row Active After $t_{DLP}$ Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Row Active After $t_{DLP}$ Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Read Start	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Write Start	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal <sup>(10)</sup>	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Illegal <sup>(10)</sup>	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		

**Operation Command Table<sup>(1,2)</sup> (Cont.)**

Current State	Command	Operation	$\overline{CS}$	RAS	CAS	WE	BA0-1	A10	A0-A11
Write Recovery With Auto Precharge	DESL	No Operation, Idle State After $t_{DAL}$ Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Row Active After $t_{DLP}$ Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Row Active After $t_{DLP}$ Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Illegal <sup>(10)</sup>	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Illegal <sup>(10)</sup>	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal <sup>(10)</sup>	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Illegal <sup>(10)</sup>	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
MRS	Illegal	L	L	L	L	OP CODE			
Refresh	DESL	No Operation, Idle State After $t_{RFC}$ Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Idle State After $t_{RFC}$ Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Idle State After $t_{RFC}$ Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Illegal	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
MRS	Illegal	L	L	L	L	OP CODE			
Mode Register Set	DESL	No Operation, Idle State After 2 clocks Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Idle State After 2 clocks Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Idle State After 2 clocks Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V <sup>(18)</sup>
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V <sup>(18)</sup>
	ACT	Illegal	L	L	H	H	V	V	V <sup>(18)</sup>
	PRE/PALL	Illegal	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
MRS	Illegal	L	L	L	L	OP CODE			

## 64Mb SDR SDRAM

**Note for Command Rule Table, DQM Truth Table, CKE Truth Table, Operation Command Table:**

1. H: HIGH level input, L: LOW level input, X: HIGH or LOW level input, V: Valid data input.
2. All input signals are latched on the rising edge of the CLK signal.
3. Both banks must be placed in the idle state in advance.
4. The states of the A0 to A11 pins are loaded into the mode register as an OP CODE.
5. The row address is generated automatically internally at this time. The DQ pin and the address pin data are ignored.
6. During a self refresh operation, all pin data (states) other than CKE is ignored.
7. The selected bank must be placed in the idle state in advance.
8. The selected bank must be placed in the active state in advance.
9. This command is valid only when the burst length set to full page.
10. This is possible depending on the state of the bank selected by the BA0-1 pins.
11. Time to switch internal busses is required.
12. The device can be switched to power down mode by dropping the CKE pin LOW when both banks in the idle state. Input pins other than CKE are ignored at this time.
13. The device can be switched to self refresh mode by dropping the CKE pin LOW when both banks in the idle state. Input pins other than CKE are ignored at this time.
14. Possible if  $t_{RRD}$  is satisfied.
15. Illegal if  $t_{RAS}$  is not satisfied.
16. The conditions for burst interruption must be observed. Also note that the device will enter the precharged state immediately after the burst operation completes if auto precharge is selected.
17. Command input becomes possible after the period  $t_{RCD}$  has elapsed. Also note that the device will enter the precharge state immediately after the burst operation completes if auto precharge is selected.
18. A8, A9 = don't care.

**CKE Command Truth Table<sup>(1)</sup>**

Current State	Operation	CKE <sub>n-1</sub>	CKE <sub>n</sub>	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-1	A10	A0-A11
Self Refresh	Undefined	H	X	X	X	X	X	X	X	X
	Self Refresh Recovery <sup>(2)</sup>	L	H	H	X	X	X	X	X	X
	Self Refresh Recovery <sup>(2)</sup>	L	H	L	H	H	H	X	X	X
	Illegal	L	H	L	H	H	L	X	X	X
	Illegal <sup>(2)</sup>	L	H	L	H	L	X	X	X	X
	Illegal <sup>(2)</sup>	L	H	L	L	X	X	X	X	X
	Self Refresh	L	L	X	X	X	X	X	X	X
Self Refresh Recovery	Idle State After $t_{RC}$ Has Elapsed	H	H	H	X	X	X	X	X	X
	Idle State After $t_{RC}$ Has Elapsed	H	H	L	H	H	X	X	X	X
	Illegal	H	H	L	H	L	X	X	X	X
	Illegal	H	H	L	L	X	X	X	X	X
	Power Down On Next Cycle	H	L	H	X	X	X	X	X	X
	Power Down On Next Cycle	H	L	L	H	H	X	X	X	X
	Illegal	H	L	L	H	L	X	X	X	X
	Illegal	H	L	L	L	X	X	X	X	X
	Clock Suspend Termination On Next Cycle	L	H	X	X	X	X	X	X	X
	Clock Suspend	L	L	X	X	X	X	X	X	X

## CKE Command Truth Table<sup>(1)</sup> (Cont.)

Current State	Operation	CKE <sub>n-1</sub>	CKE <sub>n</sub>	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-1	A10	A0-A11
Power Down	Undefined	H	X	X	X	X	X	X	X	X
	Power Down Mode Termination, Idle Afterwards <sup>(2)</sup>	L	H	X	X	X	X	X	X	X
	Power Down Mode	L	L	X	X	X	X	X	X	X
All Banks Idle	No Operation	H	H	H	X	X	X	X	X	X
	See Operation Command Table	H	H	L	H	X	X	X	X	X
	Bank Active Or Precharge	H	H	L	L	H	X	X	X	X
	Auto Refresh	H	H	L	L	L	H	X	X	X
	See Operation Command Table	H	H	L	L	L	L	OP CODE		
	Power Down On Next Cycle	H	L	H	X	X	X	X	X	X
	See Operation Command Table	H	L	L	H	X	X	X	X	X
	See Operation Command Table	H	L	L	L	H	X	X	X	X
	Self Refresh <sup>(3)</sup>	H	L	L	L	L	H	X	X	X
	See Operation Command Table	H	L	L	L	L	L	OP CODE		
	Power Down Mode <sup>(3)</sup>	L	X	X	X	X	X	X	X	X
Other States	See Operation Command Table	H	H	X	X	X	X	X	X	X
	Clock Suspend On Next Cycle <sup>(4)</sup>	H	L	X	X	X	X	X	X	X
	Clock Suspend Termination On Next Cycle	L	H	X	X	X	X	X	X	X
	Clock Suspend Termination On Next Cycle	L	L	X	X	X	X	X	X	X

### Note:

1. H: HIGH level input, L: LOW level input, X: HIGH or LOW level input.
2. The CLK pin and the other input are reactivated asynchronously by the transition of the CKE level from LOW to HIGH. The minimum setup time ( $t_{CKA}$ ) required before all commands other than mode termination must be satisfied.
3. Both banks must be set to the idle state in advance to switch to power down mode or self refresh mode.
4. The input must be command defined in the Operation Command Table.

## Bank Selection and Precharge Address Allocation

Bank active at read/write are controlled by BA0-1

BA0	BA1	Active & Read/Write
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

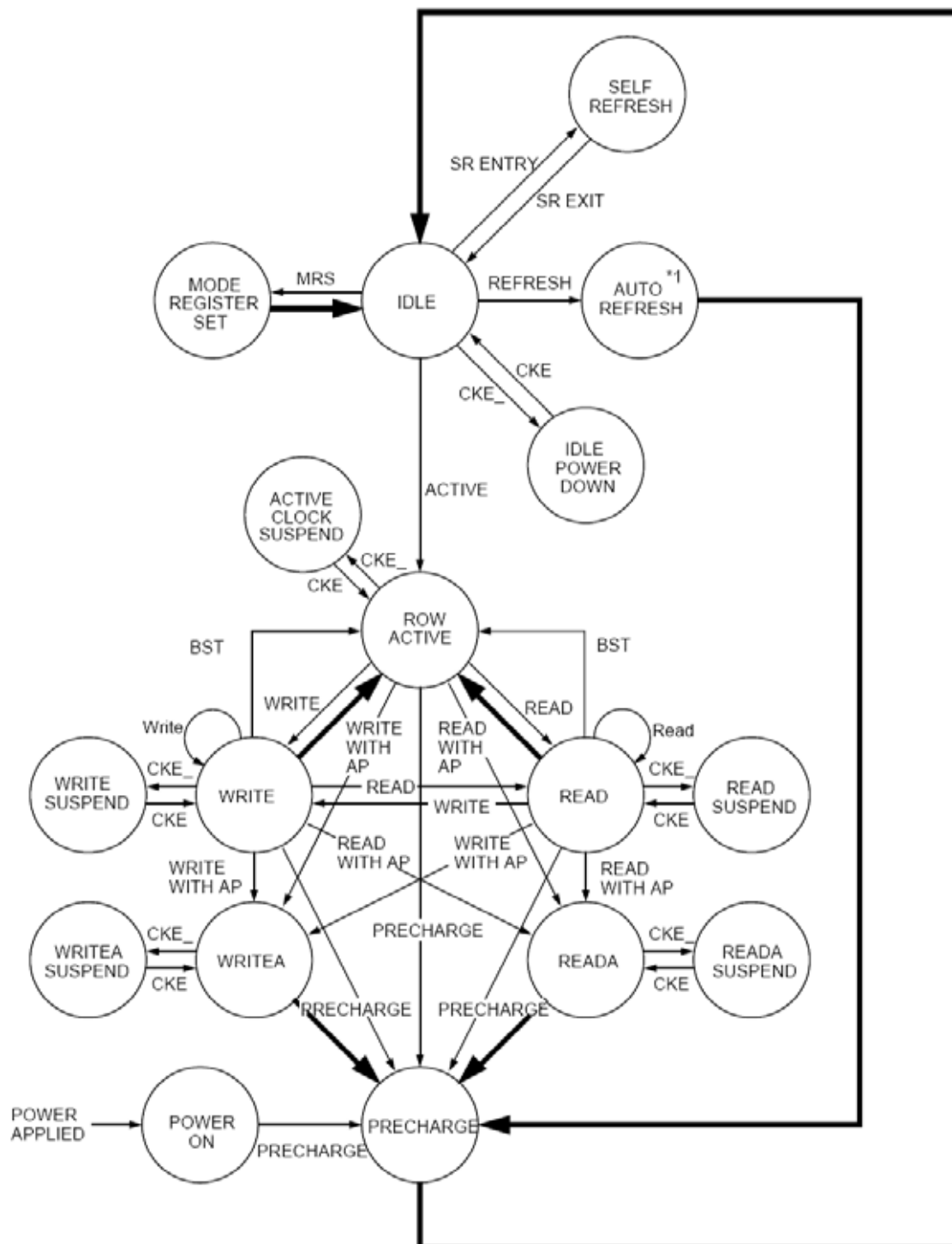
Enable and disable Auto Precharge function are controlled by A10/AP in read/write command

A10/AP	BA0	BA1	Operation
0	0	0	Disable Auto Precharge, leave Bank 0 active at end of burst
	0	1	Disable Auto Precharge, leave Bank 1 active at end of burst
	1	0	Disable Auto Precharge, leave Bank 2 active at end of burst
	1	1	Disable Auto Precharge, leave Bank 3 active at end of burst
1	0	0	Enable Auto Precharge, precharge Bank 0 at end of burst
	0	1	Enable Auto Precharge, precharge Bank 1 at end of burst
	1	0	Enable Auto Precharge, precharge Bank 2 at end of burst
	1	1	Enable Auto Precharge, precharge Bank 3 at end of burst

A10/AP and BA0-1 control bank precharge when precharge is asserted

A10/AP	BA0	BA1	Precharge
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	X	X	All Banks

### Simplified State Diagram



➡ Automatic transition after completion of command.

➡ Transition resulting from command input.

Note: After the Auto Refresh operation, Precharge operation is performed automatically and enter the IDLE state.

## 64Mb SDR SDRAM

### Function Descriptions

#### Device Initialization At Power On

(Power On Sequence)

1. Apply power and start clock, attempt to maintain CKE = "H", DQM = "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for minimum of 200 $\mu$ s.
3. Issue precharge commands for all banks of the SDRAM.
4. Issue 2 or more Auto Refresh commands.
5. Issue a mode register set command to initialize the mode register.

Sequence of 4 and 5 is regardless of the order. The SDRAM is now ready for normal operation.

#### Mode Register Settings

The mode register set command sets the mode register. When this command is executed, pins A0 to A9, A11, A10, and BA0-1 function as data input pins for setting the register, and this data becomes the device internal OP CODE. This OP CODE has fields as listed in the table below.

Input Pin	Field
BA0, BA1	Mode Options
A11, A10,	Mode Options
A9	Write Burst Length
A8, A7	Test Mode
A6, A5, A4	/CAS Latency
A3	Burst Type
A2, A1, A0	Burst Length

Note that the mode register set command can be executed only when both banks are in the idle state. Wait at least two cycles after executing a mode register set command before executing the next command.

#### $\overline{\text{CAS}}$ Latency

During a read operation, between the execution of the read command and data output is stipulated as the  $\overline{\text{CAS}}$  latency. This period can be set using the mode register set command. The optimal  $\overline{\text{CAS}}$  latency is determined by the clock frequency and device speed grade. See the table of Operating Frequency / Latency Relationships for details on the relation ship between the clock frequency and the  $\overline{\text{CAS}}$  latency. See the table of the Mode Register for details.

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### Burst Length

When writing or reading, data can be input or output continuously. In these operations, an address is input only once and that address is taken as the starting address internally by the SDRAM. The SDRAM then automatically generates the following address. The burst length field in the mode register stipulates the number of data items input or output in sequence. In the SDRAM, a burst length of 1, 2, 4, 8, or full page can be specified. See the table of the Mode Register for details.

### Burst Type

The burst data order during a read or write operation is stipulated by the burst type, which can be set by the mode register set command. The SDRAM supports sequential mode and interleaved mode burst type settings. See the table of the Mode Register for details. Also see the table of Burst Length and Column Address Sequence for details on DQ data orders in these modes.

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Mode Register

Address	BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU		RFU		WBL	TM		LT Mode			BT	BL		

	A2	A1	A0	Sequential	Interleave
Burst Length	0	0	0	1	1
	0	0	1	2	2
	0	1	0	4	4
	0	1	1	8	8
	1	0	0	Reserved	Reserved
	1	0	1	Reserved	Reserved
	1	1	0	Reserved	Reserved
	1	1	1	Full Page	Reserved

	A3	Type
Burst Type	0	Sequential
	1	Interleaved

	A6	A5	A4	/CAS Latency
Latency Mode	0	0	0	Reserved
	0	0	1	Reserved
	0	1	0	2
	0	1	1	3
	1	0	0	Reserved
	1	0	1	Reserved
	1	1	0	Reserved
	1	1	1	Reserved

	A8	A7	Test Mode
Test Mode	0	0	Mode Register Set
	0	1	Reserved
	1	0	Reserved
	1	1	Reserved

	A9	Type
Write Burst Length	0	Burst
	1	Single

## Burst Length And Column Address Sequence

Burst Length	Column Address			Address Sequence	
	A2	A1	A0	Sequential	Interleaved
2	X	X	0	0-1	0-1
	X	X	1	1-0	1-0
4	X	0	0	0-1-2-3	0-1-2-3
	X	0	1	1-2-3-0	1-0-3-2
	X	1	0	2-3-0-1	2-3-0-1
	X	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

## Burst Length Control

Basic Mode	1	At MRS A210 = "000" At Auto Precharge $t_{RAS}$ should not be violated
	2	At MRS A210 = "001" At Auto Precharge $t_{RAS}$ should not be violated
	4	At MRS A210 = "010"
	8	At MRS A210 = "011"
	Full Page	At MRS A210 = "111" At the end of the burst length, burst is wrap-around
Random Mode	Burst Stop	$t_{BDL}=1$ , valid DQ after burst stop is 1, 2 for $\overline{CAS}$ latency 2, 3, respectively. Using burst stop command, and burst length control is possible.
Interrupt Mode	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst. Row precharge command of the same bank stops read/read burst with Auto Precharge. $t_{RDL}=1$ with DQM, valid DQ after burst stop is 1, 2 for $\overline{CAS}$ latency 2, 3, respectively. During read/write burst with Auto Precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with Auto Precharge, $\overline{CAS}$ interrupt can not be issued.

## Burst Type Control

Basic Mode	Sequential Counting	At MRS A3 = "0". See the Burst Length and Column Address Sequence Table. BL = 1, 2, 4, 8, and full page.
	Interleave Counting	At MRS A3 = "0". See the Burst Length and Column Address Sequence Table. BL = 1, 2, 4, 8. At BL = 1, 2, Interleave Counting = Sequential Counting
Random Mode	Random Column Access $t_{CCD} = 1 \text{ CLK}$	Every cycle read/write command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.



## Operation of the SDRAM

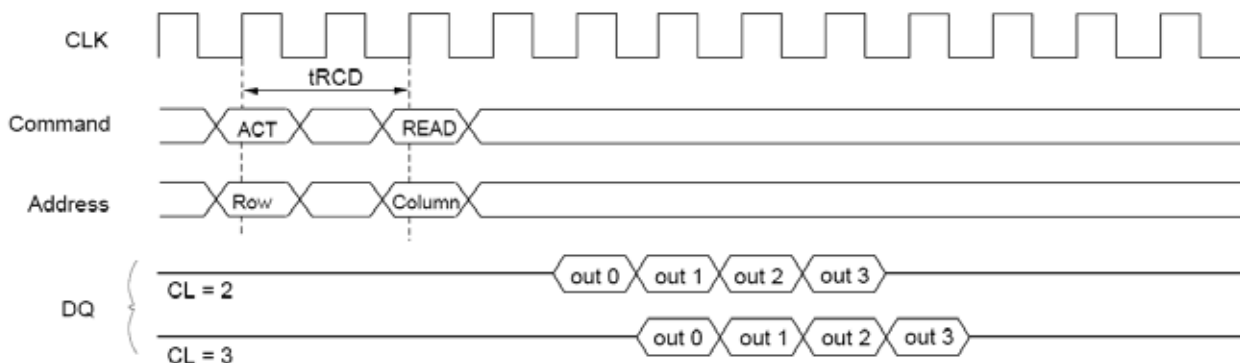
### Read/Write Operations

#### Bank Active

Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACT) command. An interval of  $t_{RCD}$  is required between the bank active command input and the following read/write command input.

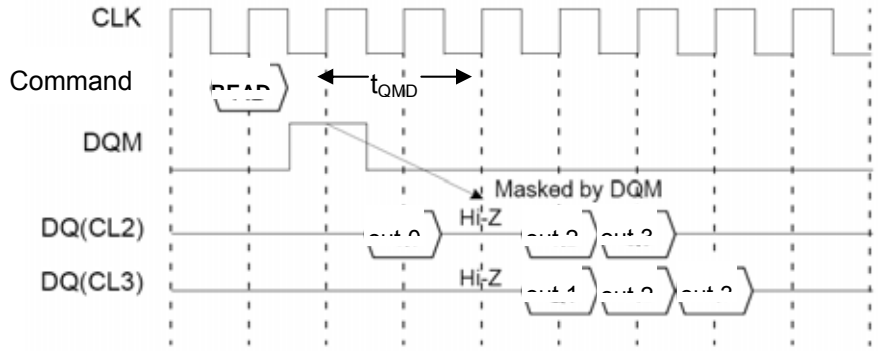
#### Burst Read

The Read cycle is started by executing the read command. The address provided during read command execution is used as the starting address. First, the data corresponding to this address is output in synchronization with the clock signal after  $\overline{CAS}$  latency period. Next, data corresponding to an address generated automatically by the device is output in synchronization with the clock signal. The output buffers go to the LOW impedance state  $\overline{CAS}$  latency minus one cycle after the read command, and go to the HIGH impedance state automatically after the last data is output. However, the case where the burst length is a full page is an exception. In this case output buffers must be set to the high impedance state by executing a burst stop command. Note that upper byte and lower byte output data can be masked in dependently under control of the signals applied to the U/LQM pins. The delay period ( $t_{QMD}$ ) is fixed at two, regardless of the  $\overline{CAS}$  latency setting, when this function is used. The selected bank must be set to the active state before executing this command.



**Burst Read Operation (Burst Length = 4,  $\overline{CAS}$  Latency = 2, 3)**

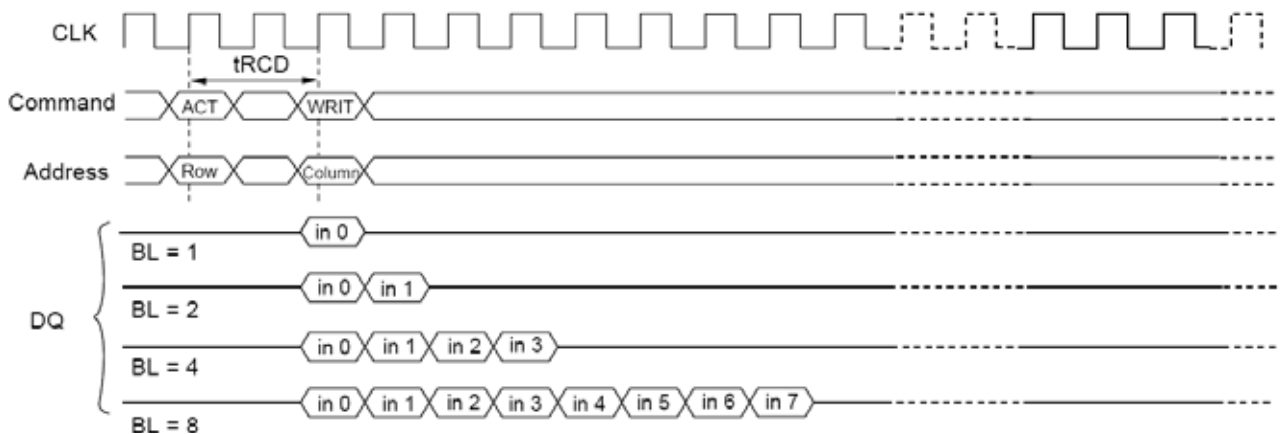
64Mb SDR SDRAM



**Burst Read masked by DQM Operation (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 2, 3)**

**Burst Write**

The Write cycle is started by executing the command. The address provided during write command execution is used as the starting address, at the same time, data for this address is input in synchronization with the clock signal. Next, data is input in other in synchronization with the clock signal. During this operation, data is written to address generated automatically by the device. This cycle terminates automatically after a number of clock cycles determined by the stipulated burst length. However, the case where the burst length is a full page is an exception. In this case the write cycle must be terminated by executing a burst stop command. The latency for DQ pin data input is zero, regardless of the  $\overline{\text{CAS}}$  latency setting. However, a wait period (write recovery: tDPL) after the last data input is required for the device to complete the write operation. Note that the upper byte and lower byte input data can be masked independently under control of the signal applied to the U/LQM pins. The delay period (t<sub>DMD</sub>) is fixed at zero, regardless of the  $\overline{\text{CAS}}$  latency setting, when this function is used. The selected bank must be set to the active state before executing this command.



**Burst Write Operation (Burst Length = 1, 2, 4, 8,  $\overline{\text{CAS}}$  Latency = 2, 3)**

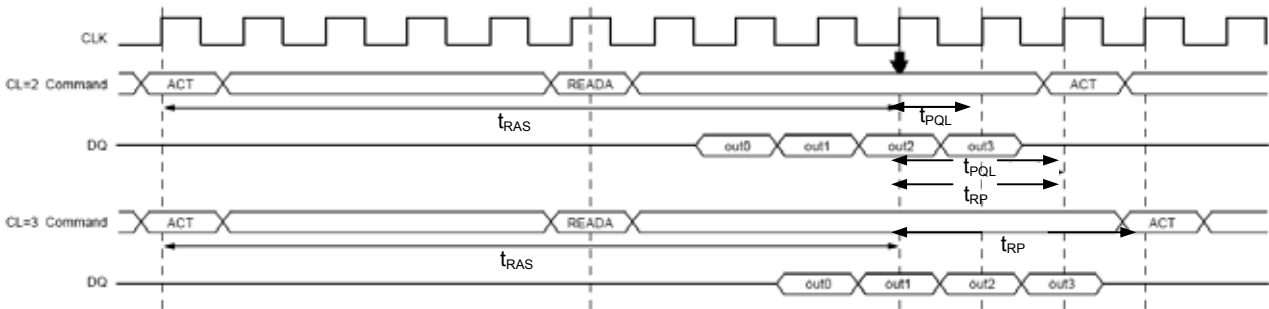
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Auto Precharge Operations

Read With Auto-Precharge

The Read With Auto Precharge command first executes a burst read operation and then puts the selected bank in the precharge state automatically. After the precharge completes, the bank goes to the idle state. Thus this command performs a read command and a precharge command in a single operation. During this operation, the delay period ( $t_{PQL}$ ) between the last burst data output and the start of the precharge operation differs depending on the  $\overline{CAS}$  latency setting. When the  $\overline{CAS}$  latency setting is two, the precharge operation starts on one clock cycle before the last burst data is output ( $t_{PQL} = -1$ ). When the  $\overline{CAS}$  latency setting is three, the precharge operation starts on two clock cycles before the last burst data is output ( $t_{PQL} = -2$ ). Therefore, the selected bank can be made active after a delay of  $t_{RP}$  from the start position of this precharge operation. The selected bank must be set to the active state before executing this command. The Auto Precharge function is invalid if the burst length is set to full page.

$\overline{CAS}$ Latency	3	2
$t_{PQL}$	-2	-1



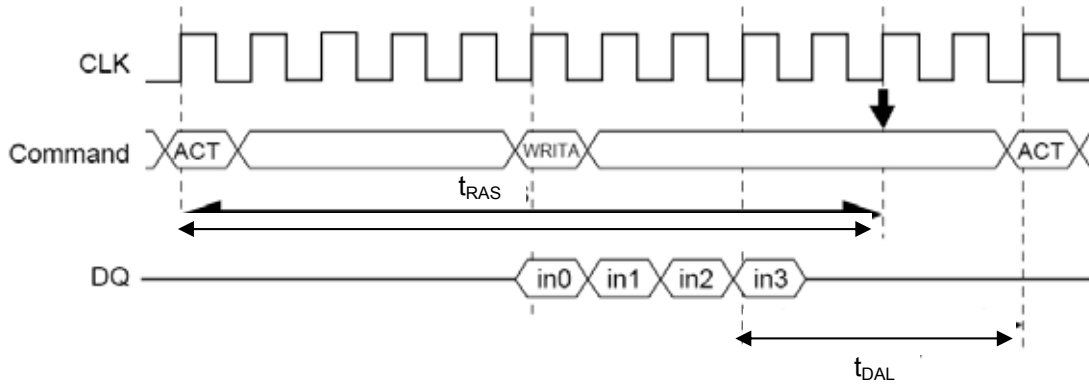
Read With Auto Precharge Operation (Burst Length = 4,  $\overline{CAS}$  Latency = 2, 3)

Write With Auto-Precharge

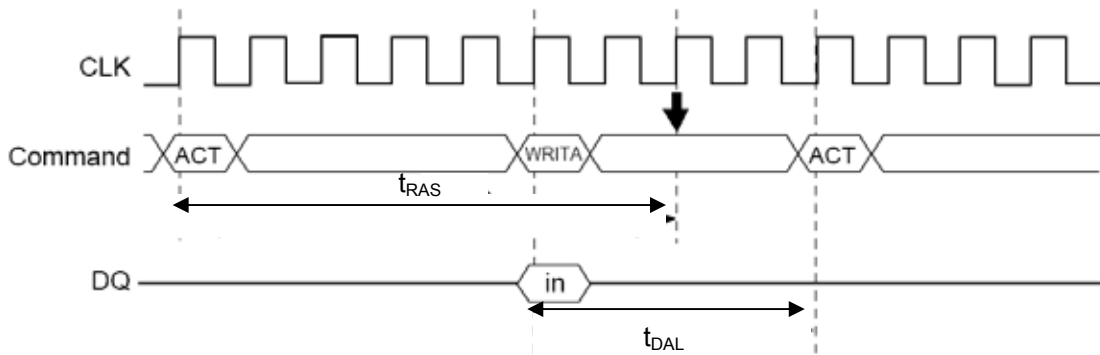
The Write With Auto Precharge command first executes a burst write operation and then puts the selected bank in the precharge state automatically. After the precharge completes, the bank goes to the idle state. Thus this command performs a write command and a precharge command in a single operation. During this operation, the delay period ( $t_{DAL}$ ) between the last burst data output and the completion of the precharge operation differs depending on the  $\overline{CAS}$  latency setting. The delay ( $t_{DAL}$ ) is  $t_{RP}$  plus one CLK period. That is, the precharge operation starts one clock period after the last burst data input. Therefore, the selected bank can be made active after a delay of  $t_{DAL}$ . The selected bank must be set to the active state before executing this command. The Auto Precharge function is invalid if the burst length is set to full page.

$\overline{CAS}$ Latency	3	2
$t_{DAL}$	1CLK + $t_{RP}$	1CLK + $t_{RP}$

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Write With Auto Precharge Operation (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 3)



Write With Auto Precharge Operation (Single Write,  $\overline{\text{CAS}}$  Latency = 3)

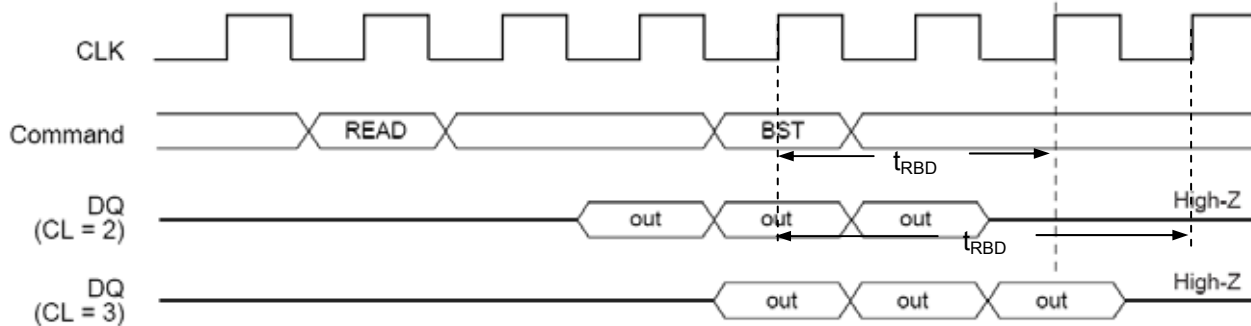
**Burst Stop Operations**

**Burst Stop At Read**

The SDRAM can output data continuously from the burst start address (a) to location a + 255 during a read cycle in which the burst length is set to full page. The SDRAM repeats the operation starting at the 256<sup>th</sup> cycle with the data output returning to location (a) and continuing with a+1, a+2, a+3, etc. A burst stop command must be executed to terminate this cycle. A precharge command must be executed within the ACT to PRE command period ( $t_{\text{RAS max.}}$ ) following the burst stop command. After the period ( $t_{\text{RBD}}$ ) required for burst data output to stop following the execution of the burst stop command has elapsed, the outputs go to the HIGH impedance state. This period  $t_{\text{RBD}}$  is two clock cycles when the  $\overline{\text{CAS}}$  latency is two and three clock cycle when the  $\overline{\text{CAS}}$  latency is three.

$\overline{\text{CAS}}$ Latency	3	2
$t_{\text{RBD}}$	3	2

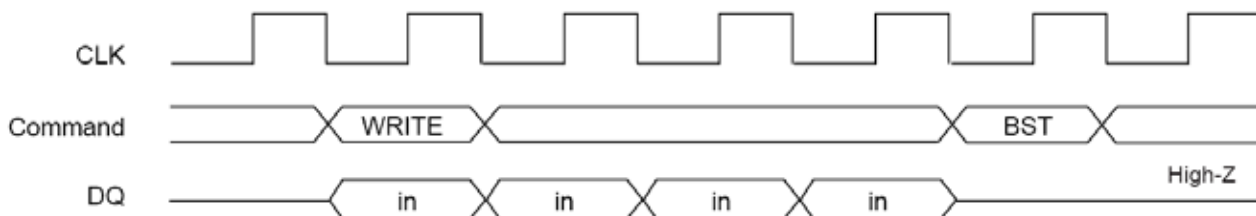
64Mb SDR SDRAM



**Burst Stop At Read Operation (Burst Length = Full,  $\overline{\text{CAS}}$  Latency = 2, 3)**

**Burst Stop At Write**

The SDRAM can input data continuously from the burst start address (a) to location a + 255 during a write cycle in which the burst length is set to full page. The SDRAM repeats the operation starting at the 256<sup>th</sup> cycle with the data input returning to location (a) and continuing with a+1, a+2, a+3, etc. A burst stop command must be executed to terminate this cycle. A precharge command must be executed within the ACT to PRE command period ( $t_{\text{RAS max.}}$ ) following the burst stop command. After the period ( $t_{\text{WBD}}$ ) required for burst data input to stop following the execution of the burst stop command has elapsed, the write cycle terminates. This period  $t_{\text{WBD}}$  is zero clock cycle, regardless of the  $\overline{\text{CAS}}$  latency.



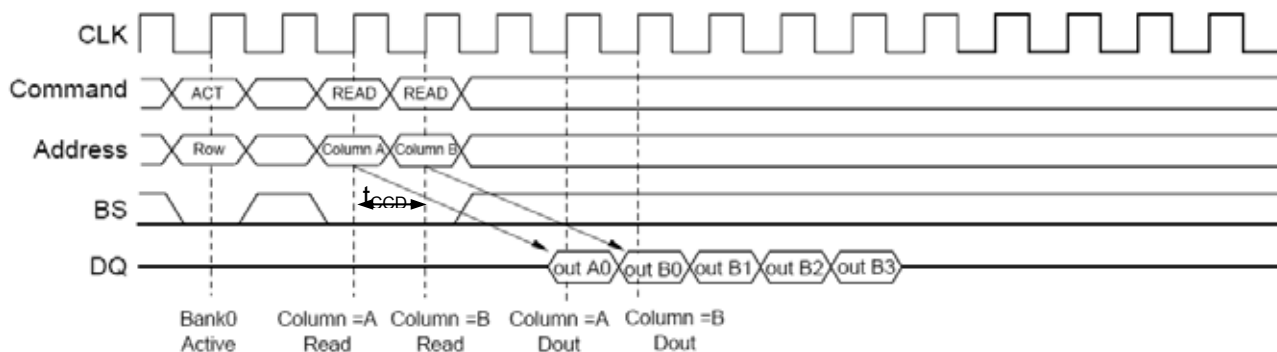
**Burst Stop At Write Operation (Burst Length = Full,  $\overline{\text{CAS}}$  Latency = 2, 3)**

**Command Intervals**

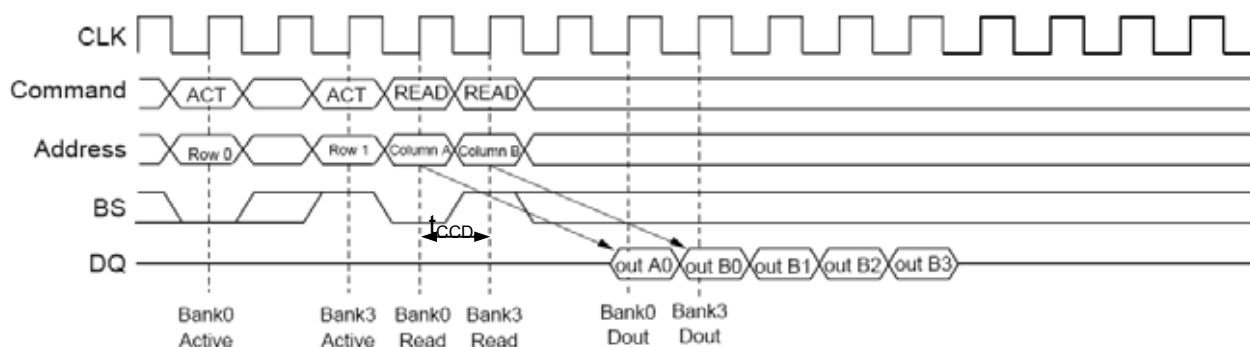
**Read To Read Interval**

A new command can be executed while a read cycle is in progress, i.e. before that cycle completes. When the second read command is executed, after the  $\overline{\text{CAS}}$  latency has elapsed, data corresponding to the new read command is output in place of the data due to the previous read command. The interval between two read commands ( $t_{\text{CCD}}$ ) must be at least one clock cycle. The selected bank must be set to the active state before executing this command.

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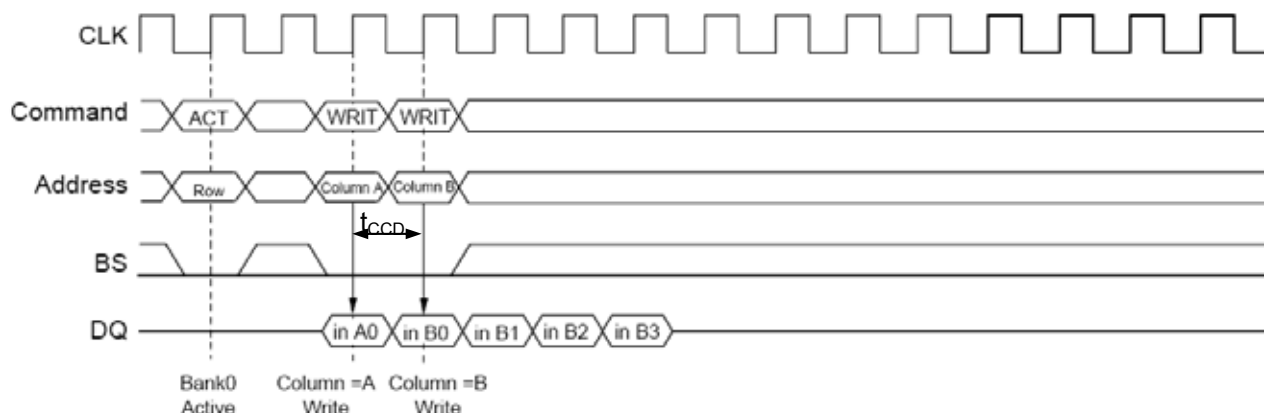
**Read To Read Command Interval, Same ROW address in same bank**  
**(Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 3)**



**Read To Read Command Interval, different bank (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 3)**

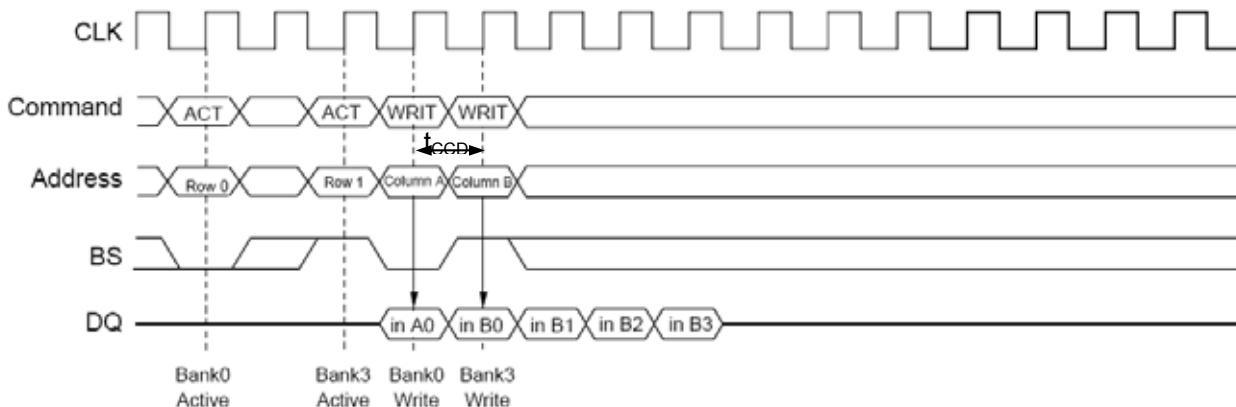
**Write To Write Interval**

A new command can be executed while a write cycle is in progress, i.e. before that cycle completes. When the second read command is executed, data corresponding to the new write command can be input in place of the data due for the previous write command. The interval between two write commands ( $t_{CCD}$ ) must be at least one clock cycle. The selected bank must be set to the active state before executing this command.



**Write To Write Command Interval, Same ROW address in same bank**  
**(Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 2, 3)**

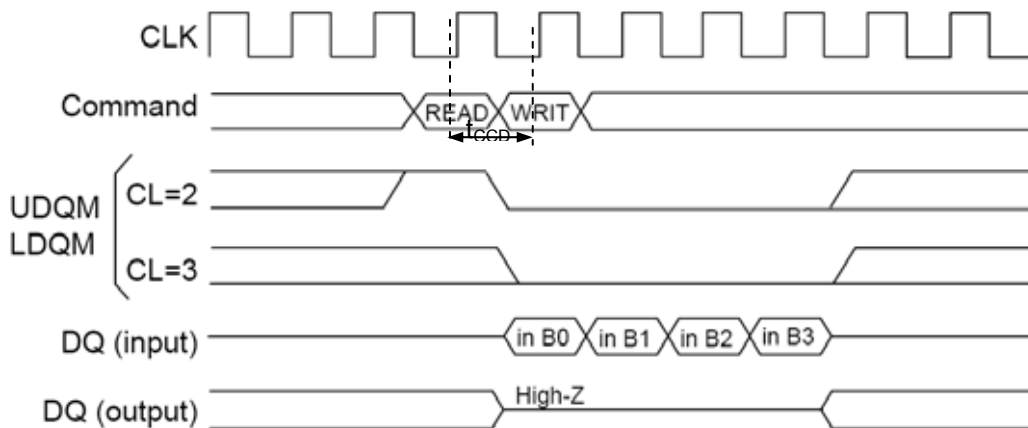
64Mb SDR SDRAM



Write To Write Command Interval, different bank (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 2, 3)

Read To Write Interval

A read command can be interrupted and a new write command executed while the read cycle is in progress, i.e. before that cycle completes. Data corresponding to the new write command can be input at the point new write command is executed. To prevent collision between input and output data at the DQn pins during this operation, the output data must be masked using the U/LDQM pins. The interval ( $t_{\text{CCD}}$ ) between these commands must be at least on clock cycle. The selected bank must be set to the active state before executing this command.

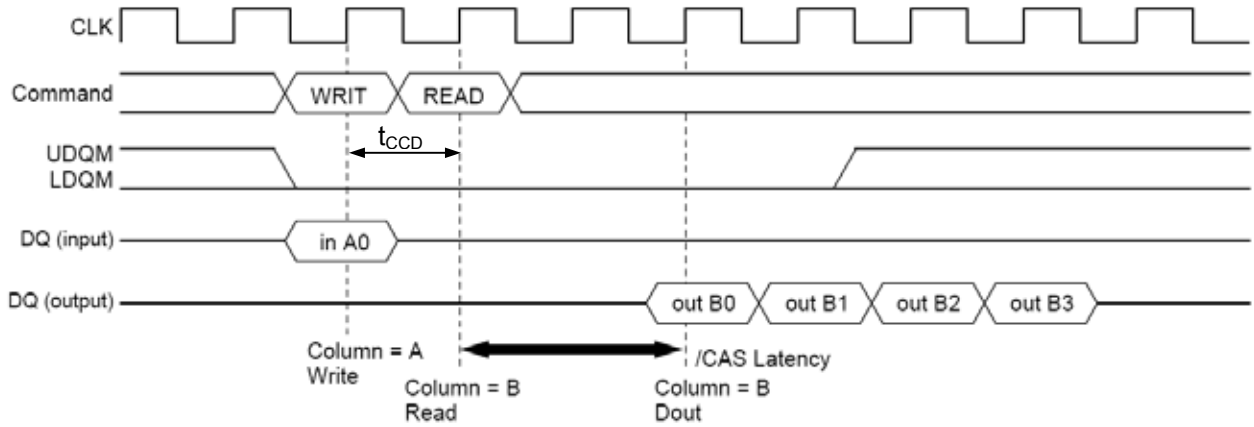


Read To Write Command Interval (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 2)

**64Mb SDR SDRAM**

**Write To Read Interval**

A new command can be executed while the read a write cycle is in progress, i.e. before that cycle completes. Data corresponding to the new read command is output after the  $\overline{\text{CAS}}$  latency has elapsed from the point the new read command was executed. The I/On pins must be placed in the HIGH impedance state at least one cycle before data is output during this operation. The interval ( $t_{\text{CCD}}$ ) between these commands must be at least on clock cycle. The selected bank must be set to the active state before executing this command.

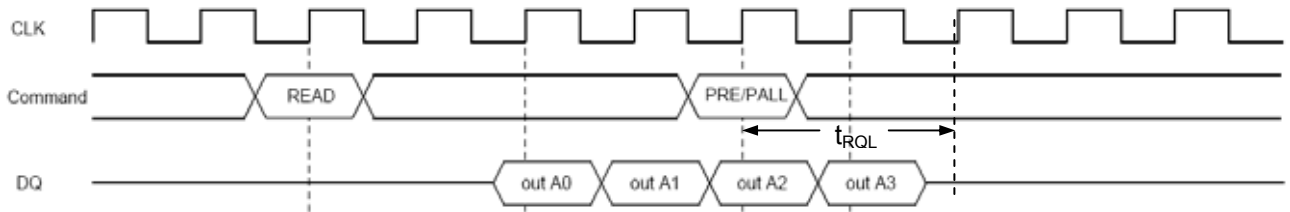


**Write To Read Command Interval (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 2)**

**Read To Precharge Interval**

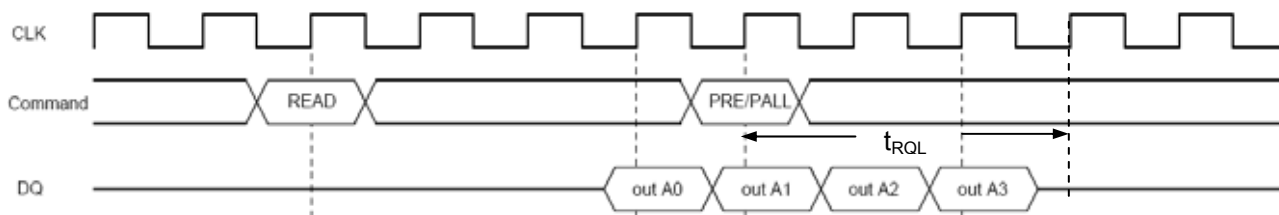
A read cycle can be interrupted by the execution of the precharge command before that cycle completes. The delay time ( $t_{\text{RQL}}$ ) from the execution of the precharge command to the completion of the burst output is the clock cycle  $\overline{\text{CAS}}$  latency.

$\overline{\text{CAS}}$ Latency	3	2
$t_{\text{RQL}}$	3	2



**Read To Precharge Command Interval (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 2)**

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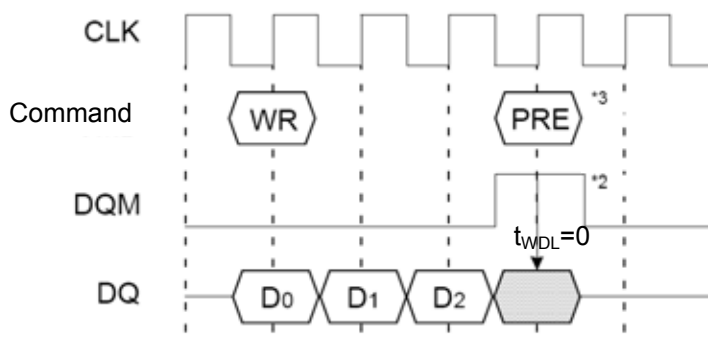


Read To Precharge Command Interval (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 3)

Write To Precharge Interval

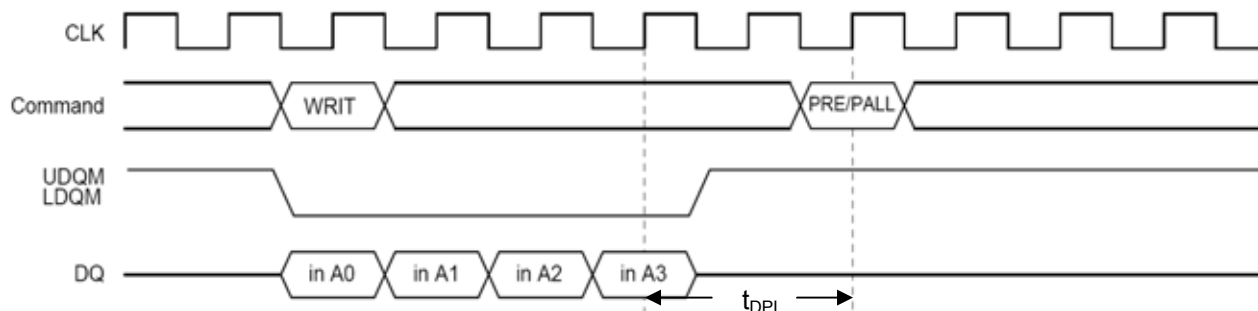
A write cycle can be interrupted by the execution of the precharge command before that cycle completes. The delay time ( $t_{\text{WDL}}$ ) from the precharge command to the point where burst input is invalid, i.e. the point where input data is no longer written to device internal memory is zero clock cycle regardless of the  $\overline{\text{CAS}}$  latency. To inhibit invalid write, the DQM signal must be asserted HIGH with the precharge command. This precharge command and burst write command must be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual bank operation. Inversely, to write all the burst data to the device, the precharge command must be executed after the write data recovery period ( $t_{\text{DPL}}$ ) has elapsed. Therefore, the precharge command must be executed on one clock cycle that follows the input of the last burst data item.

$\overline{\text{CAS}}$ Latency	3	2
$t_{\text{WDL}}$	0	0
$t_{\text{DPL}}$	2	2



Write To Precharge Command Interval masked by DQM (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 2)

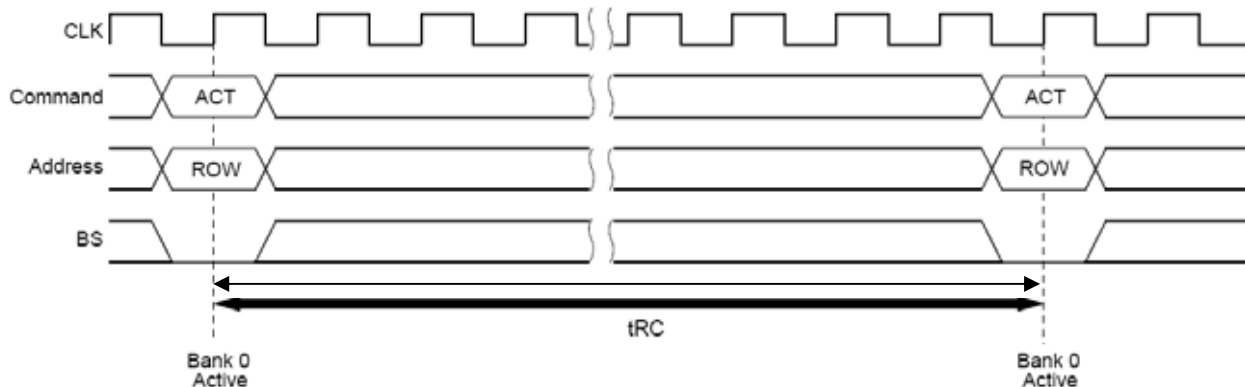
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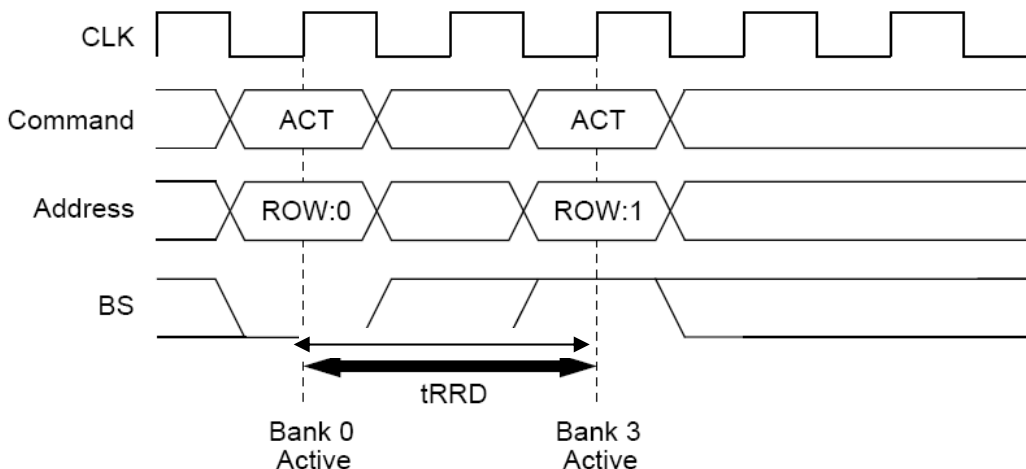
Write To Precharge Command Interval (Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 3)

Bank Active Command Interval

The interval between the two bank active commands must be no less than  $t_{RC}$ . In the case of different bank active commands, the interval between the two bank active commands must be no less than  $t_{RRD}$ .



Bank Active to Bank Active for the same bank

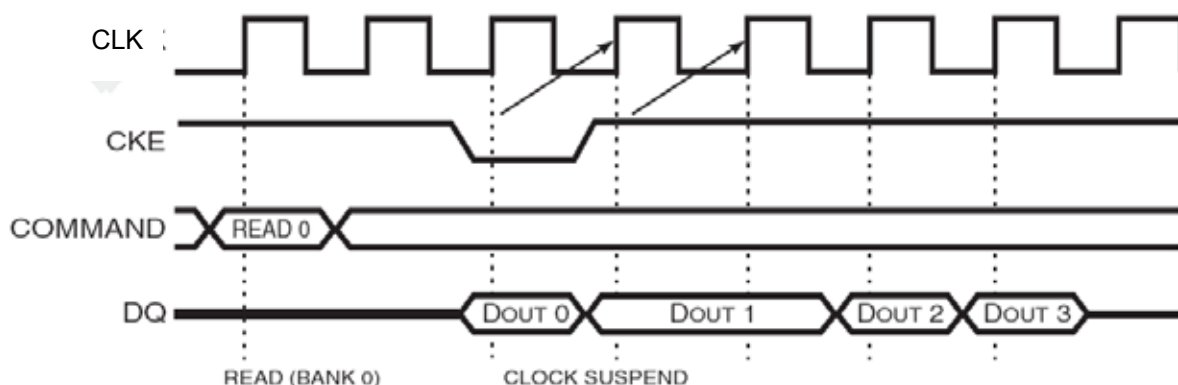


Bank Active to Bank Active for the different bank

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**Clock Suspend**

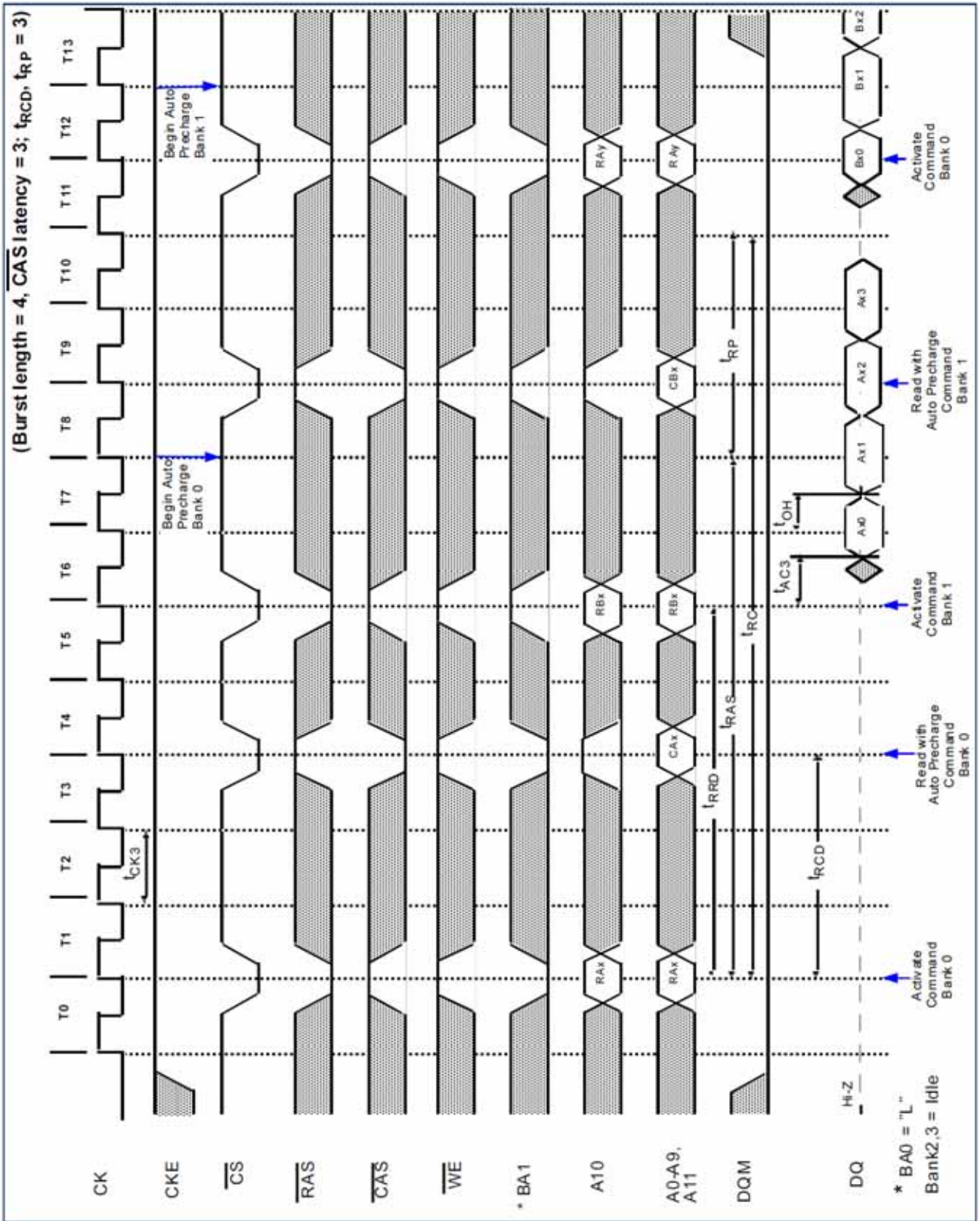
When the CKE pin is dropped from HIGH to LOW during a read or write cycle, the SDRAM enters clock suspend mode on the next CLK rising edge. This command reduced the device power dissipated by stopping the device internal clock. Clock suspend mode continues as long as the CKE pin remains low. In this state, all inputs other than CKE pin are invalid and no other commands can be executed. Also, the device internal states are maintained. When the CKE pin goes from LOW to HIGH clock suspend mode is terminated on the next CLK rising edge and device operation resumes. The next command cannot be executed until the recovery period ( $t_{CKA}$ ) has elapsed. Since this command differs from Self Refresh command described previously in that the refresh operation is no performed automatically internally, the refresh operation must be performed within in the refresh period ( $t_{REF}$ ). Thus the maximum time that clock suspend mode can be held is just under the refresh cycle time.



**Clock Suspend (Burst Length = 4,  $\overline{CAS}$  Latency = 2)**

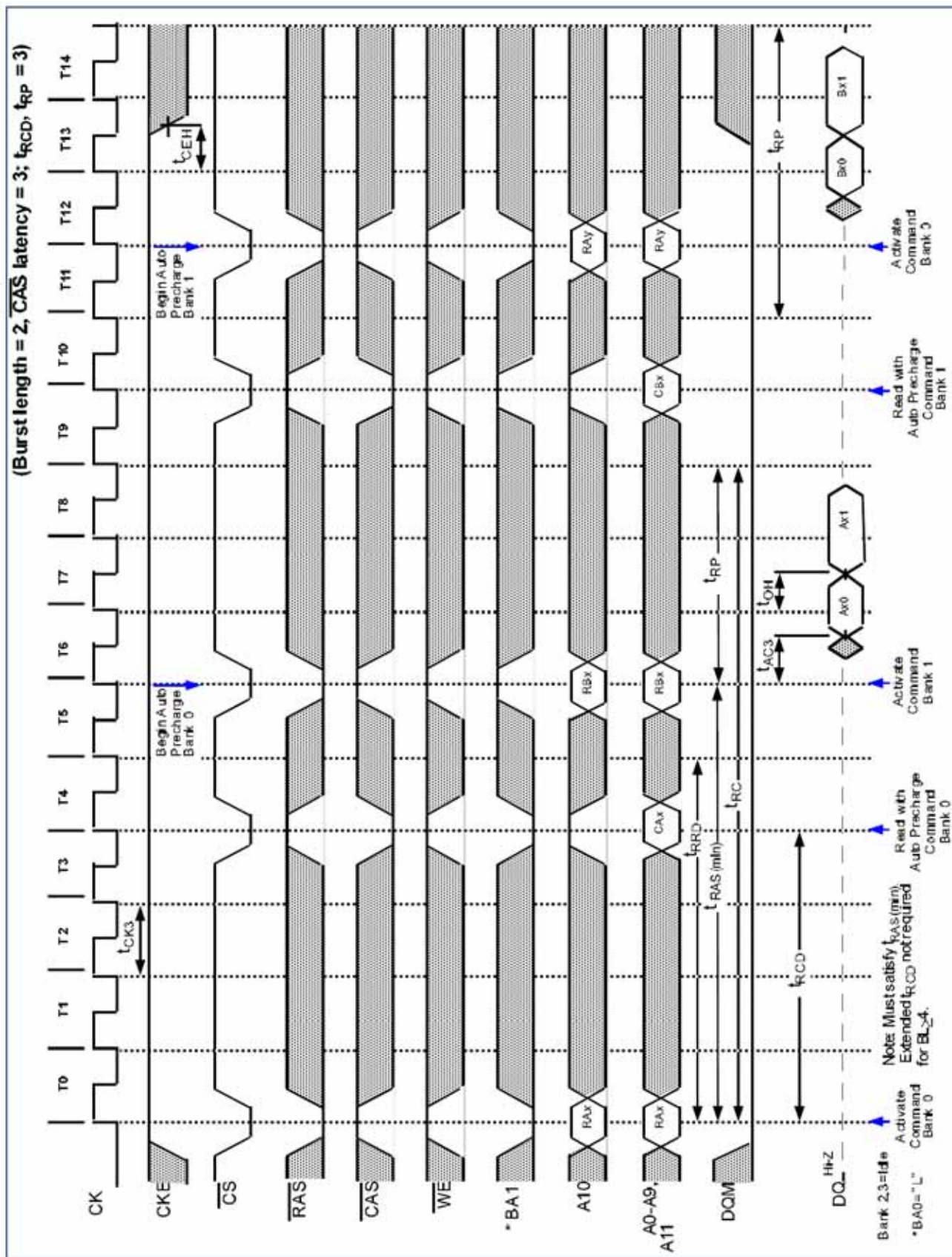


AC Parameters for Read Timing (3/3/3)



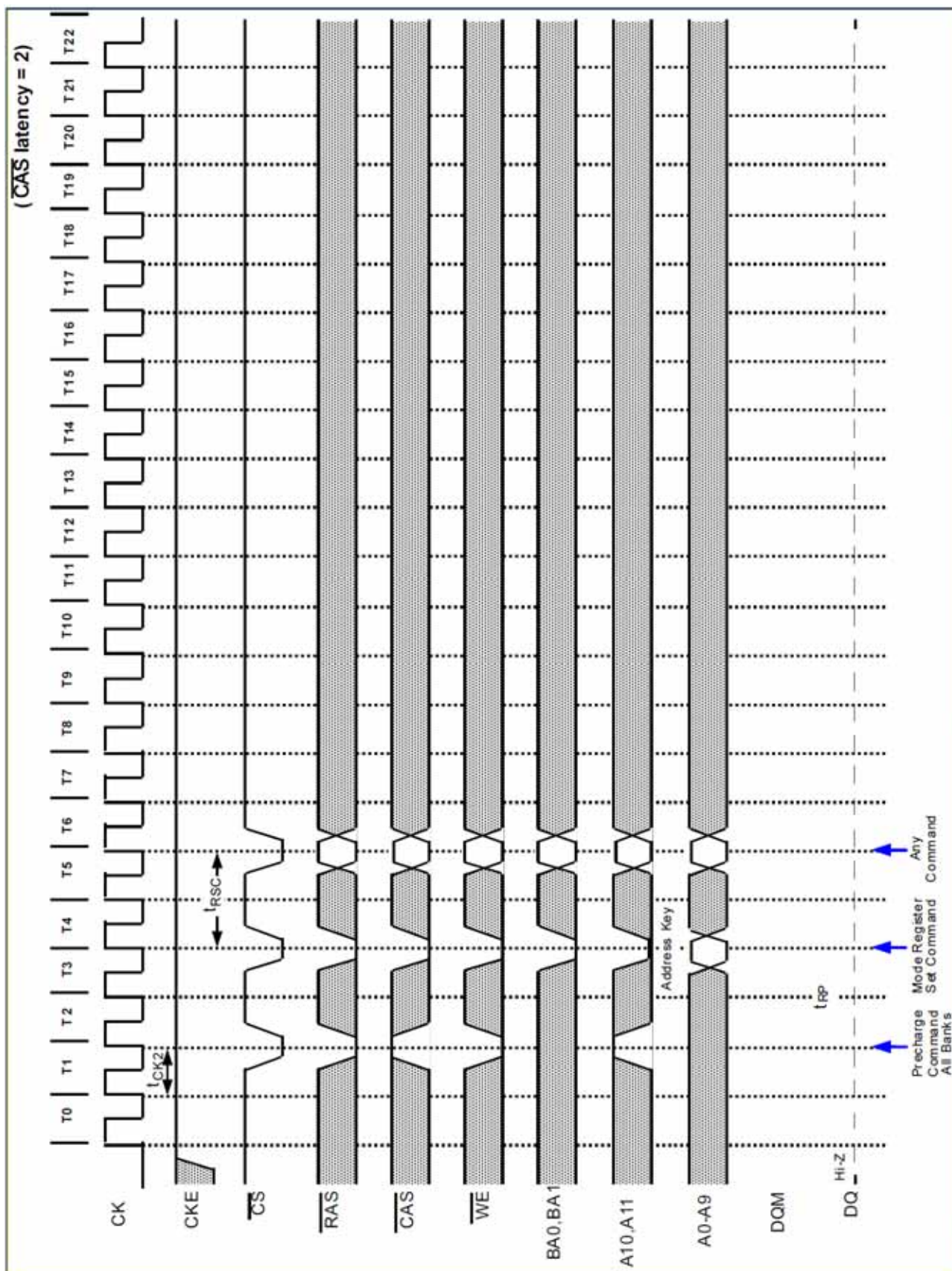
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AC Parameters for Read Timing (3/3/3)

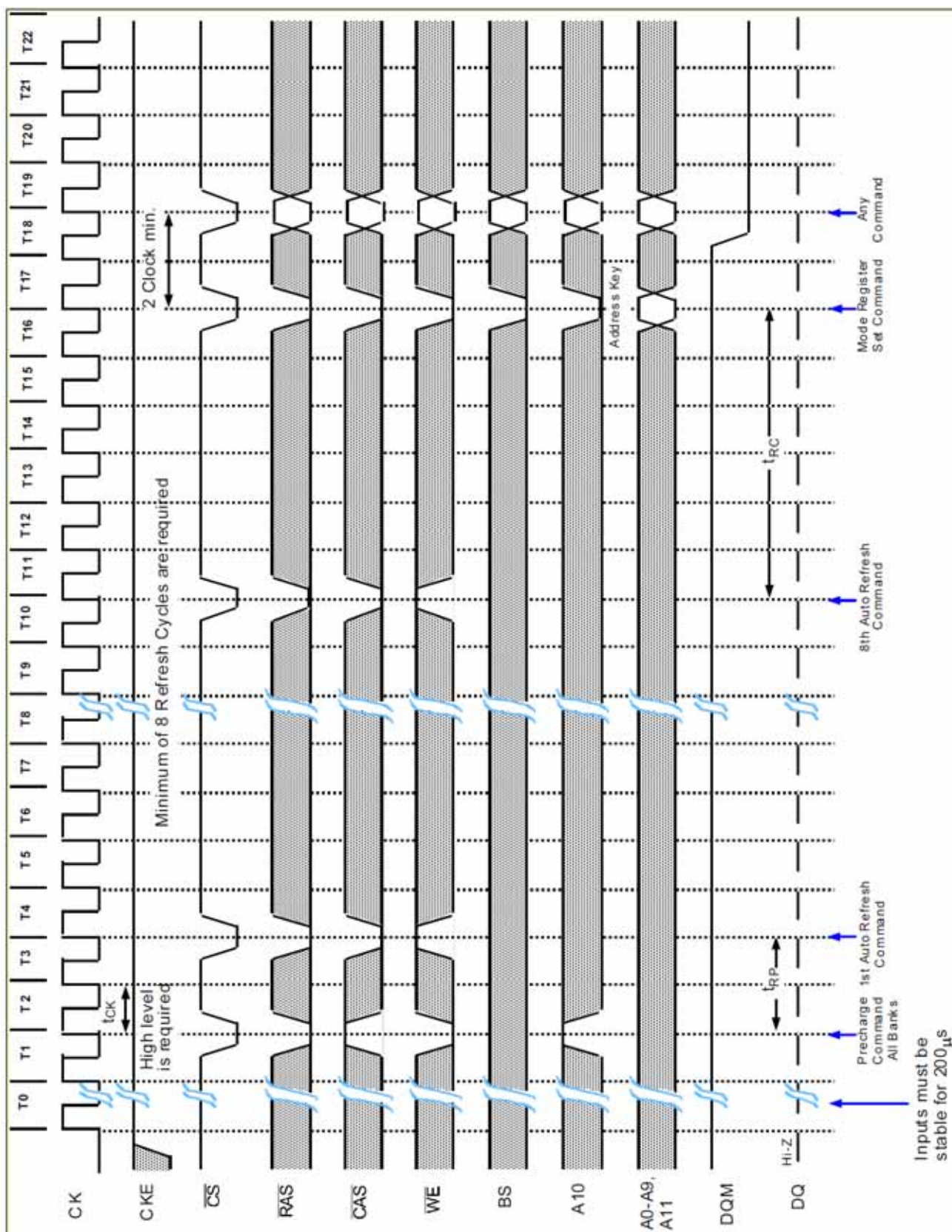




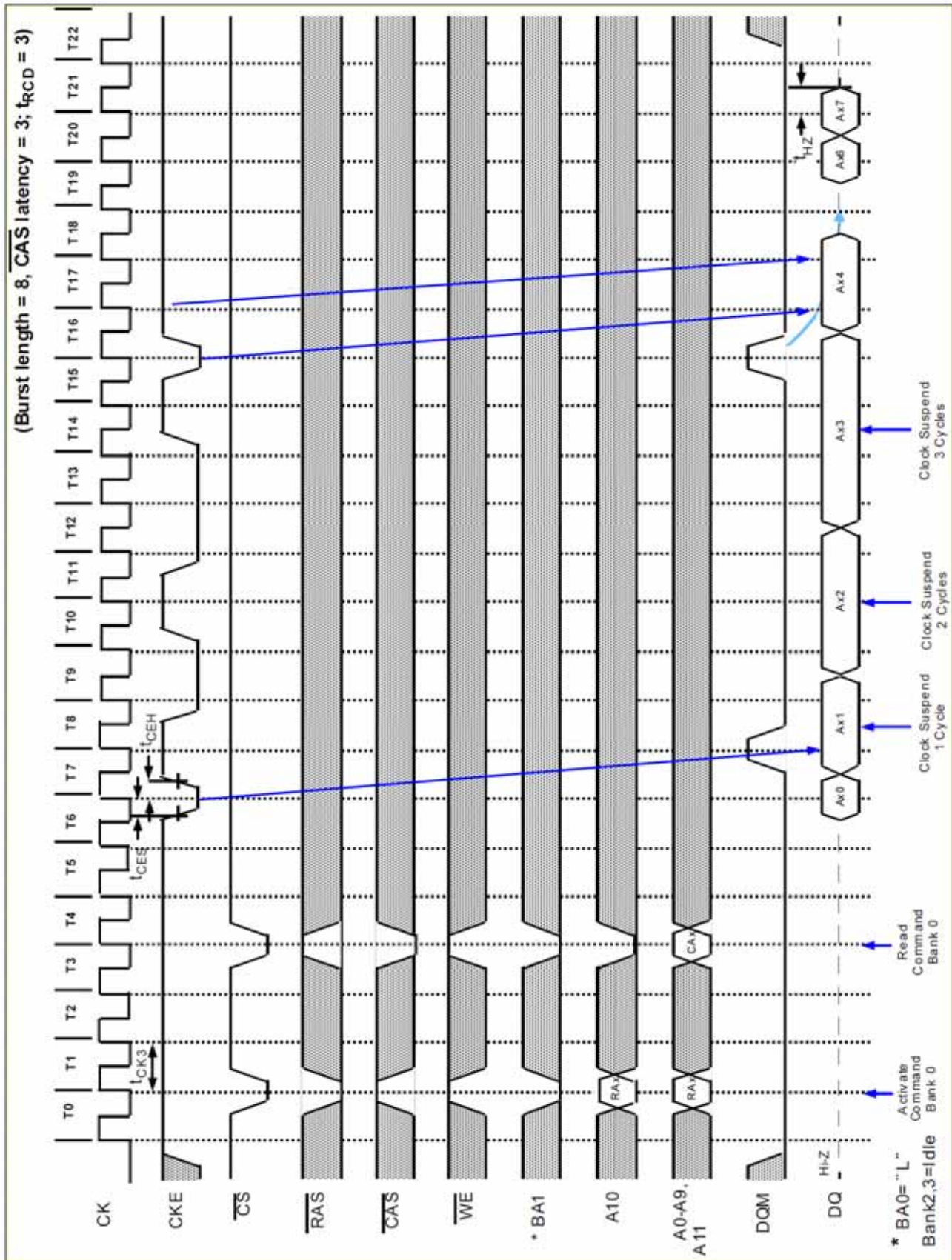
Mode Register Set



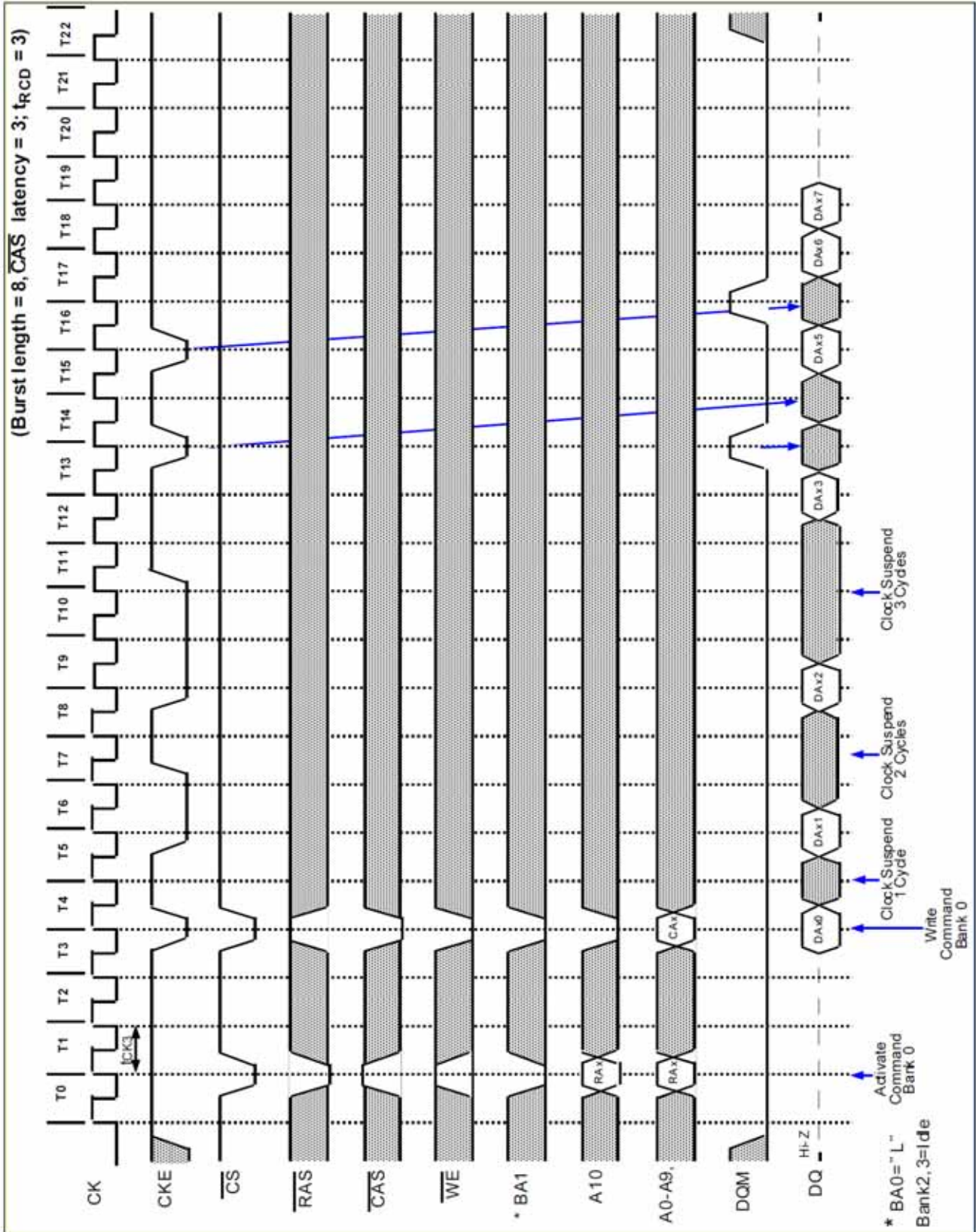
Power-On Sequence and Auto Refresh (CBR)



Clock Suspension / DQ during Burst Read

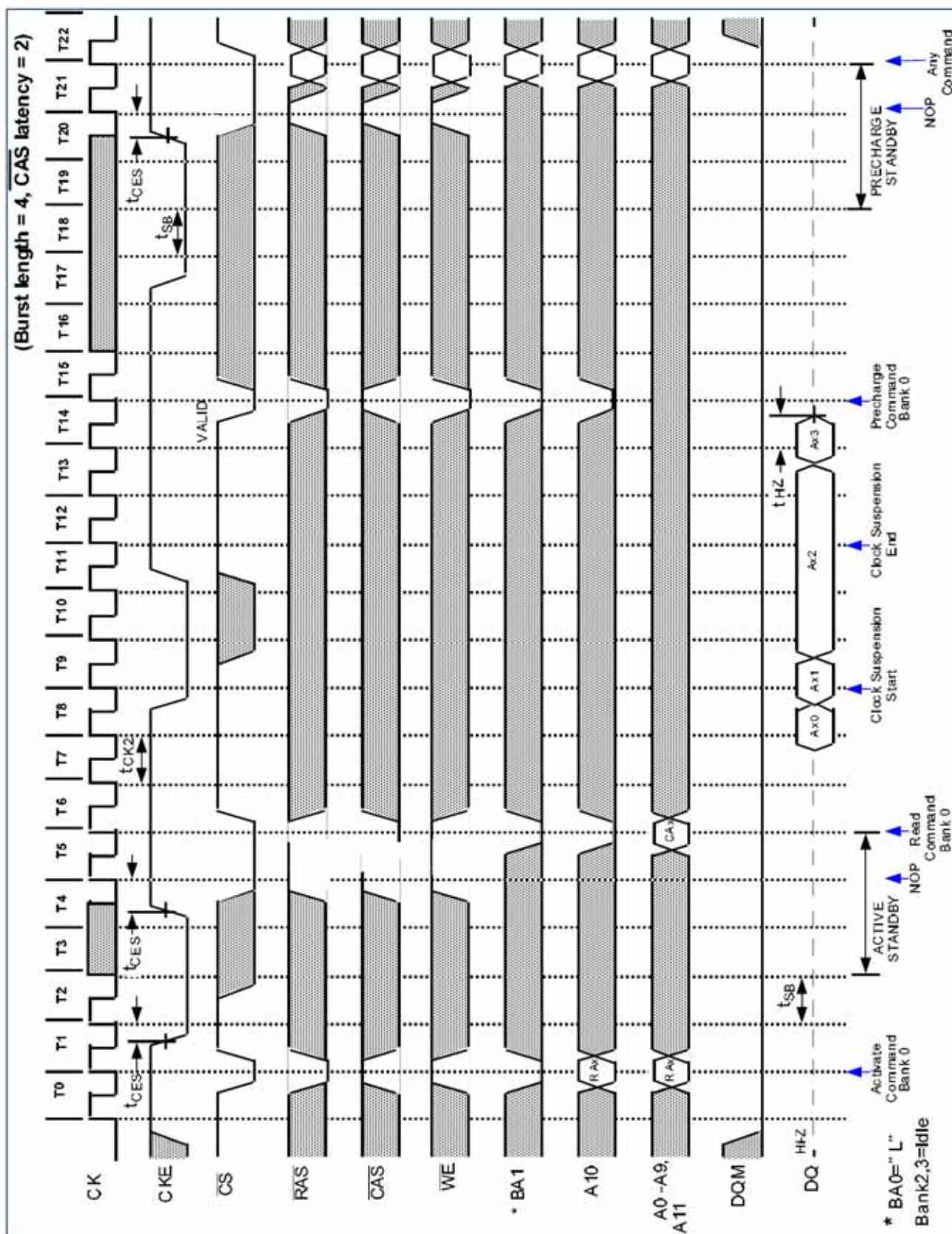


Clock Suspension / DQM during Burst Write

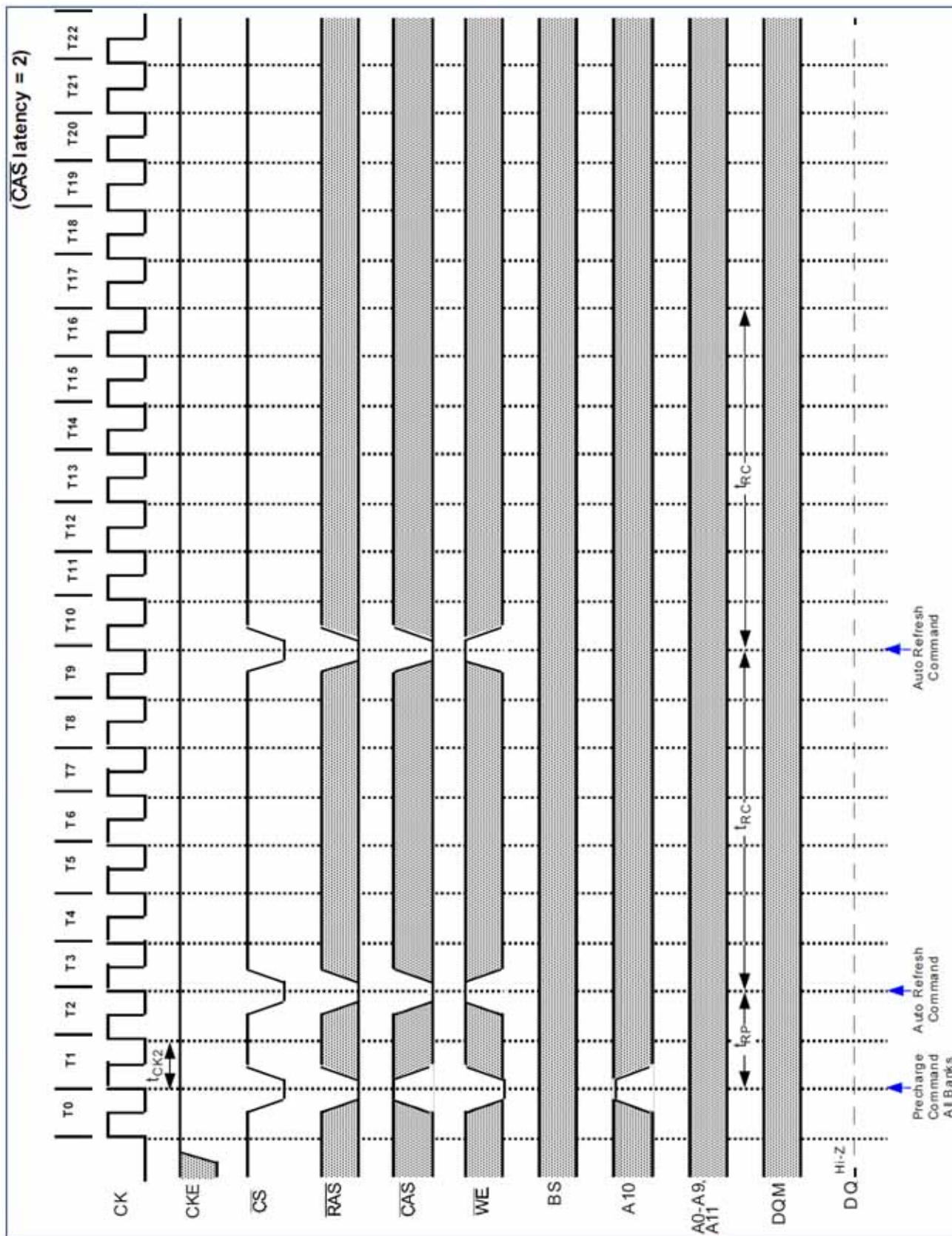




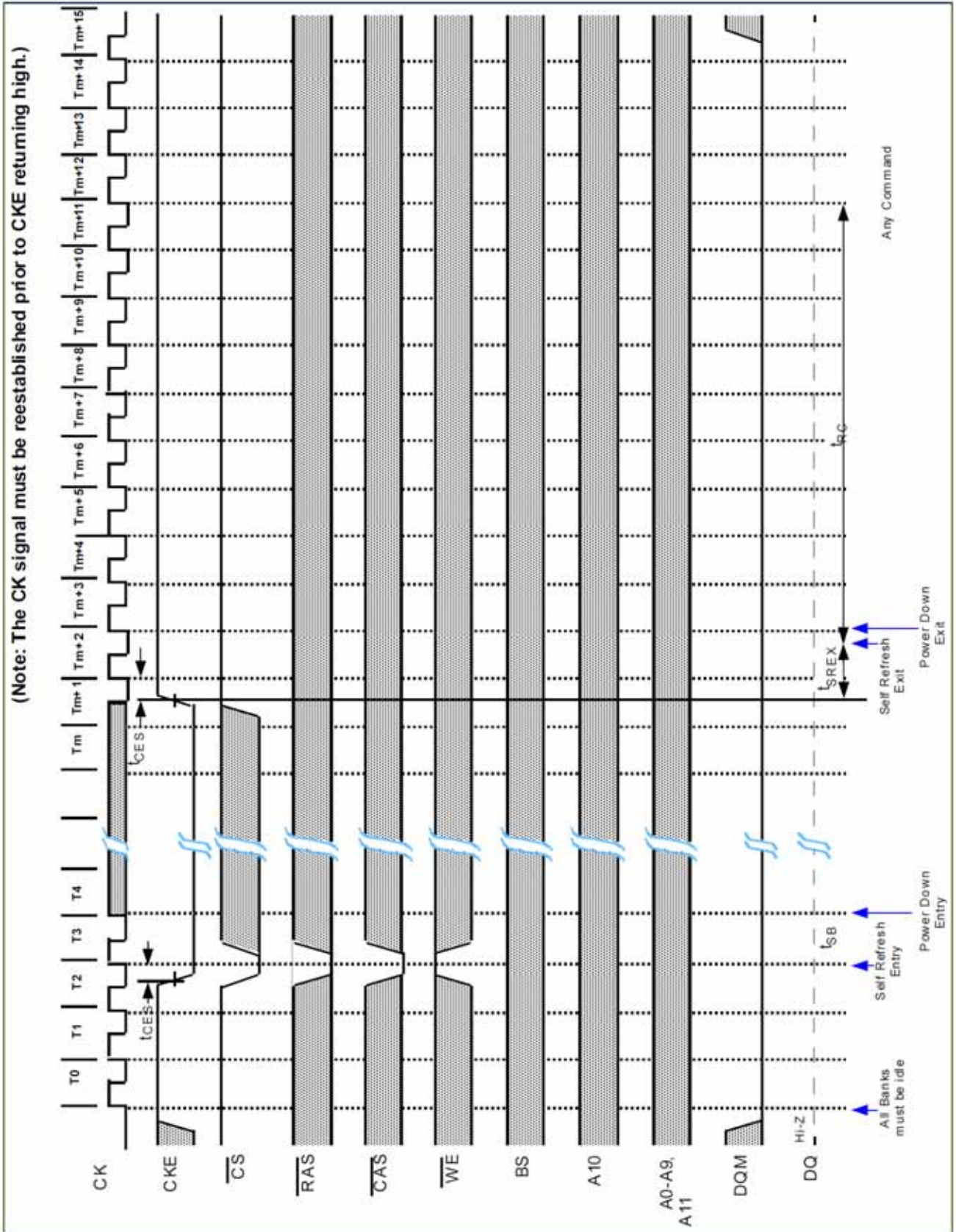
Power Down Mode and Clock Suspend



Auto Refresh (CBR)

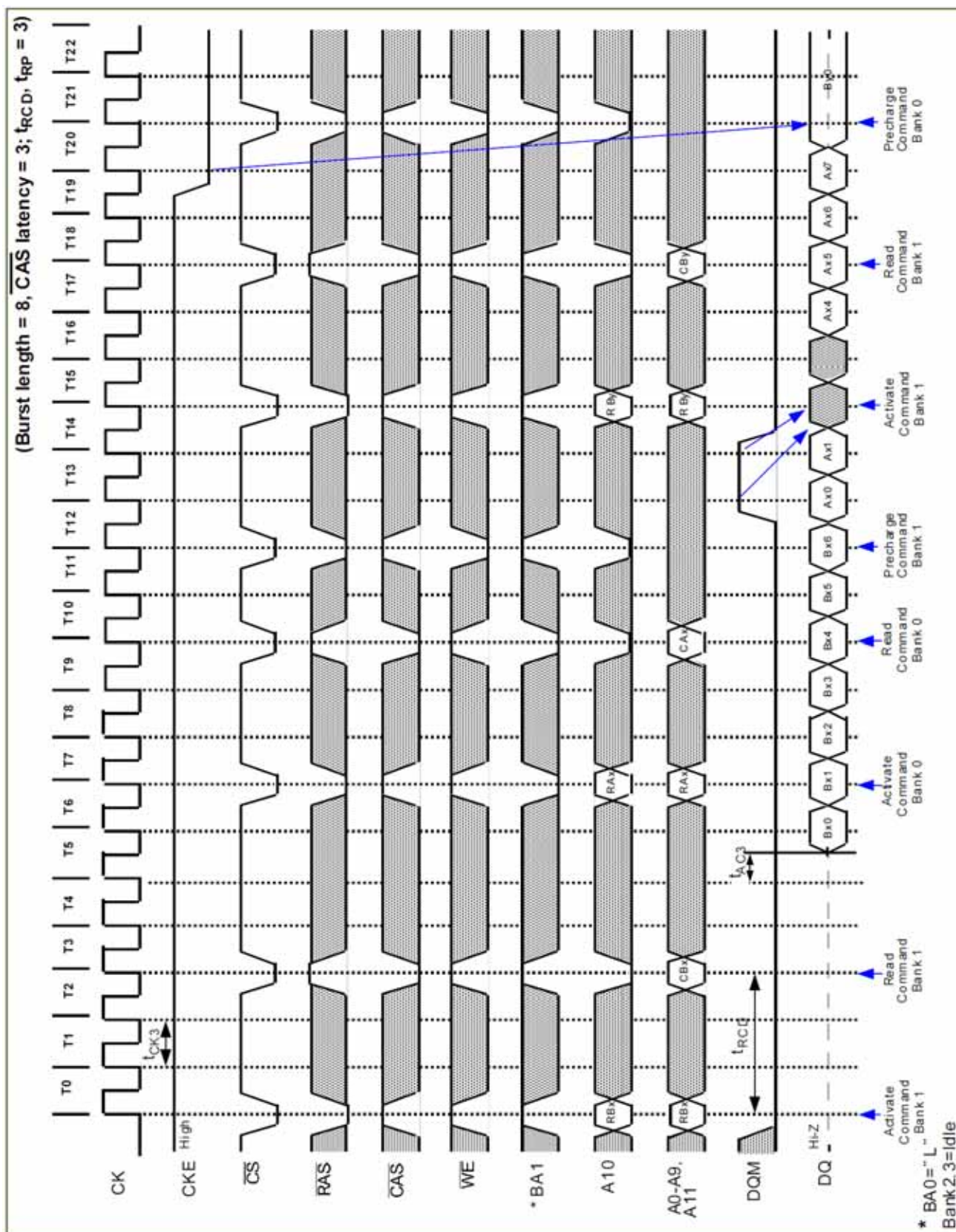


Self Refresh (Entry and Exit)



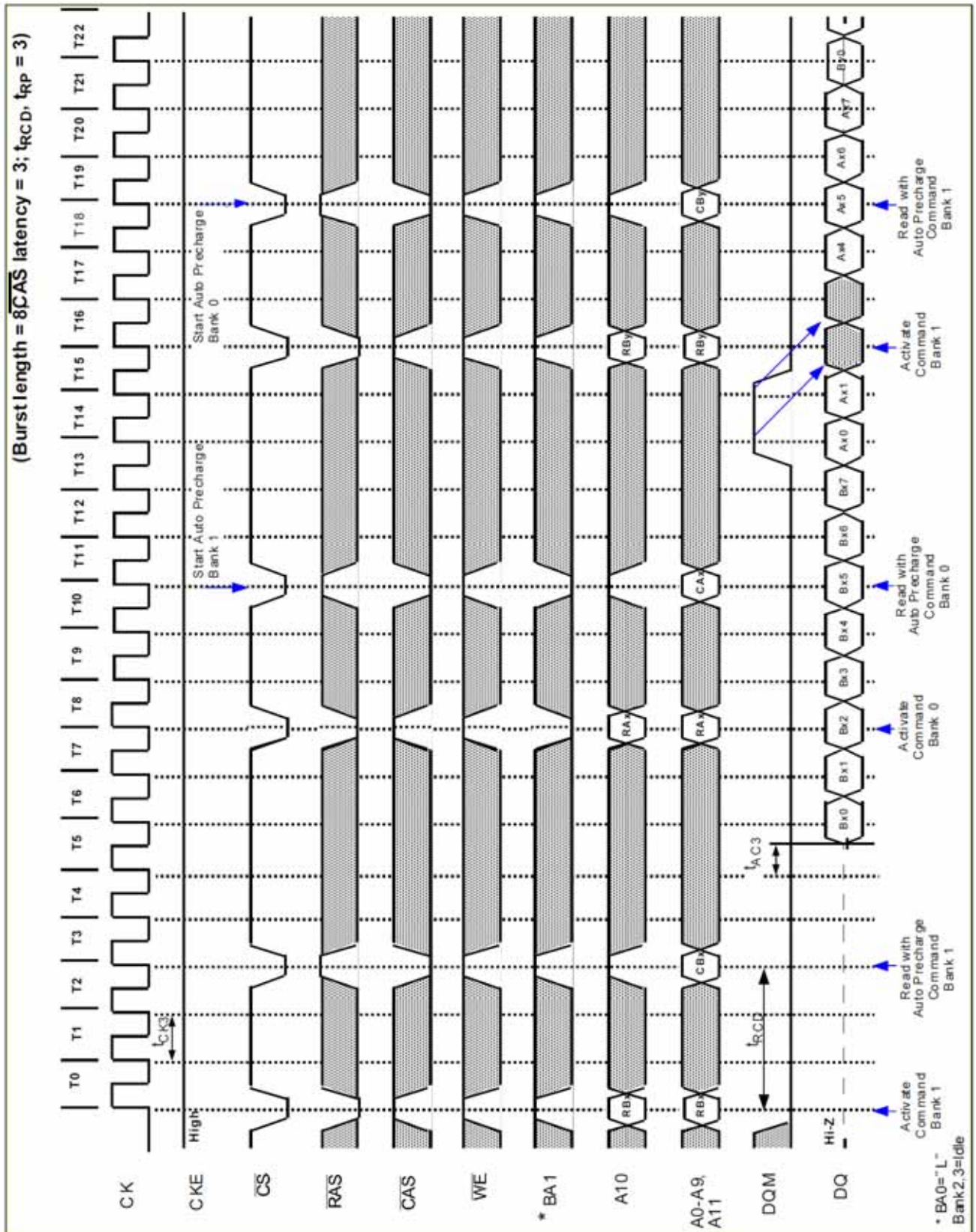


Random Row Read (Interleaving Banks) with Precharge



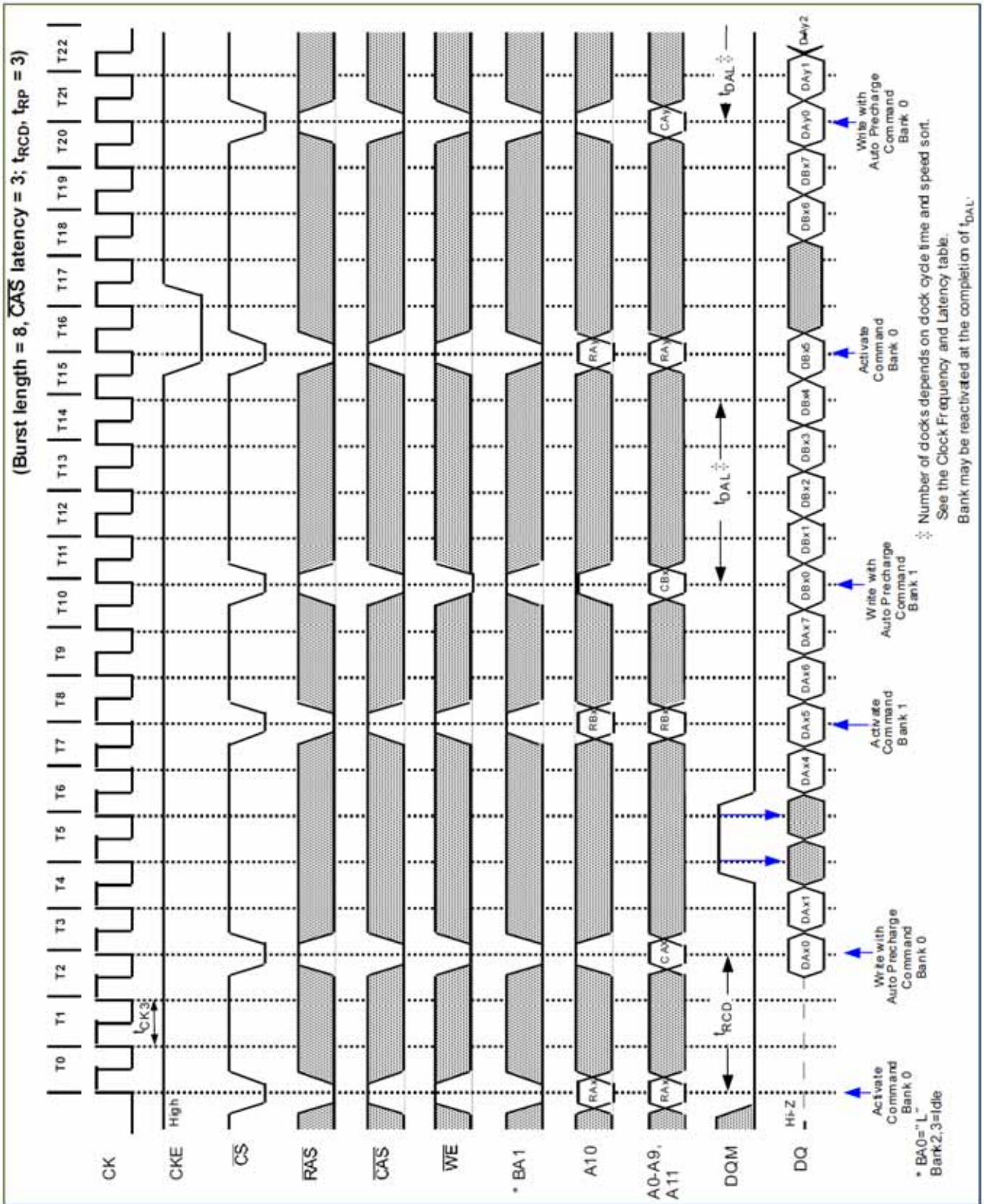
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Random Row Read (Interleaving Banks) with Auto-Precharge

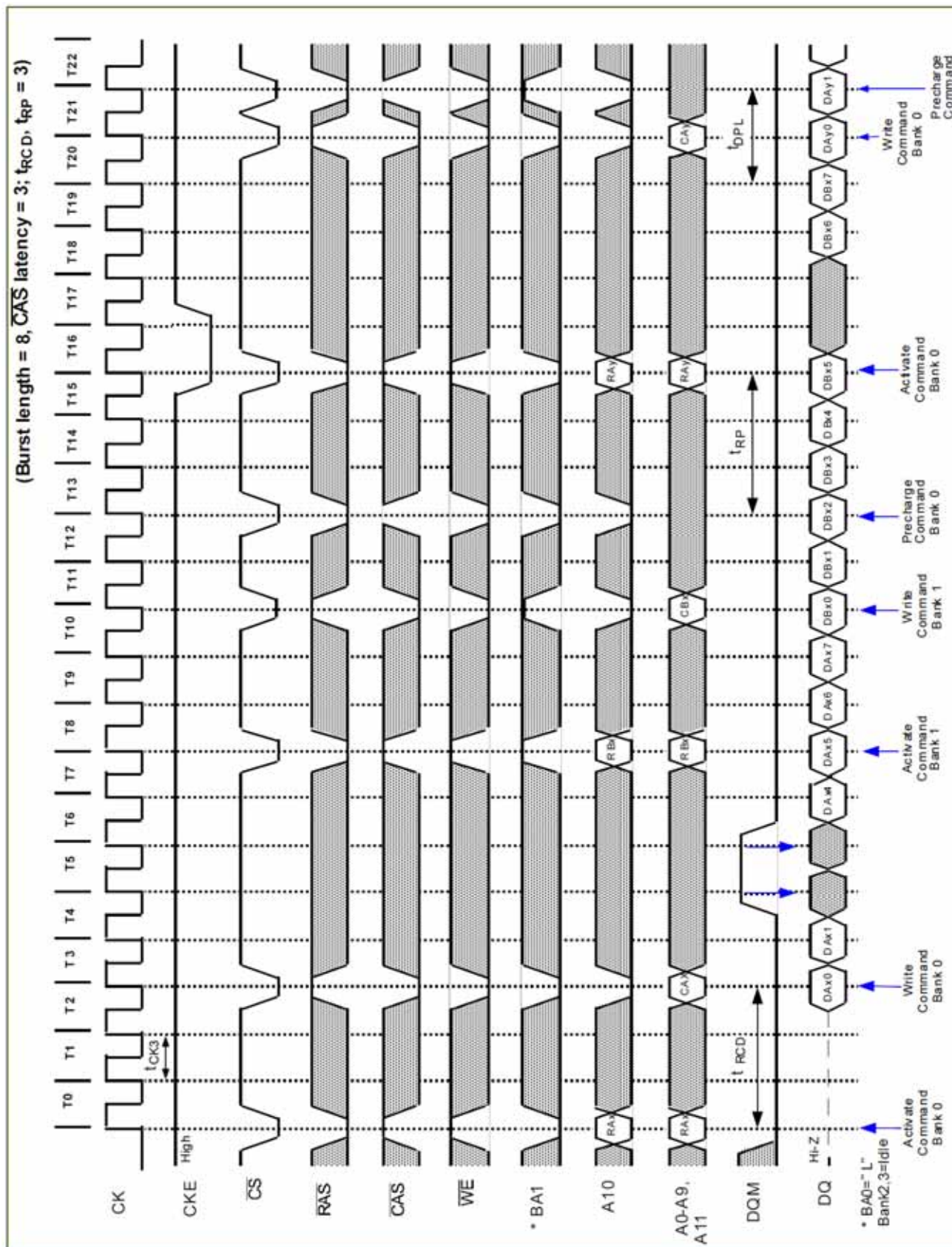


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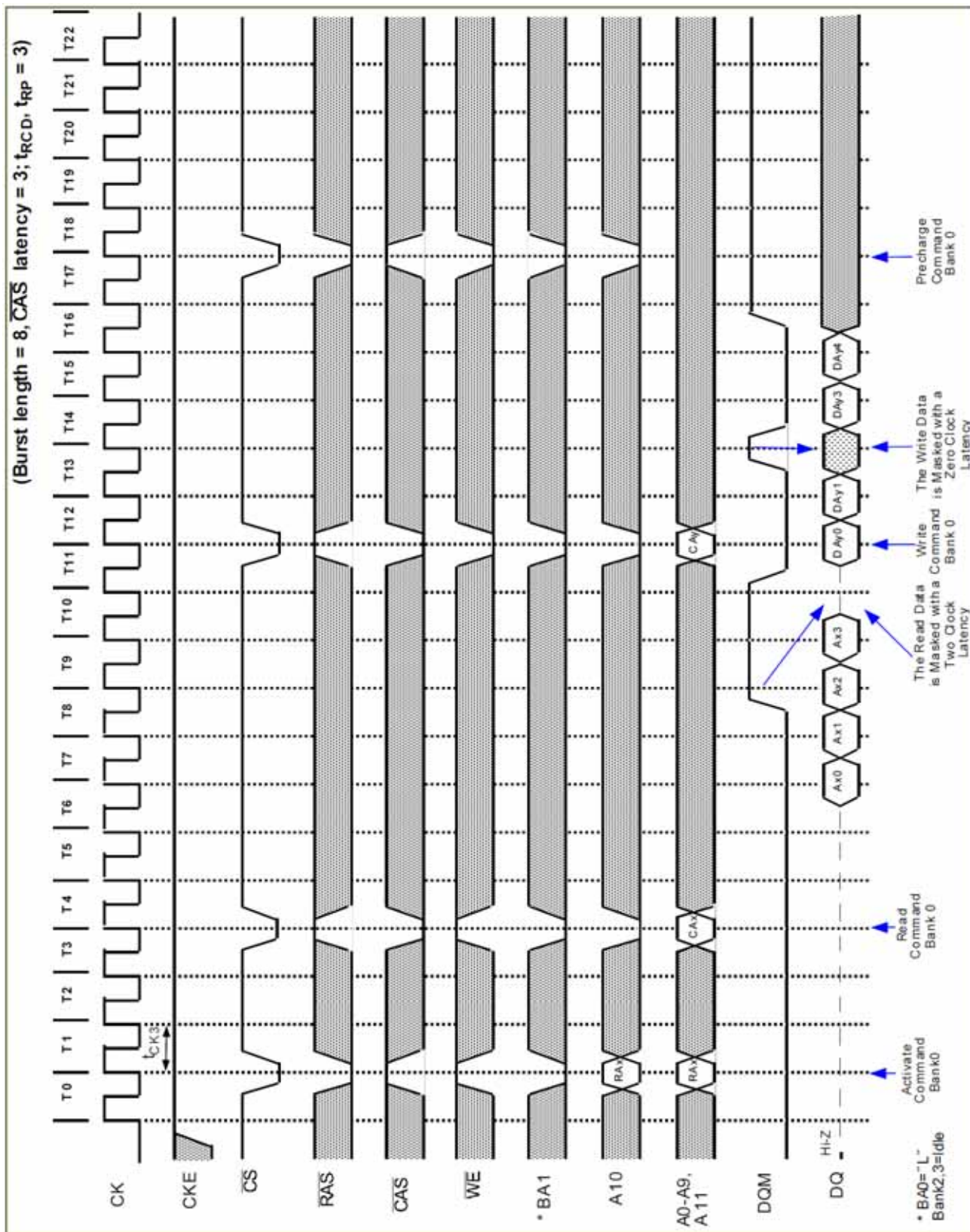
Random Row Write (Interleaving Banks) with Auto-Precharge



Random Row Write (Interleaving Banks) with Precharge

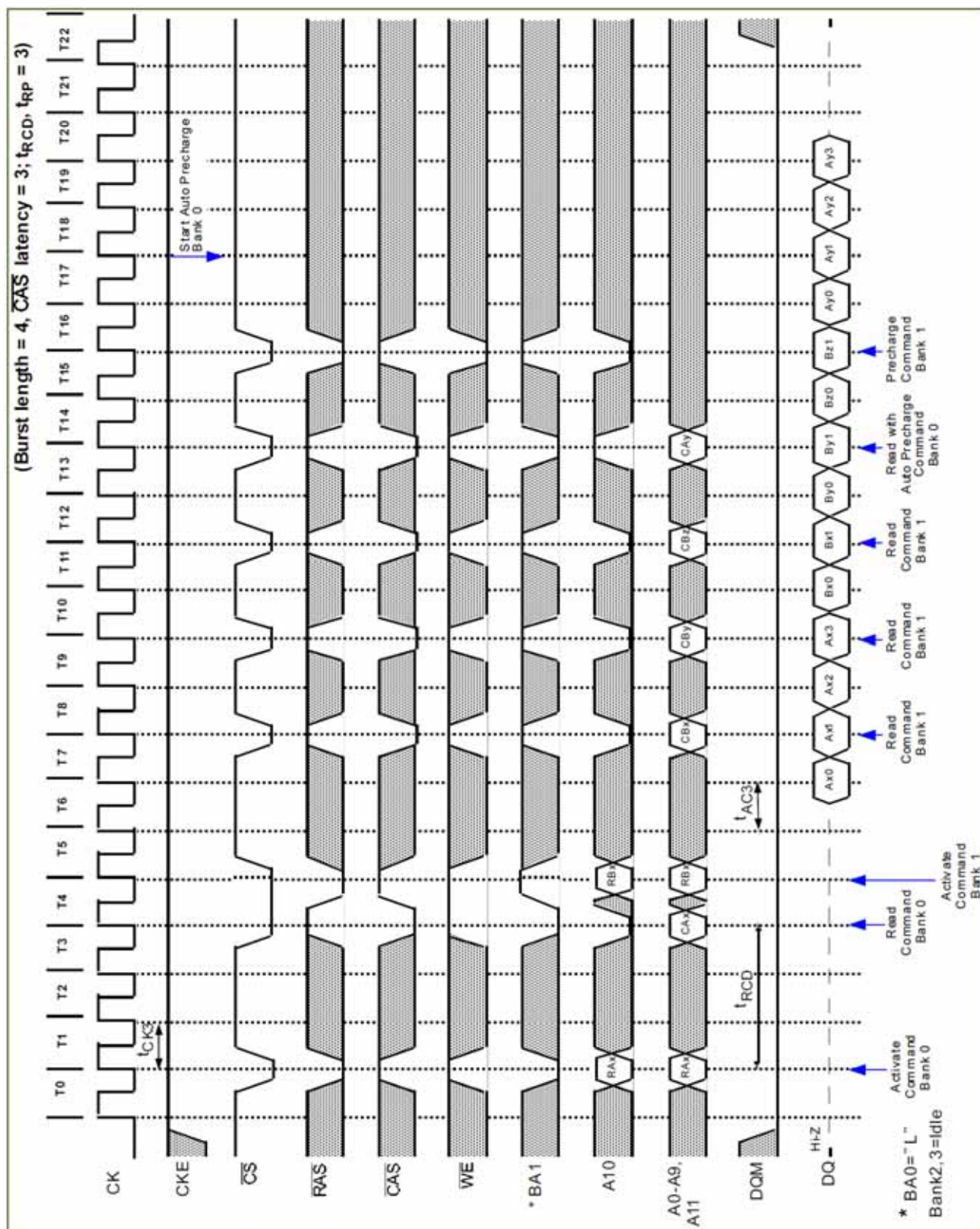


Read / Write Cycle



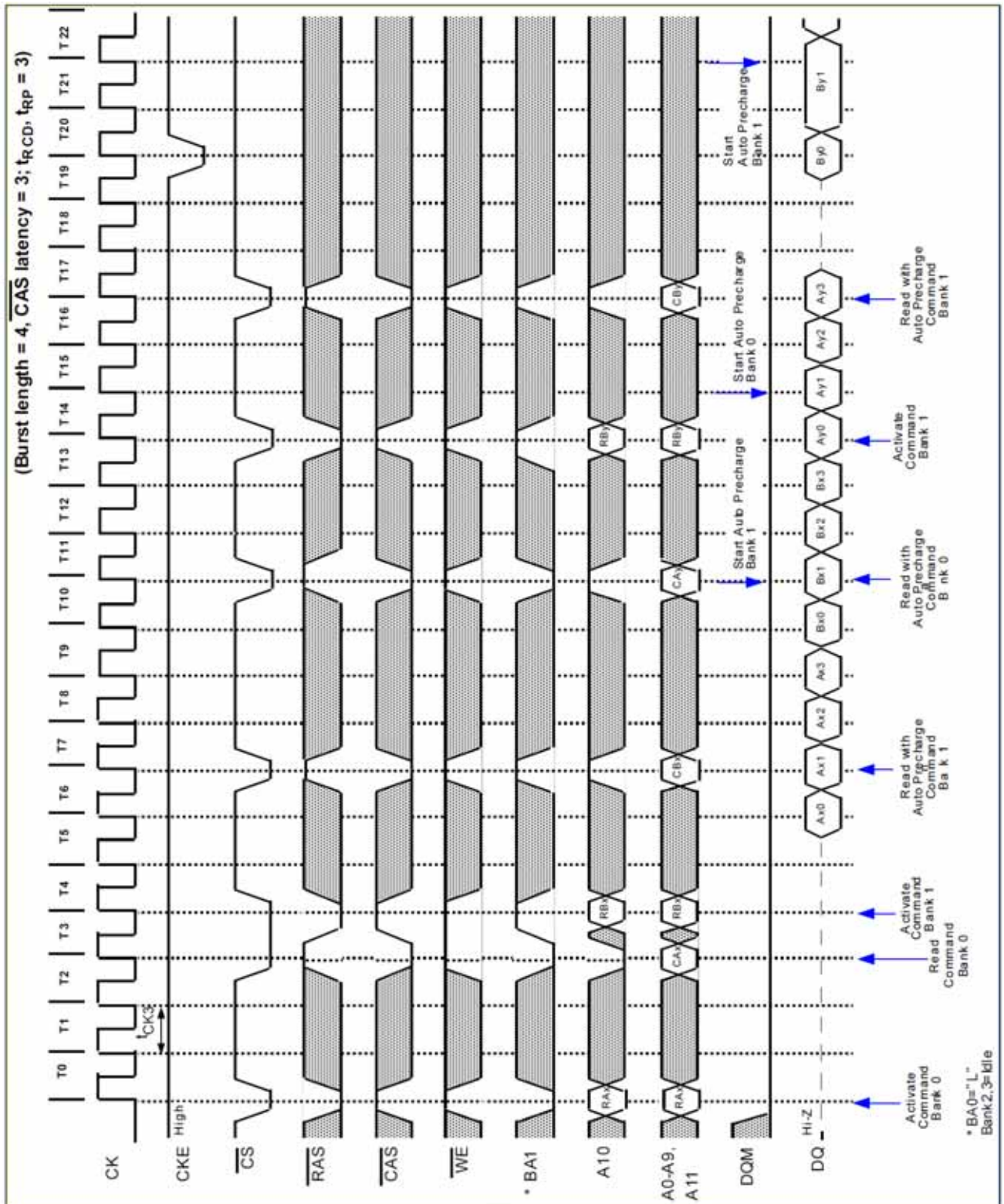
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Interleaved Column Read Cycle



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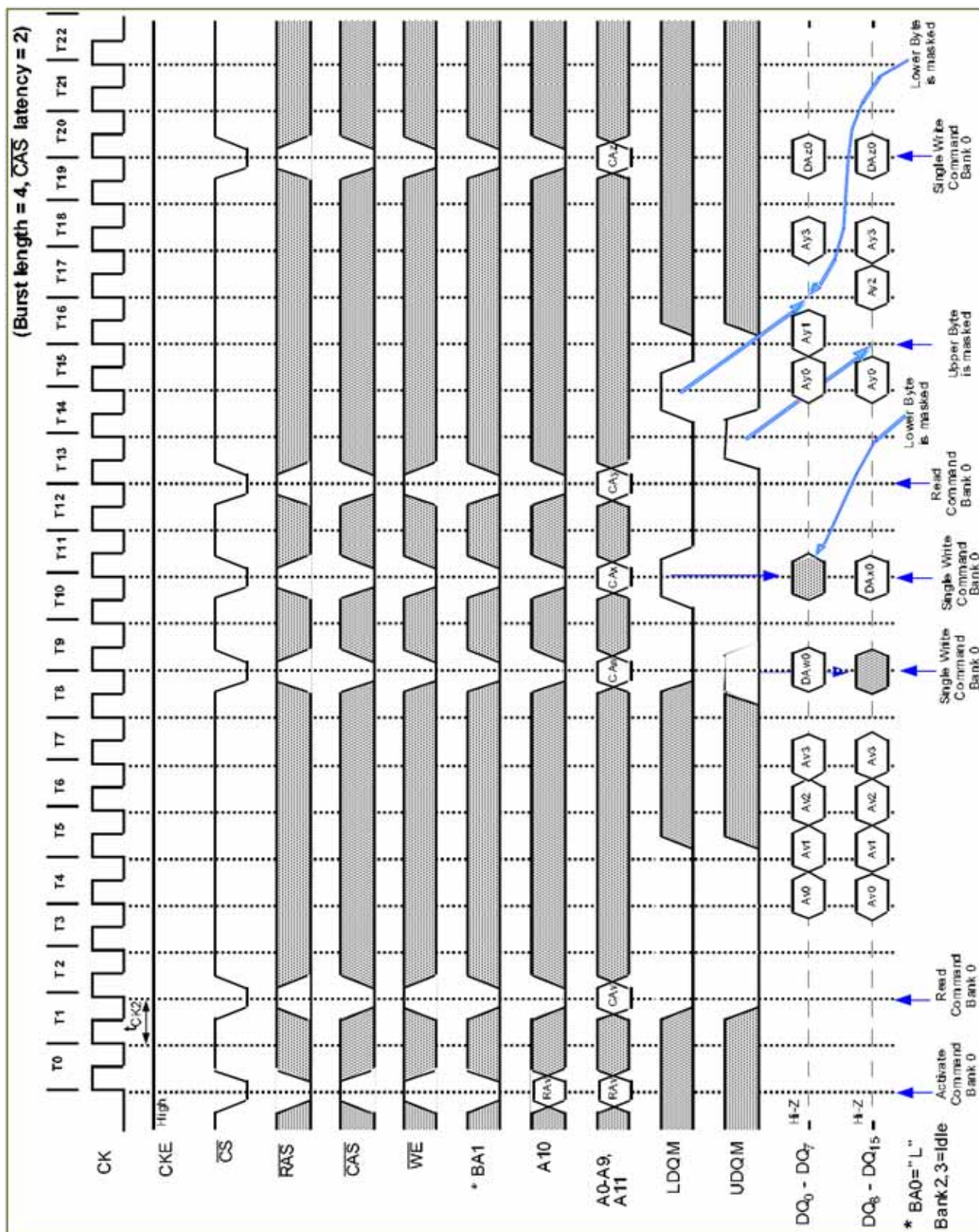
Auto Precharge after Read Burst



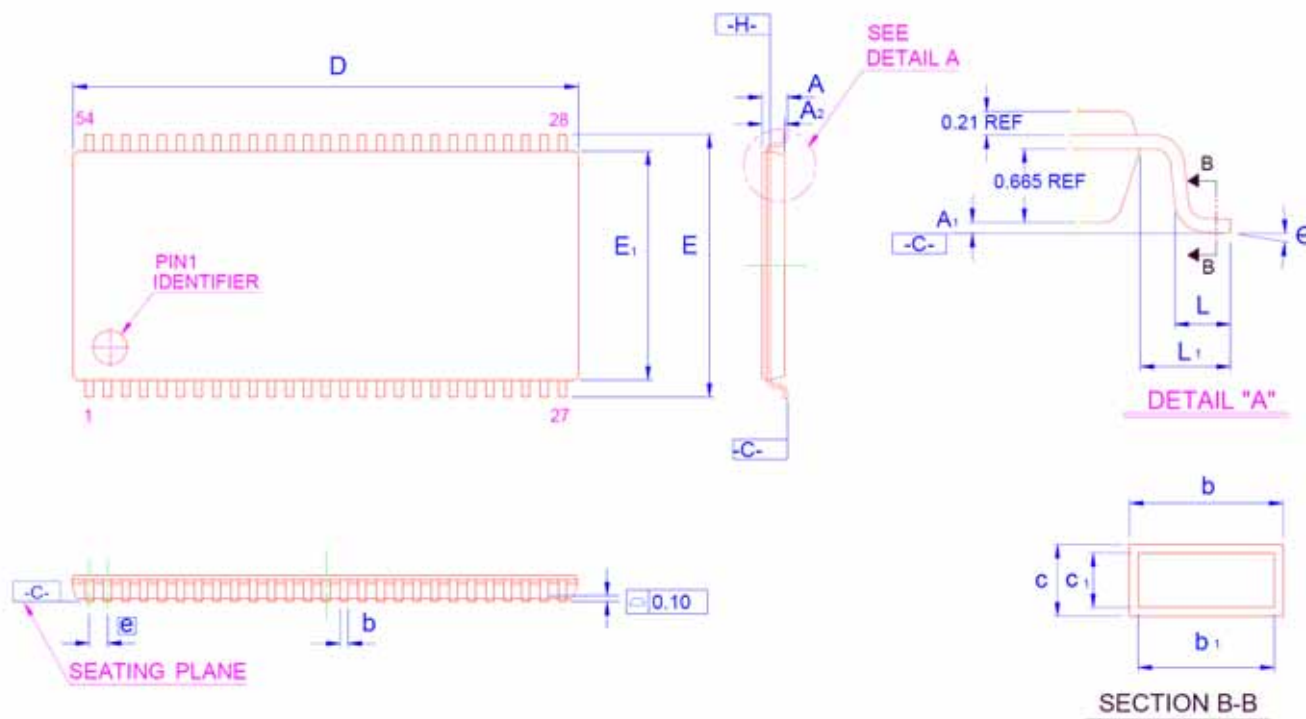




Burst Read and Single Write Operation



Package Information



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	-	-	1.20	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.25	-	0.45	0.010	-	0.018
b1	0.25	0.35	0.40	0.010	0.014	0.016
c	0.12	-	0.21	0.005	-	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.031 BSC		
$\theta$	0°	-	10°	0°	-	10°

**Revision Log**

Rev	Date	Modification
1.0	Mar. 2011	Official Release
1.1	Jul. 2011	Revised P/N Typo

**64Mb SDR SDRAM**

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