2 x 4K x 16 Cache-Data Static RAM L7C183/184

T-46-23-12

2

FEATURES

- 2 × 4K × 16 or 8K × 16 Cache-Data Static RAM with Direct Map or Two-Way Set Associative
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 20 ns worst-case
- Low Power Operation
  Active: 700 mW typical at 45 ns
  Standby: 75 mW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with Cypress CY7C183/184
- Package Styles Available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 48-pin Ceramic LCC
  - 52-pin Plastic LCC

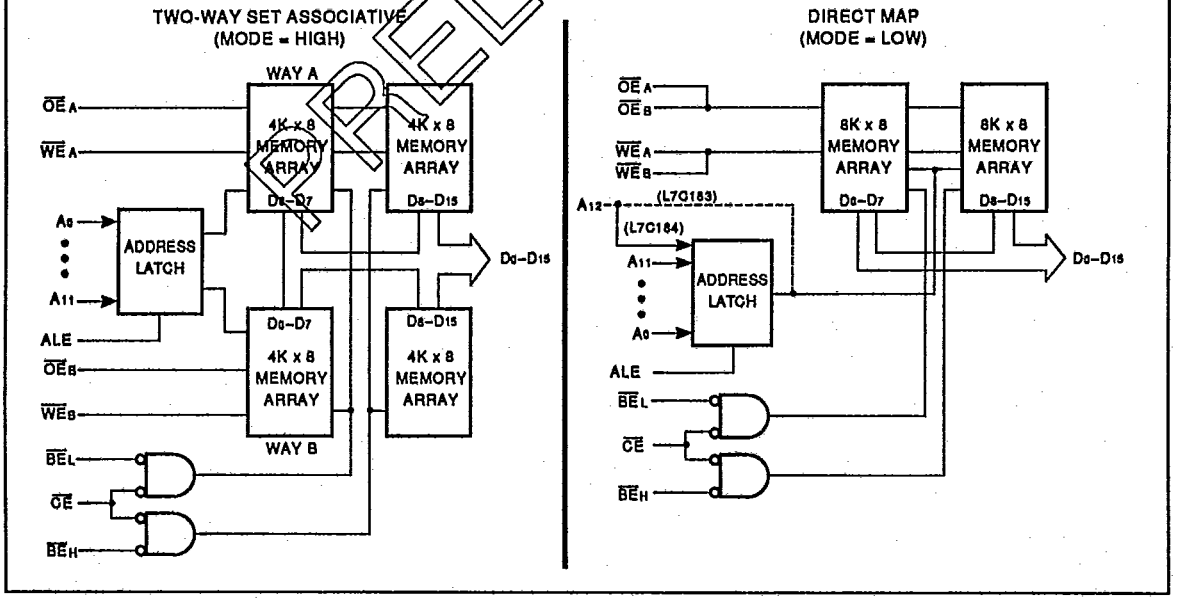
DESCRIPTION

The L7C183 and L7C184 are high-performance, low-power CMOS static RAMs which contain 128K bits organized into either two, two-way set associative blocks of 4K × 16 RAM, or one directly mapped 8K × 16-bit RAM.

The L7C183 and L7C184 are designed specifically for use with the Intel 82385 Cache Controller. Addresses are latched on the falling edge of the Address Latch Enable (ALE) signal. When ALE is HIGH, the latch is transparent. The L7C183 has all address bits latched by the ALE signal except A12, which is unlatched. A12, which bypasses the latch, has a faster access time. All address bits are latched by the ALE signal in the L7C184. The mode pin controls whether the L7C183 and L7C184 are configured as direct mapped 8K × 16 or two-way set associative 2 × 4K × 16 RAMs. When mode is HIGH, the circuits are placed in the two-way mode. In the two-way mode, the upper address bit, A12 is a "don't care", and should be externally wired to ground. When mode is LOW, the circuits are placed in the direct mapped mode.

Writing is accomplished in the two-way mode by taking $\overline{CE}$ LOW and by inserting the respective $\overline{BE}$x and $\overline{WE}$x signals LOW. $\overline{BE}_L$ enables bits D0–D7 while $\overline{BE}_H$ enables bits D8–D15. $\overline{WE}_A$ enables cache bank A, and $\overline{WE}_B$ enables cache bank B to receive whatever data resides on the data bus. $\overline{OE}_A$ and $\overline{OE}_B$ similarly enable cache banks A and B, respectively, to drive the data bus. Writing is accomplished in the direct mode by tying $\overline{WE}_A$ and $\overline{WE}_B$ together externally, and using A12 to determine which 4K × 16 memory bank is selected.

L7C183/184 Block Diagram



Reading is accomplished in the two-way mode by taking $\overline{CE}$ LOW, inserting the respective $\overline{OE}$x and $\overline{BE}$x signals LOW, and the respective $\overline{WE}$x signal HIGH. The contents of the memory location specified on the address pins which appear on the 16 outputs. Activation of $\overline{OE}_A$ and $\overline{OE}_B$ simultaneously will cause both banks to be deselected. Reading is accomplished in the direct mode by tying $\overline{OE}_A$ and $\overline{OE}_B$ together externally. A_{12} will determine which 4K x 16 memory bank is enabled.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 700 mW (typical) at 45 ns.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read accesses which are longer than the minimum access time, or when the memory is deselected and addresses do not change (stable). In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The memory typically consumes only 9 mW at 3 V, allowing effective battery backup operation.

Latchup and static discharge protection are provided on-chip. The L7C183 and L7C184 can withstand an injection current of up to 200 mA on any pin without damage.

Truth Table — Two-Way Mode (MODE = HIGH)

$\overline{CE}$	$\overline{BE}_L$	$\overline{BE}_H$	$\overline{OE}_A$	$\overline{OE}_B$	$\overline{WE}_A$	$\overline{WE}_B$	Operation	
H	X	X	X	X	X	X	Outputs Hi-Z, Write Disabled	
L	H	H	X	X	X	X	Outputs Hi-Z, Write Disabled	
X	X	X	H	H	X	X	Outputs HI-Z	
X	X	X	L	L	X	X	Outputs Hi-Z	
L	L	H	L	H	H	H	Read I/O_0–I/O_7	Way A
L	L	H	H	L	H	H	Read I/O_0–I/O_7	Way B
L	H	L	L	H	H	H	Read I/O_8–I/O_{15}	Way A
L	H	L	H	L	H	H	Read I/O_8–I/O_{15}	Way B
L	L	L	L	H	H	H	Read I/O_0–I/O_{15}	Way A
L	L	L	H	L	H	H	Read I/O_0–I/O_{15}	Way B
L	L	H	X	X	L	H	Write I/O_0–I/O_7	Way A
L	L	H	X	X	H	L	Write I/O_0–I/O_7	Way B
L	H	L	X	X	L	H	Write I/O_8–I/O_{15}	Way A
L	H	L	X	X	H	L	Write I/O_8–I/O_{15}	Way B
L	L	L	X	X	L	H	Write I/O_0–I/O_{15}	Way A
L	L	L	X	X	H	L	Write I/O_0–I/O_{15}	Way B
L	L	H	X	X	L	L	Write I/O_0–I/O_7	Way A & B
L	H	L	X	X	L	L	Write I/O_8–I/O_{15}	Way A & B
L	L	L	X	X	L	L	Write I/O_0–I/O_{15}	Way A & B

Truth Table — Direct Mode (MODE = LOW)

$\overline{CE}$	$\overline{BE}_L$	$\overline{BE}_H$	$\overline{OE}_A$	$\overline{OE}_B$	$\overline{WE}_A$	$\overline{WE}_B$	Operation
H	X	X	X	X	X	X	Outputs Hi-Z, Write Disabled
L	H	H	X	X	X	X	Outputs Hi-Z, Write Disabled
X	X	X	H	H	X	X	Outputs HI-Z
L	L	H	L	L	H	H	Read I/O_0–I/O_7
L	H	L	L	L	H	H	Read I/O_8–I/O_{15}
L	L	L	L	L	H	H	Read I/O_0–I/O_{15}
L	L	H	X	X	L	L	Write I/O_0–I/O_7
L	H	L	X	X	L	L	Write I/O_8–I/O_{15}
L	L	L	X	X	L	L	Write I/O_0–I/O_{15}

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–0.5 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

2

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ Vcc ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ Vcc ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ Vcc ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –1.0 mA, Vcc = Min.	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, Vcc = Min.			0.4	V
V_{IH}	Input High Voltage		2.2		Vcc + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ Vcc	–10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ Vcc, Output Disabled	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, Vcc = Max (Note 4)			–350	mA
I_{CC2}	Vcc Current, Standby	(Note 8)		50	250	µA
I_{CC3}	Vcc Current, DR Mode	Vcc = 3.0 V (Note 9)		3.0	50	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, Vcc = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

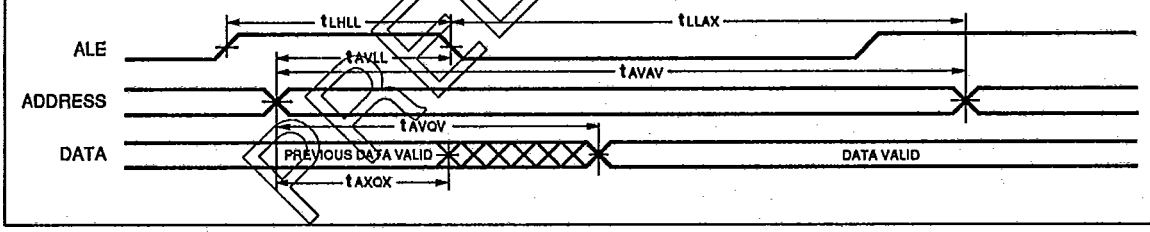
			L7C183/184-				
Symbol	Parameter	Test Condition	45	35	25	20	Unit
I_{CC1}	Vcc Current, Active	(Note 6)	170	220	300	370	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

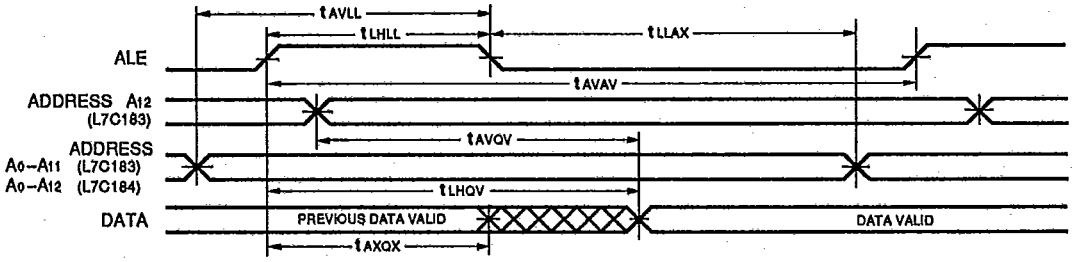
Read Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C183/184- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max
tAVAV	Read Cycle Time	45		35		25		20	
tAVQV	Address Valid to Output Valid, A_0–A_{11} (13, 14)		45		35		25		20
tAVQV	Address Valid to Output Valid, A_{12} (13, 14)		35		25		17		12
tAXQX	Address Change to Output Change	3		3		3		3	
tLHQV	ALE High to Output Valid		45		35		25		20
tCLQV	Chip Enable Low to Output Valid (13, 15)		20		15		12		10
tBLQV	Byte Enable Low to Output Valid (13, 15)		20		15		12		10
tOLQV	Output Enable Low to Output Valid (13, 15, 20)		16		14		10		10
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3	
tBLQZ	Byte Enable Low to Output Low Z (20, 21)	3		3		3		3	
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0	
tCHQZ	Chip Enable High to Output High Z (20, 21)		12		10		8		8
tBHQZ	Byte Enable High to Output High Z (20, 21)		12		10		8		8
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		8
tLHLL	ALE Pulse Width		12		10		8		8
tAVLL	Address Valid to ALE Low	6		6		4		4	
tLLAX	ALE Low to Address Change	4		4		4		4	
tOLOH	$\overline{OEA}$, $\overline{OEB}$ Overlap Time (20)	0		0		0		0	
tPU	$\overline{CE}$, $\overline{BEx}$ Low to Power Up (10, 19)	0		0		0		0	
tPD	Power Up to Power Down (10, 19)		45		35		25		20
tCHVL	Chip Enable High to Output Retention (10)	0		0		0		0	

Read Cycle — Address Controlled (Notes 13, 14)

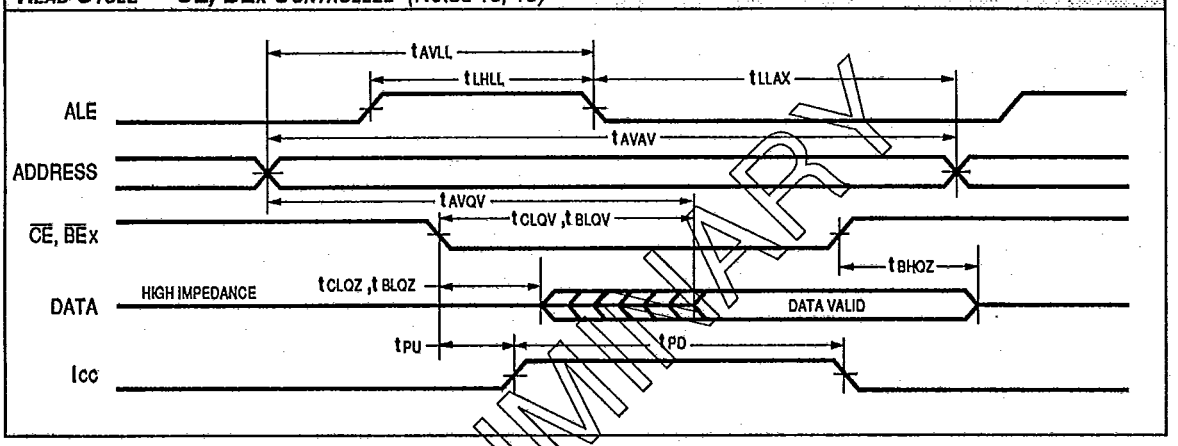


Read Cycle — ALE Controlled (Notes 13, 14)

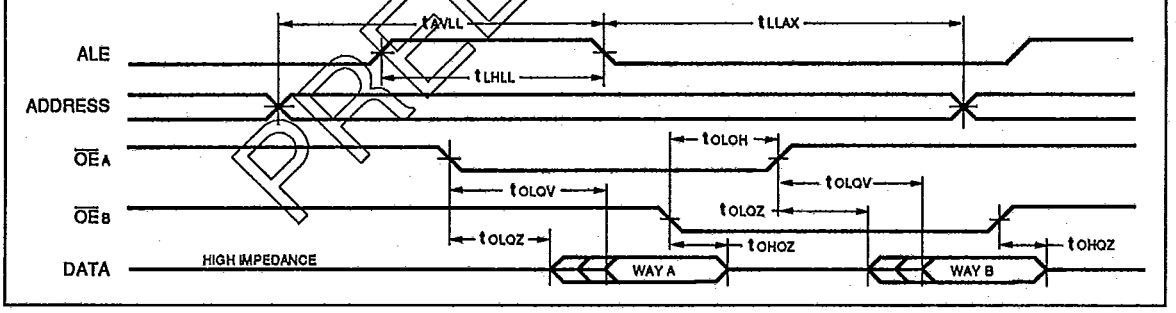


2

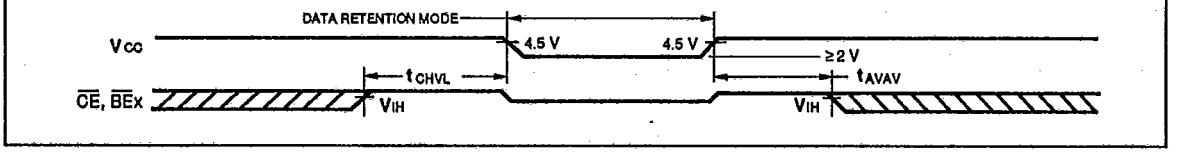
READ CYCLE — $\overline{CE}$, $\overline{BE}$x CONTROLLED (Notes 13, 15)



READ CYCLE — $\overline{OE}$ CONTROLLED (Notes 13, 15)



DATA RETENTION

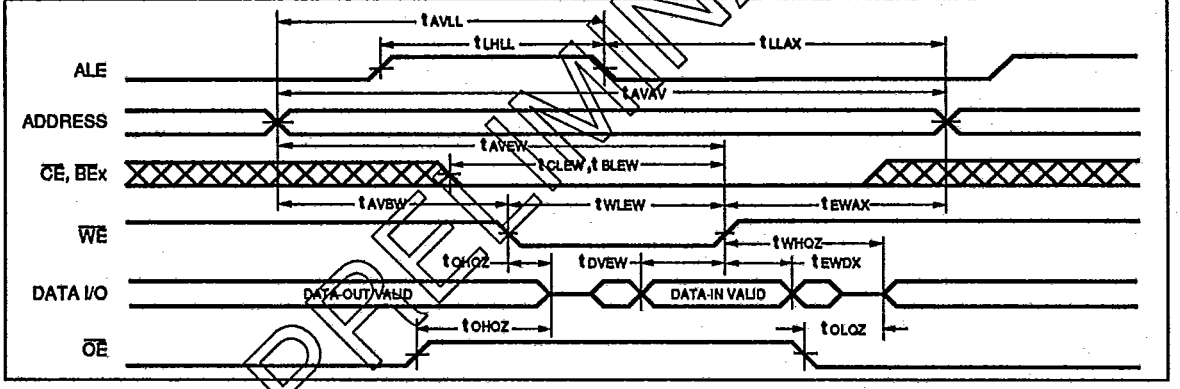


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

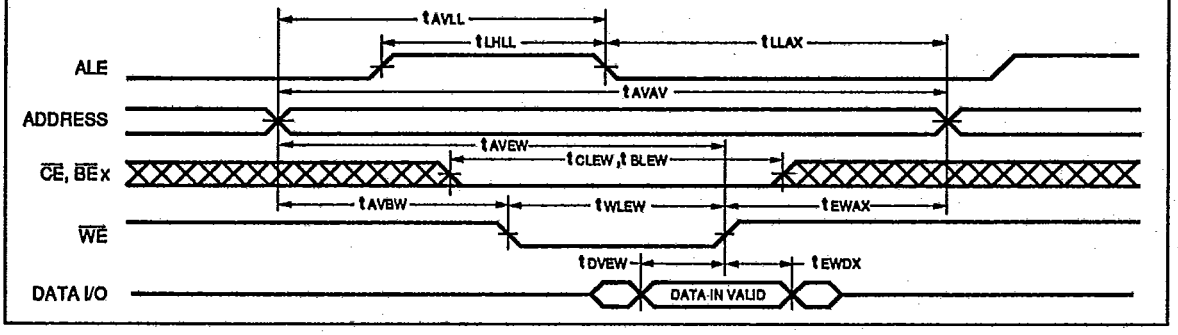
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C183/184- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max
tAVAV	Write Cycle Time	45		35		25		20	
tCLEW	Chip Enable Low to End of Write Cycle	30		20		15		12	
tBLEW	Byte Enable Low to End of Write Cycle	30		20		15		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	30		20		15		12	
tEWAX	End of Write Cycle to Address Change	2		2		2		2	
tWLEW	Write Enable Low to End of Write Cycle	30		20		15		12	
tDVEW	Data Valid to End of Write Cycle	15		10		10		8	
tEWDX	End of Write Cycle to Data Change	0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		12		10		8		8
tLHLL	ALE Pulse Width	12		10		8		8	
tAVLL	Address Valid to ALE Low	8		6		4		4	
tLLAX	ALE Low Address Change	4		4		4		4	

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



Write Cycle — CE Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE},\overline{CS} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE},\overline{CS} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE},\overline{CS} = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE},\overline{CS}$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 100 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE},\overline{CS}$ low).

15. All address lines are valid prior-to the $\overline{CE},\overline{CS}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE},\overline{CS}$ low and $\overline{WE}$ low. Both signals must be LOW to initiate a write. Either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE},\overline{CS}$ going low, the output remains in a high impedance state.

18. If $\overline{CE},\overline{CS}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE},\overline{CS}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE},\overline{CS}$ active).

c. Transition on any address line ($\overline{CE},\overline{CS}$ active).

d. Transition on any data line ($\overline{CE},\overline{CS}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE},\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

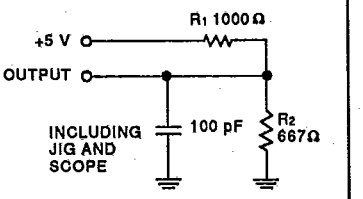


FIGURE 1b.

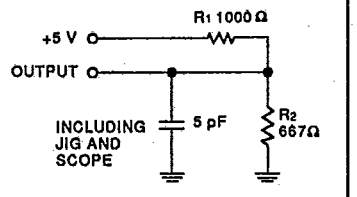
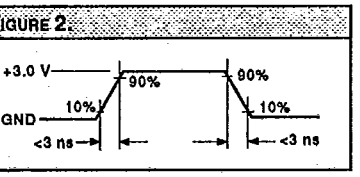
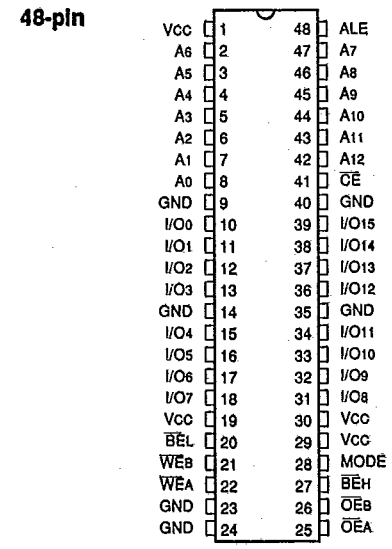


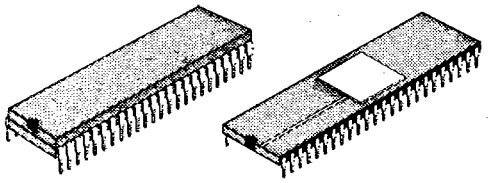
FIGURE 2.



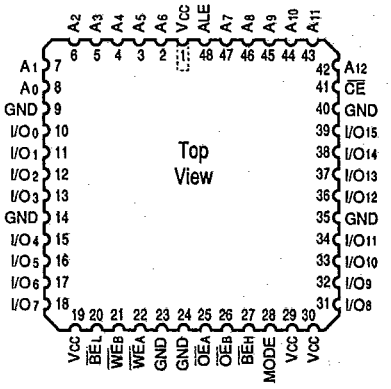
ORDERING INFORMATION

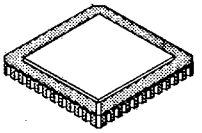
48-pin





48-pin
(550 x 550)



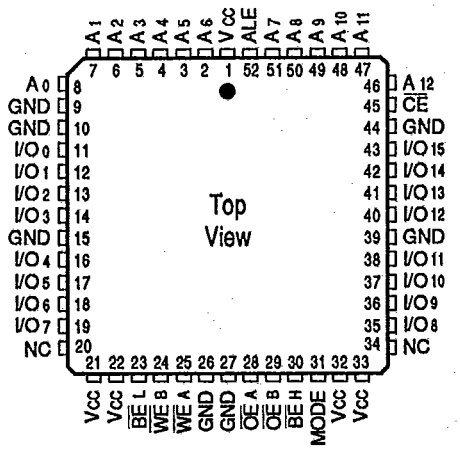


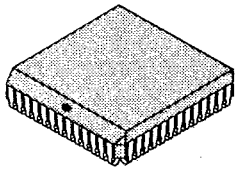
Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Ceramic Leadless Chip Carrier(K9)
	0°C to +70°C — Commercial Screening		
45 ns 35 ns 25 ns	L7C183PC or L7C184PC — 45 / 35 / 25	L7C183DC or L7C184DC — 45 / 35 / 25	L7C183KC or L7C184KC — 45 / 35 / 25
	–55°C to +125°C — Commercial Screening		
45 ns 35 ns		L7C183DM or L7C184DM — 45 / 35	L7C183KM or L7C184KM — 45 / 35
	–55°C to +125°C — Extended Screening		
45 ns 35 ns		L7C183DME or L7C184DME — 45 / 35	L7C183KME or L7C184KME — 45 / 35
	–55°C to +125°C — MIL-STD-883 Compliant		
45 ns 35 ns		L7C183DMB or L7C184DMB — 45 / 35	L7C183KMB or L7C184KMB — 45 / 35

2

ORDERING INFORMATION

52-pin





Speed	Plastic J-Lead Chip Carrier (J5)
	0°C to +70°C — COMMERCIAL SCREENING
45 ns 35 ns 25 ns 20 ns	L7C183JC or L7C184JC — 45 / 35 / 25 / 20
	–55°C to +125°C — COMMERCIAL SCREENING
45 ns 35 ns 25 ns	
	–55°C to +125°C — EXTENDED SCREENING
45 ns 35 ns 25 ns	
	–55°C to +125°C — MIL-STD-883 COMPLIANT
45 ns 35 ns 25 ns	