Description

The GMM7644200CS/SG is an 4M x 64 bits Dynamic RAM MODULE which is assembled 16 pieces of 4M x 4bit DRAMs in 24 pin SOJ package and two 16bit driver ICs in 48pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM7644200CS/SG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. The GMM7644200CS/SG provides common data inputs and outputs.

Features

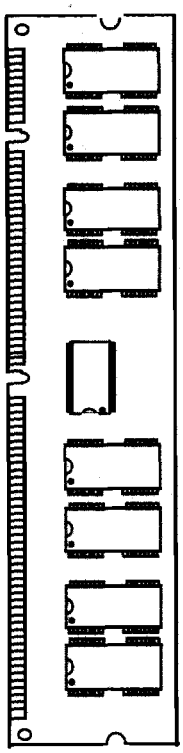
- 168 pins Dual In-Line Package
  - GMM7644200CS : Solder plating
  - GMM7644200CSG : Gold plating
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time

(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM7644200CS/SG-6	60	20	110	40
GMM7644200CS/SG-7	70	25	130	45

- Low Power
  Active : 7,040/6,160 mW (MAX)
  Standby : 418 mW (CMOS level : MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 4096 Refresh Cycles/64ms

- **GMM7644200CS/SG** (Double Side)

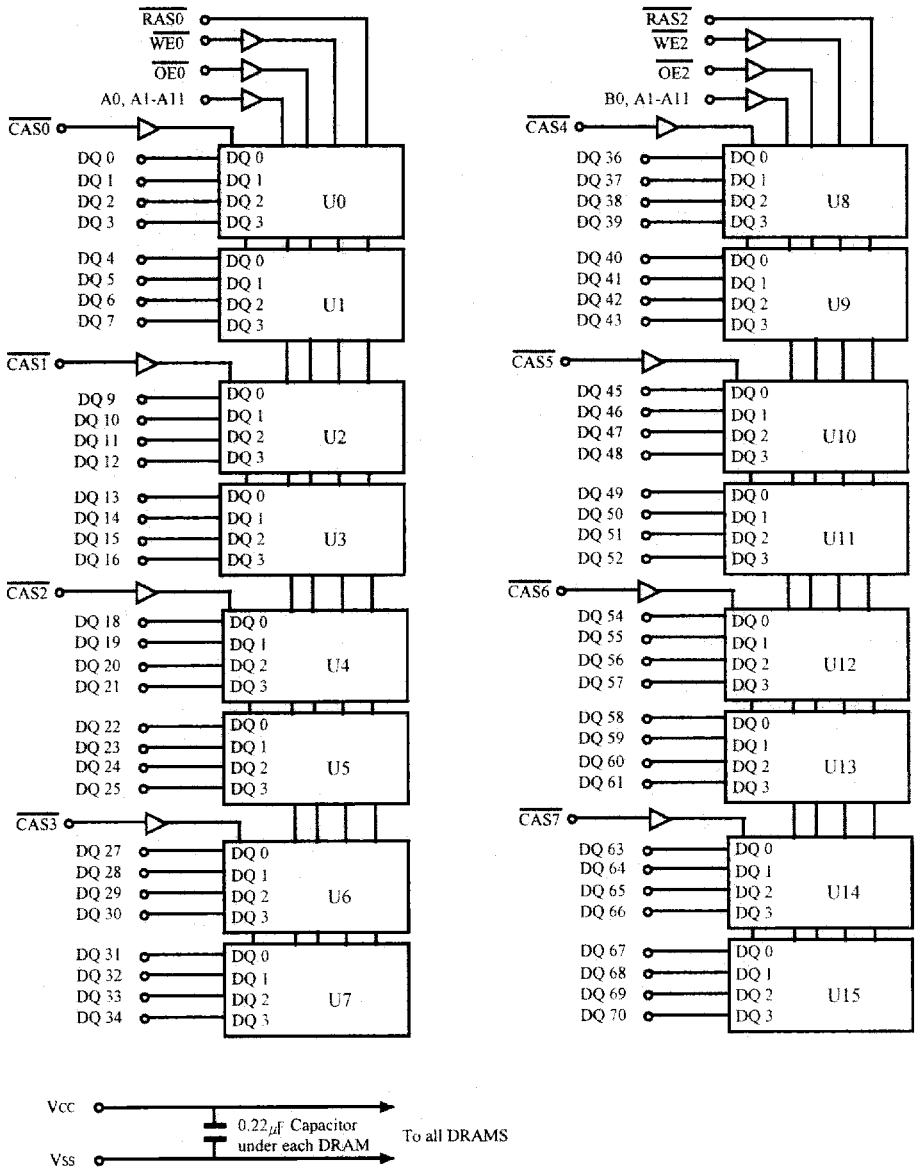


Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	29	/CAS_2	57	DQ_{22}	85	V_{SS}	113	/CAS_3	141	DQ_{58}
2	DQ_0	30	/RAS_0	58	DQ_{23}	86	DQ_{36}	114	/RAS_1*	142	DQ_{59}
3	DQ_1	31	/OE_0	59	V_{CC}	87	DQ_{37}	115	RFU	143	V_{CC}
4	DQ_2	32	V_{SS}	60	DQ_{24}	88	DQ_{38}	116	V_{SS}	144	DQ_{60}
5	DQ_3	33	A_0	61	RFU	89	DQ_{39}	117	A_1	145	RFU
6	V_{CC}	34	A_2	62	RFU	90	V_{CC}	118	A_3	146	RFU
7	DQ_4	35	A_4	63	RFU	91	DQ_{40}	119	A_5	147	RFU
8	DQ_5	36	A_6	64	RFU	92	DQ_{41}	120	A_7	148	RFU
9	DQ_6	37	A_8	65	DQ_{25}	93	DQ_{42}	121	A_9	149	DQ_{61}
10	DQ_7	38	A_{10}	66	RSVD	94	DQ_{43}	122	A_{11}	150	RSVD
11	RSVD	39	A_{12}*	67	DQ_{27}	95	RSVD	123	A_{13}*	151	DQ_{63}
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ_9	41	RFU	69	DQ_{28}	97	DQ_{45}	125	RFU	153	DQ_{64}
14	DQ_{10}	42	RFU	70	DQ_{29}	98	DQ_{46}	126	B_0	154	DQ_{65}
15	DQ_{11}	43	V_{SS}	71	DQ_{30}	99	DQ_{47}	127	V_{SS}	155	DQ_{66}
16	DQ_{12}	44	/OE_2	72	DQ_{31}	100	DQ_{48}	128	RFU	156	DQ_{67}
17	DQ_{13}	45	/RAS_2	73	V_{CC}	101	DQ_{49}	129	/RAS_3*	157	V_{CC}
18	V_{CC}	46	/CAS_4	74	DQ_{32}	102	V_{CC}	130	/CAS_5	158	DQ_{68}
19	DQ_{14}	47	/CAS_6	75	DQ_{33}	103	DQ_{50}	131	/CAS_7	159	DQ_{69}
20	DQ_{15}	48	/WE 2	76	DQ_{34}	104	DQ_{51}	132	/PDE	160	DQ_{70}
21	DQ_{16}	49	V_{CC}	77	RSVD	105	DQ_{52}	133	V_{CC}	161	RSVD
22	RSVD	50	RSVD	78	V_{SS}	106	RSVD	134	RSVD	162	V_{SS}
23	V_{SS}	51	RSVD	79	PD_1	107	V_{SS}	135	RSVD	163	PD_2
24	RSVD	52	DQ_{18}	80	PD_3	108	RSVD	136	DQ_{54}	164	PD_4
25	RSVD	53	DQ_{19}	81	PD_5	109	RSVD	137	DQ_{55}	165	PD_6
26	V_{CC}	54	V_{SS}	82	PD_7	110	V_{CC}	138	V_{SS}	166	PD_8
27	/WE 0	55	DQ_{20}	83	ID 0	111	RFU	139	DQ_{56}	167	ID 1
28	/CAS_0	56	DQ_{21}	84	V_{CC}	112	/CAS_1	140	DQ_{57}	168	V_{CC}

Note : Pins Marked * are not used in this module.

Block Diagram



Pin	Function	Pin	Function
A0-A11, B0	Address Inputs	$\overline{PDE}$	Presence Detect Enable
DQ0-DQ70	Data Input/Output	V_{CC}	Power (+5V)
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS0}$-$\overline{CAS7}$	Column Address Strobe	NC	No Connection
$\overline{WE0}$, $\overline{WE2}$	Read/Write Enable	$\overline{OE0}$, $\overline{OE2}$	Output Enable
PD 1-8	Presence Detect	RSVD	Reserved Use
ID 0-1	ID bit	RFU	Reserved for Future Use

Presence Detect Pins (Optional)

Pin	60ns	70ns
PD1	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	0	0
PD6	1	0
PD7	1	1
PD8	1	1

Refresh Mode	
	ID1
Normal	0
Self-Refresh	1

* 0 : Vss
1 : NC or Vcc

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	℃
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-0.5 ~ 7.0	V
V_{CC}	Power Supply Voltage	-0.5 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	16	W

*Note: 1. Stress greater than above Absolute Maximum Ratings may cause permanent damage to the device.

Recommended DC Operating Conditions (T_A = 0 ~ 70℃)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	-	6.5	V	1
V_{IL}	Input Low Voltage	0	-	0.8	V	1

*Note: 1. All voltages referenced to V_{SS}.

DC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70℃)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output 밑 □Level Voltage (I_{OUT} = -5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output 밥 □Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	-	1280	mA	1, 2
		70ns	-	1120		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		-	92	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	-	1280	mA	2
		70ns	-	1120		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	60ns	-	1280	mA	1, 3
		70ns	-	1120		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC}-0.2V)		-	76	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	-	1280	mA	
		70ns	-	1120		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	140	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All Other Pins Not Under Test = 0V		-160	160	㎂	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		-10	10	㎂	

Note: 1. I_{CC} depends on output load condition when the device is selected. I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, T_A = 25℃, f = 1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (A0~A11, B0)	-	20	pF	1
C_{I2}	Input Capacitance ($\overline{WE}$0, $\overline{WE}$2, $\overline{OE}$0, $\overline{OE}$2)	-	20	pF	1, 2
C_{I3}	Input Capacitance ($\overline{RAS}$0 , $\overline{RAS}$2)	-	60	pF	1, 2
C_{I4}	Input Capacitance ($\overline{CAS}$0~$\overline{CAS}$7)	-	20	pF	1, 2
$C_{I/O}$	I/O Capacitance (DQ0~DQ70)	-	20	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70℃, Notes 1, 15)

The GMM7644200CS/SG writes data only in early write cycle (twcs ≥ twcs(min)).
Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycle (Common Parameters)

Symbol	Parameter	GMM7644200 CS/SG-6		GMM7644200 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	18	10,000	ns	
t_{ASR}	Row Address Setup Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Setup Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	45	ns	9
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	25	15	30	ns	10
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	23	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{REF}	Refresh Period (4096 Cycles)	-	64	-	64	ms	

Read Cycle

Symbol	Parameter	GMM7644200 CS/SG-6		GMM7644200 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	2, 3
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	3, 4
t_{AA}	Access Time from Column Address	-	35	-	40	ns	3, 5, 14
t_{RCS}	Read Command Setup Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	ns	6
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-	ns	6
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{OFF}	Output Buffer Turn-off Time	-	20	-	20	ns	7

Write Cycle

Symbol	Parameter	GMM7644200 CS/SG-6		GMM7644200 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	23	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	18	-	ns	
t_{DS}	Data-in Setup Time	0	-	0	-	ns	12
t_{DH}	Data-in Hold Time	15	-	18	-	ns	12

Refresh Cycle

Symbol	Parameter	GMM7644200 CS/SG-6		GMM7644200 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	-	0	-	ns	
t_{WRP}	$\overline{WE}$ Setup Hold Time ($\overline{CAS}$-before $\overline{RAS}$ Refresh Cycle)	0	-	0	-	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$-before $\overline{RAS}$ Refresh Cycle)	10	-	10	-	ns	

Fast Page Mode Cycle

Symbol	Parameter	GMM7644200 CS/SG-6		GMM7644200 CS/SG-7		Unit	Note
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	ns	13
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	ns	14
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	45	-	ns	
t_{RRWC}	Fast Page Mode Read-Modify-Write Cycle Time	85	-	96	-	ns	

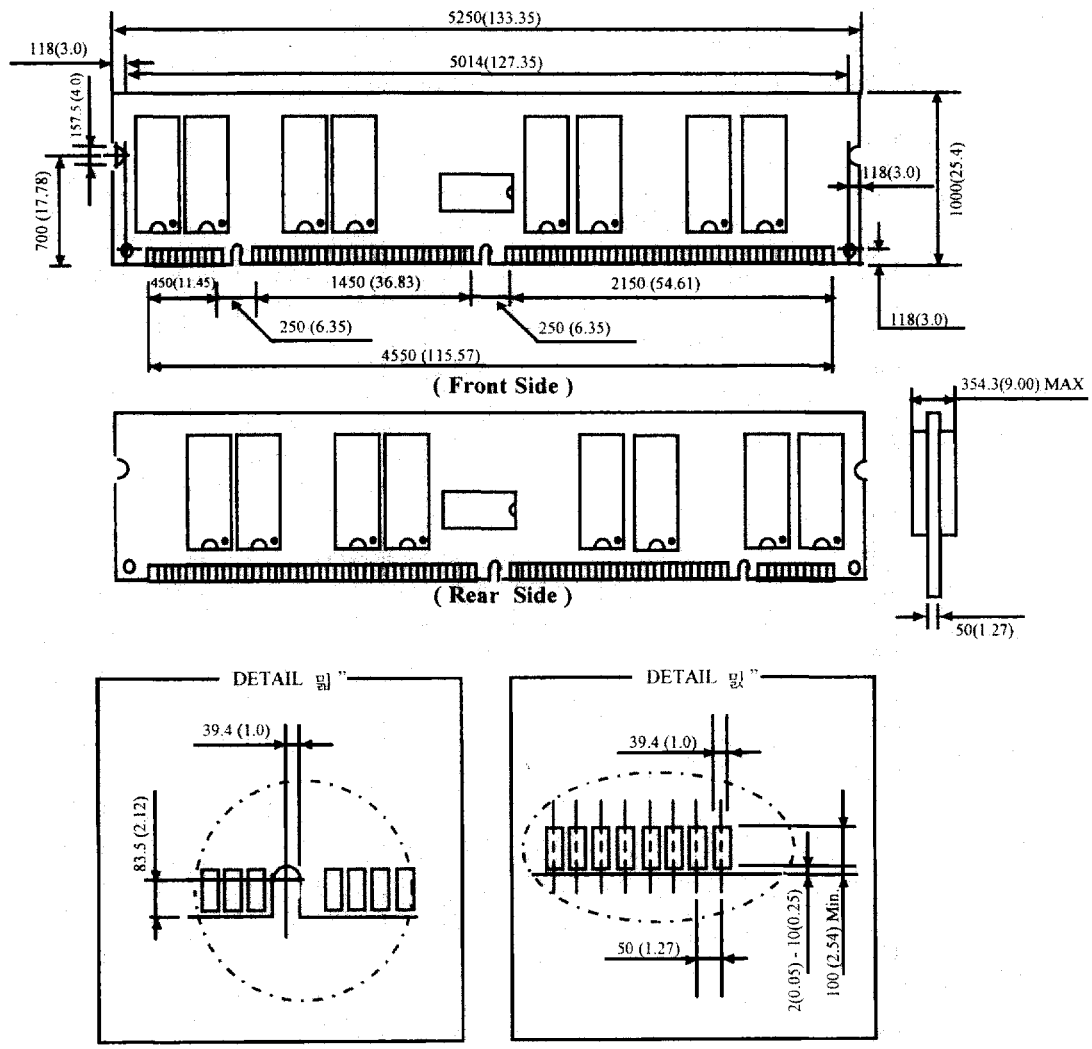
Notes:

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max).
5. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \geq t_{RAD}$(max).
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
7. t_{OFF}(max) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
8. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
10. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
11. t_{WCS} is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
13. t_{RASP} is defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.

Timing Waveforms : Please refer to attached Timing Waveform-9

Package Dimension

Unit: mil (mm)
* (1mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.